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Multilevel Converters: Dual Two-Level Inverter Scheme

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To my parents

“Zwei Dinge erfüllen das Gemüt mit immer neuer und zunehmender Bewunderung und Ehrfurcht, je öfter und anhaltender sich das Nachdenken damit beschäftigt: Der bestirnte Himmel über mir, und das moralische Gesetz in mir.”

“Two things fill the mind with ever new and increasing admiration and awe, the more often and steadily reflection is occupied with them: the starry heaven above me and the moral law within me”

Kritik der reinen Vernunft (Critique of Pure Reason). I. Kant (1724-1804).

"There are two things that are indefinite to me; the first is the universe, the second is the stupidity of mankind, and I am not sure about the first one."

A. Einstein (1879-1955).

“Patientia est honestatis aut utilitatis causa rerum arduarum ac difficilium voluntaria ac diuturna perpessio.”

“Patience is a wilful and constant tolerance of hard and difficult things with purposes of honesty and utility.”

Rhetorica - De Invenzione. Marcus Tullius Cicero (106 bC-43 bC).

Acknowledgements

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Even with other friends the relations have changed during these years, but in a slighter way. We are still meeting every week and we are still doing the same things as three years ago. Different places, different behaviours, but we continue to get fun together and to help one another. Hence, I want to thank all friends at once, because these pages would not be sufficient to contain a punctual description of the reasons why I have to thank each one among the friend of mine.

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Thank to everyone

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Preface

The first attempt of power conversion was made by Pacinotti in 1864 and then Wilde, Varley and Siemens patented the dynamo in 1866-67. With his machine Pacinotti had the possibility to convert mechanical into electrical power and vice versa. Further improvements allowed Ferraris (1885) to create a rotating electro-magnetic field able to make a metallic egg rotate. This principle is the basis of induction machine operation.

Unfortunately, both Pacinotti's and Ferraris' machines were directly connected to the power source; hence they were without any automatic control. Moreover, the problems related to not controlled start-up are relevant and well known.

Power Electronics are a viable solution to these problems and got more and more importance during the years due to the benefits they brought into electrical engineering fields. Power Electronics inherited their foundations from signal amplifier technologies and then developed to drive high powers. There are lots of advantages which Power Electronics brought, but the most meaningful is the possibility to control electrical machine and to manage the flows of electro-magnetic power. During Eighties and Nineties, the developments of Power Electronics allowed to implement innovatory systems and to improve the existent ones. Due to Power Electronics it was possible to build drives, active filters, static Var compensators, etc…

Nowadays, the static converter can connect systems with different electrical characteristics: for instance, choppers connect two DC systems with different voltage level, whereas inverters transform power from DC to AC with variable amplitude and frequency.

Unfortunately, the existing converter topologies allow a small margin to further improvements because of the intrinsic limits of semiconductor devices. Indeed, considering the electrical characteristics of switching devices, it can be asserted it will be harder and harder overcome the actual limits imposed by silicon. For instance, only slowest devices can withstand voltages of the order of magnitude of 10 kV.

The multilevel converters were born with the specific aim to overcome the voltage limit of semiconductor devices: one of their first applications was the connection between AC and DC high voltage systems. The main idea at the basis of multilevel converters is to connect more devices in series and clamp the voltages between their pins. The differences among multilevel converter structures derive from how the clamping is done. In cascade H-bridge converters the clamping is done by the batteries, diodes have this task in diode-clamped topologies, and so on.

The first multilevel converter can be attributed to R. H. Baker and L. H. Bannister, who patented the cascade H-bridge in 1975. In 1980 Baker patented diode-clamped topology which can be still considered the most used. In 1992, T. A. Meynard and H. Foch patented the flying-capacitor architecture. In the same year, S. Osagawara, J. Takagali, H. Akagi and A. Nabae proposed a new approach: they considered a standard Current Source Inverter (CSI) and increased the number of current levels instead of voltage ones. From 1992 till now, the research on multilevel converters both perfected original topologies and invented new ones, finding ever new and uncommon applications.

The former use of multilevel converter in high voltage applications is still implemented on high voltage DC transmission lines, to connect the DC side to AC grid. Moreover, low voltage applications for which multilevel are suited were discovered. In particular, multilevel converters

offer a better quality of the output waveforms than standard converters. This peculiarity is very useful to comply with the standards about the energy quality which become stricter and stricter. Moreover, multilevel converters are suited even in drive applications, because sophisticated control algorithms can exploit the high number of levels to improve the performance of the system.

Multilevel converters can bring innovations even in traction applications, a particular niche of drive applications. Considering the state of the art in this technology field, it can be asserted the maximum power limit has been reached. This fact derives both from standards and from economical reasons.

Considering land traction industrial applications, standards limit the maximum voltage of each battery banks at 96 V for safety reasons. On the other hand, standard do not impose this limit to road vehicles, but the market does. The semiconductor switches usually used in this kind of applications are MOSFETs rated 150 V because they have the smallest cost among all the devices. Hence, even if the limit on the voltage is not imposed by an actual law, it is still present in road transport applications too.

One way to overcome this problem was presented by Profumo. He proposed to use a double-wound 3-phase motor, instead of the standard ones. In this way, with two converters and two control systems the power is doubled by the injection of twice the current than a standard solution. Unfortunately, in case of fault in one inverter, the vehicle will be still able to proceed, but at reduced current that means the torque the motor produces is halved. Considering that the vehicle is at full load or in a steep slope, the reduction of the torque will mean the impossibility to move or, even worse, the vehicle will move backward.

Another viable solution to increase the power keeping constant the maximum DC voltage is given by multi-phase converters. Unfortunately, this solution is even more expensive than the previous because both multiphase converter and motor are custom-made. Moreover, even the control system must be designed for the specific number of phases and may require a lot of resources.

The dual 2-level inverter, the multilevel converter topology studied and proposed in this dissertation, represents the third way to overcome the power limit. Considering battery-fed applications, the two insulated sources can be easily found splitting the battery bank in two parts. Moreover, all the 3-phase machines allow the six-wire open-end connection required by this system. Hence, using only standard components connected in an unusual way, it is possible to twice the power delivered to the load.

The use of standard converters and motors has intrinsic advantages in term of costs and reliability. Furthermore, in case of fault of one inverter, the vehicle will be able to move producing the rated torque, but at half the rated speed because the system will lack voltage instead of current. Hence, the vehicle will move slower, but it will be still able to scour slopes.

For these reasons, dual 2-level inverter is well suited for land traction application, but even other applications can have benefits deriving from the exploitation of the peculiarities of the dual 2-level inverter. In particular naval hybrid traction and active filter applications have been proposed for that converter type.

Naval traction can use this converter together with two diesel engines to have two selectable power levels. Indeed some ships, like fishing boats, must operate in two cruise modalities. During fishing operations, the trawl-nets represent a load requiring great torque, but low power: only one inverter and one engine can be used to guarantee the required power and a pretty good efficiency of mechanical system. On the other hand, when the boat is moving, the required power is largely more, and the dual 2-level inverter must be fully used together with the two engines. In this way the overall efficiency of the system can be improved in both cruise modalities.

Regarding active filtering, a possible application of the dual 2-level inverter has been found and it is being currently investigated at the Department of Electrical Engineering of Bologna. Being a quite new application for the dual 2-level inverter, a summary of the benefit brought by the

converter is actually a hard job. Anyway the direction assumed by the research is to use two photovoltaic panels to provide power and a 3-phase transformer for the connection to the grid.

The investigation on the dual 2-level inverter is a research theme which offers several prospects because the converter itself has the possibilities to be widely used. It has some advantages proper of the multilevel converters, but does not require any custom-built hardware. Moreover, converter architecture suggests the idea to manage the power flowing throughout the two inverters offering a way to control the discharge of battery banks, for instance.

The following dissertation has the aim to investigate this multilevel topology, starting from the basis. A survey of multilevel topologies and modulation will introduce to the accurate description of the dual 2-level inverter. Two modelling methodology for this converter will be analysed: one is the use of space vectors, the other is based on complex duty-cycle theory. Using these mathematical tools, a power sharing technique will be presented together to the analytical study of its effects during commutations. To conclude, two converter have been built and some experimental results will be shown, proving that power sharing can be realized.

Chapter 1

Survey of topologies

1.1. Introduction

1.1.1. Short history

The concept of utilizing multiple small voltage levels to perform power conversion was presented by an MIT researcher over twenty years ago [1,2]. Advantages of this multilevel approach include good power quality, good **Electro-Magnetic Compatibility** (**EMC**), low switching losses and high voltage capability. The main disadvantages of this technique are the larger number of semiconductor switches required than the 2-level solution and the capacitor banks or insulated sources needed to create the voltage steps on the DC busses. The first topology introduced was the **series H-bridge** design [1]. This was followed by the **diode-clamped** converter [2-4] which utilises a bank of series capacitors to split the DC bus voltage. The **flying-capacitor** (or **capacitor-clamped**) [5] topology followed diode-clamped after few years: instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels. Another multilevel design, slightly different from the previous ones, involves **parallel connection** of inverter phases through inter-phase reactors [6]. In this design the semiconductors must block the entire voltage, but share the load current. Several combinatorial designs have also emerged [7], implemented cascading the fundamental topologies [8-12]; they are called **hybrid topologies**. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels.

In the beginning multilevel converters were introduced to drive high voltages, like in **High Voltage Direct Current** (**HVDC**) applications to make the front-end connection between DC and AC lines. In this way the limits on the maximum voltage tolerable by the semiconductor switches were overtaken and the converters were able to drive directly the line voltage without a transformer. Nowadays it is possible to find multilevel applications even in low voltage field, like motor drive, because of the high quality of the AC output. In particular back-to-back multilevel systems can drive motors with very good performance concerning the line voltage and current distortions. Multilevel can even improve the converter losses.

Recent advances in power electronics have made the multilevel concept practical [1-19]. In fact, the concept is so advantageous that several major drive manufacturers have obtained patents on multilevel power converter and associated switching techniques [20-26].

1.1.2. Multilevel concept

This paragraph has the aim to introduce to the general principle of multilevel behaviour. Figure 1.1 helps to understand how multilevel converters work. The leg of a 2-level converter is represented in Figure 1.1a) in which the semiconductor switches have been substituted with an ideal switch. The voltage output can assume only two values: 0 or E. Considering Figure 1.1b), the voltage output of a 3-level inverter leg can assume three values: 0, E or $2E$. In Figure 1.1c) a generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, then the voltage levels can be different. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following.

A three-phase inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is n. The number k of the line-to-line voltage levels is given by (1.1).

$$k = 2n - 1. \tag{1.1}$$

Considering a star connected load, the number p of phase voltage levels is given by (1.2).

$$p = 2k - 1. \tag{1.2}$$

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels.

Higher is the number of levels better is the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 2-level inverter.

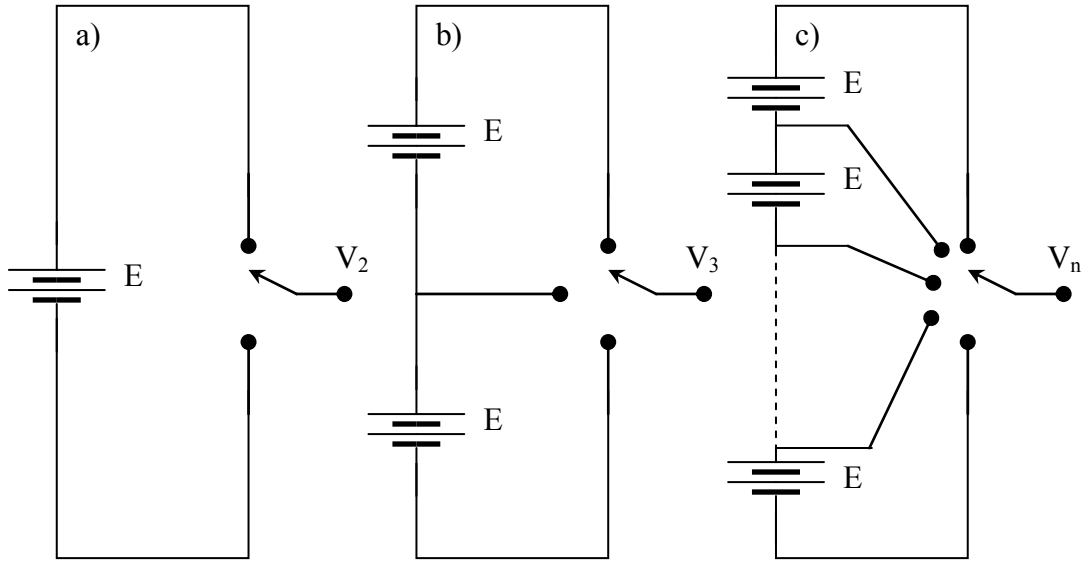


Figure 1.1: Inverter phases. a) 2-level inverter, b) 3-level inverter, c) n-level inverter.

1.1.3. Redundant states and voltage vectors

Two or more switching states that produce the same output voltage are called **redundant states**. It is possible to distinguish between two kind of redundant states: **intra-phase** and **joint-phase**. Intra-phase redundant states involve the switching state (or configuration) of only one phase; obviously this kind of redundancy is strictly related to the hardware architecture of the converter. Just to make an example, flying-capacitor converter has intra-phase redundant states; instead diode-clamped does not.

On the other hand, joint-phase redundant states involve the switching state of the whole converter and all multi-phase converters present this phenomenon. Because of the dependency on the architecture, intra-phase redundancy will be analyzed for each single converter presented in this chapter. The aim of this paragraph is to introduce the joint-phase redundancy through the use of Park transform. In order to simplify the discussion, a general three-phase n-level inverter is taken into account as shown in Figure 1.2. Furthermore, the load is supposed to be star-connected and of linear type. In this system it is possible to define three inverter voltages (v_{aO}, v_{bO}, v_{cO}). Assuming that all the voltage steps have the same value E, each inverter voltage can be expressed as:

$$v_{xO} = E \cdot s_x . \tag{1.3}$$

In (1.3), v_{xO} is the general inverter voltage and s_x is the state of the generic leg. The values assumed by s_x are limited between 0 and $n-1$ (where n is the number of levels). For example, in a 3-level inverter s_x can assume the values 0, 1, 2.

Assuming $\overline{\alpha} = e^{j\frac{2}{3}\pi}$ and applying Park transform [27] to inverter voltages, the related voltage vector and the common mode voltage can be expressed as follow:

$$\begin{aligned} \overline{v} &= \frac{2}{3}\left(v_{aO} + v_{bO}\overline{\alpha} + v_{cO}\overline{\alpha}^2\right) \\ v_o &= \frac{1}{3}\left(v_{aO} + v_{bO} + v_{cO}\right) \end{aligned} . \tag{1.4}$$

Similarly, it is possible to define three load voltages ($v_{aO'}, v_{bO'}, v_{cO'}$) and obtain $\overline{v}'$ and v_o', which represent as the load voltage vector and common mode voltage respectively. Because the load is star-connected and linear, the common mode voltage must be zero. Applying Kirchhoff's voltage law to a generic phase x, the following equation is obtained.

$$v_{kO} = v_{kO'} + v_{O'O} . \tag{1.5}$$

Substituting (1.5) in (1.4) for each phase, yields:

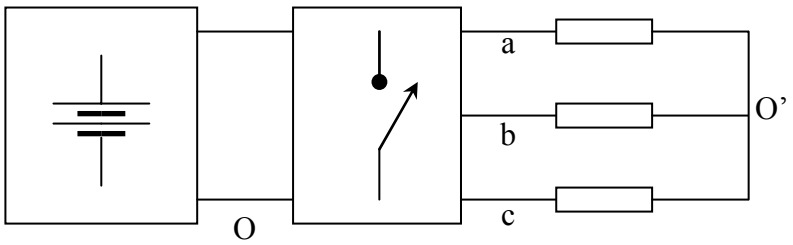


Figure 1.2: General three-phase inverter scheme.

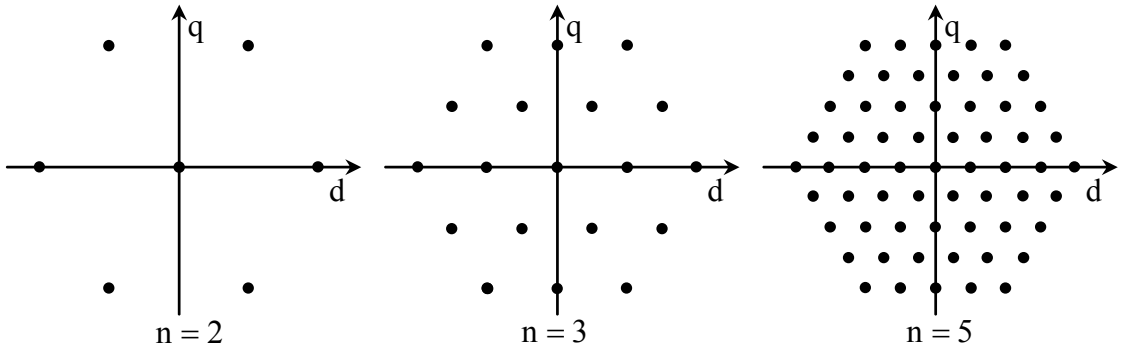


Figure 1.3: Space vectors generated by 2-level, 3-level and 5-level inverters.

$$\begin{aligned} \overline{v} &= \overline{v}' \\ v_o &= v_{O'O} \end{aligned} . \qquad \textbf{(1.6)}$$

Because the load common mode voltage is always zero, the first of (1.6) implies that the load voltages are not dependent on the common mode component of inverter voltages; in other words each set of voltages $\{v_{aO}, v_{bO}, v_{cO}\}$ applied by the inverter has the same effect on the load. Anyway, different sets of voltages may have different effects on the sources or on the converter components. For instance, redundant vectors are used in diode-clamped converter to balance the voltage level of DC capacitors.

The number of voltage sets n_{vs} an inverter can produce and the number of different voltage vector n_v can be expressed as follow:

$$n_{vs} = n^3 \qquad \textbf{(1.7)}$$

$$n_v = 3n(n-1)+1. \qquad \textbf{(1.8)}$$

Moreover, to distinguish among different switching states a converter can assume, it is possible to use the following equation which gives an univocal number (n_{sw}) for each state.

$$n_{sw} = n^2 s_a + n s_b + s_c . \qquad \textbf{(1.9)}$$

Given a specific voltage vector and its related leg states set $\{s_a, s_b, s_c\}$, the number of joint-phase redundant states n_{rs} can be expressed as follow:

$$n_{rs} = n - (s_{max} - s_{min}). \qquad \textbf{(1.10)}$$

In (1.10), s_{max} and s_{min} are the maximum and the minimum among $\{s_a, s_b, s_c\}$ respectively. The voltage space vectors generated by 2-level, 3-level and 5-level inverters are shown in Figure 1.3. Increasing the number of levels means an increment in the resolution of generable vectors. Obviously the diagrams presented in Figure 1.3 are obtained considering the same voltage step for each level. In case of different level amplitude, the number of generable vector can increase until it reaches the number of voltage sets if proper ratios among the level amplitudes are chosen. In [28-30] there is a better explanation of this use of redundant configuration.

1.1.4. Multilevel inverter performance

The limit of standard three-phase converters is related to the maximum power. Which can be delivered to the load, which is related to the maximum voltage and current of a component. Furthermore, higher is the power of a switch lower is the switching frequency. An initial solution to overcome this problem was to connect several switches in series or in parallel. The series connection of two or more semiconductor devices is really difficult due to the impossibility to perfectly synchronize their commutations. In fact, if one component switches off faster than the others it will blow up because it will be subjected to the entire voltage drop designed for the series. Instead, parallel connection is slightly less complicated because of the property of MOSFETs and more recent IGBTs to increase their internal resistance with the increment of junction temperature. When a component switches on faster than the others, it will conduct a current greater than the current it was designed for. In this way, the component increases its junction temperature and its resistance, so it limits the current which flow through it. This effect makes possible to overcome the problems coming from a delay among gate signals or from differences among real turn on time of the components. Anyway, parallel connection of the switches requires an accurate design of the board.

A modular solution is preferred to increase the power a converter can drive. In this way, a standard three-phase converter is designed with a relatively low power. Then, several converters are paralleled through decoupling inductances to reach the desired power. Even in this system a quite good synchronization among the controls of the converters is required.

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, multilevel converters present several other advantages. First of all, multilevel converters generate better output waveforms with a lower $\frac{dv}{dt}$ than the standard converters. Then, multilevel converter can increase the power quality due to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses. Furthermore, multilevel converter can operate with a lower switching frequency than 2-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Furthermore, multilevel converters can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

1.2. Diode-clamped

1.2.1. Operating principle

In Figure 1.4, 3-level and 5-level diode-clamped legs are shown; it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called **clamping diodes**. Considering the 5-level diode-clamped leg, it is possible to note that the number of diodes required to clamp the voltage changes point by point. For instance D_1 is composed only by one diode, instead D_1' is the series of three diodes. This does not mean that the diode series connection is needed in the implementation, but it simply means that the reverse voltage drop born by D_1' is three times the backward voltage drop over D_1. In the final implementation it is allowed to use either one diode with higher blocking capability or three diodes series connected. Anyway, to better understand how a diode-clamped works, it is preferred to use

series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor.

For a generic n-level diode-clamped the diode reverse voltage is given by (1.11):

$$V_r = \frac{E}{n-1}. \qquad \textbf{(1.11)}$$

In 3-level diode-clamped it is $V_r = E/2$ while in 5-level it is $V_r = E/4$. Furthermore, this voltage drop is also the reverse voltage each switch has to block. Now it is clear that increasing the levels means a reduction of the stress over the components, considering the same DC bus voltage.

Unfortunately, higher is the number of levels higher is the number of components. Increasing of one level involve the use of one capacitor, two switches and a lot of diodes more. In fact the number of clamping diodes used in a diode-clamped is related to the number of level by the following expression:

$$N_{Diodes} = (n-1)(n-2). \qquad \textbf{(1.12)}$$

Focusing the attention to the 3-level leg, it is possible to find the relationship between the state of the switches and the output voltage V_{AO}. Before all consideration, a right switches configuration must avoid every kind of shortcut. So, it is simple to understand that all the switches cannot be

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	1	0	0	E
0	1	1	0	$E/2$
0	0	1	1	0
1	0	0	1	Undefined

Table 1.1: 3-level diode-clamped leg relationships between configurations and output voltages.

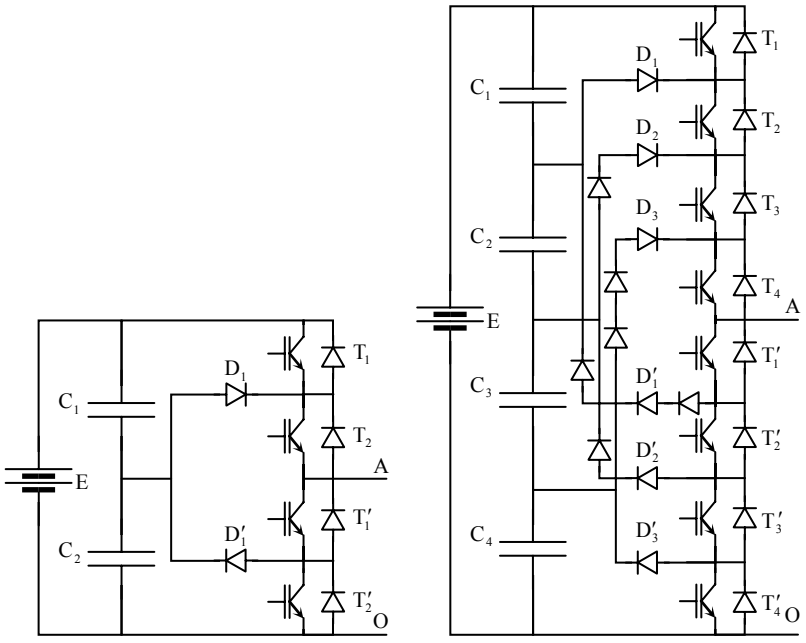


Figure 1.4: 3-level and 5-level diode-clamped legs.

simultaneously turned on. There are also other dangerous configuration, but they can be avoided switching T_1 and T_1' in a complementary way. The same has to happen for T_2 and T_2'. Considering these conditions there are only four possible configurations a 3-level diode-clamped leg can assume and they are shown in Table 1.1 with the agreement to identify switches on-state with 1 and off-state with 0. Not all the four configuration leads to a proper leg output voltage, because when T_1 in on and T_2 is off there is no defined path for the load current because whether T_2 or T_1' are not conducting, so the current flows throughout the free-willing diodes and the output voltage depends on it. As it is possible to see from Table 1.1, there are no intra-phase redundant states in 3-level diode-clamped.

Similarly, 5-level diode-clamped leg does not present redundant states and only five different configurations are allowed for the switches as Table 1.2 shows.

Switches state								
T_1	T_2	T_3	T_4	T_1'	T_2'	T_3'	T_4'	V_{AO}
1	1	1	1	0	0	0	0	E
0	1	1	1	1	0	0	0	$3E/4$
0	0	1	1	1	1	0	0	$E/2$
0	0	0	1	1	1	1	0	$E/4$
0	0	0	0	1	1	1	1	0

Table 1.2: 5-level diode-clamped leg relationships between configurations and output voltages.

Making some generalization from Table 1.1 and Table 1.2, in a n-level diode-clamped leg there are no intra-phase redundant states and $n-1$ consecutive switches are conducting. Moving the series of conducting switches from the top to the bottom end of the leg, the output voltage decreases from E to 0.

1.2.2. Characteristics

Diode-clamped converter presents some peculiarities which other multilevel topologies do not have. First of all, it is quite simple to control. Indeed, a simple extension of a traditional analog PWM control can directly gate the switches without any switching table in between. The main problems related to its control came from the digital controller which are suited for traditional 2-level converters and may not have outputs enough to drive all the semiconductors in the leg. But it is quite easy to implement a digital control system over a diode-clamped with commercial parts only, using some external hardware and designing a proper code.

Unfortunately, the reverse voltage drop changes among the components. The minimum reverse voltage drop is given by (1.11) and it is related to all the switches and some clamping diodes. For instance, considering the 5-level converter in Figure 1.4, the diode D_1' is subjected to three times the minimum reverse voltage drop when T_2' T_3' and T_4' are conducting. Anyway this is not a serious disadvantage because it can be avoided using a series of more diodes or a different kind rated for a greater reverse voltage.

A very serious problem regards the mean current through the switches which is different. Considering the 5-level leg, T_1 is conducting only when the required output voltage is E, while T_4 is always conducting but when the required voltage is 0. Furthermore, the current flowing throughout T_4 is always flowing even through T_1. So it is possible to assert that T_4 average current is smaller than T_1 average current. Choosing different kind of switches with the same reverse voltage and similar dynamic performances, but with different rated currents is quite difficult among

commercial parts. Manufacturers prefer to use the same switch for every position even if they are not fully exploited somewhere in the leg.

Diode-clamped does not require insulated DC sources to create the voltage level, but exploits several capacitors to equally split a single DC source. This is a great advantage because makes the circuitry topology suitable to substitute a traditional system in all kinds of application: to upgrade an existing system it is necessary only to design a proper diode-clamped, take out the old converter and use the new one in its place. Unfortunately, some unbalance of capacitors voltages can take place and the control must keep it into consideration. A single leg can not face this problem because there are no intra-phase redundant states to use for this purpose. In the other hands, multi-phase diode-clamped converter can balance the capacitors voltages using joint-phase redundant states. Furthermore, when this kind of converter is connected in a back-to-back configuration, a proper synchronization between inverter and rectifier controls is sufficient to keep the capacitors balanced.

1.3. Flying-capacitor

1.3.1. Operating principle

In Figure 1.5, 3-level and 5-level flying-capacitor legs are shown and it can be seen a close similarity with diode-clamped topology. The extension to more than 5 levels is easy even for flying-capacitor. As for the diodes in diode-clamped, the capacitors series are drown to highlight the voltage drop they have to tolerate. Indeed, the voltage over the capacitors nearer to the switches is lower than the voltage over the ones nearer to the source in steady-state. The voltage over each capacitor in Figure 1.5 is given by (1.13).

$$V_C = \frac{E}{n-1}. \qquad \textbf{(1.13)}$$

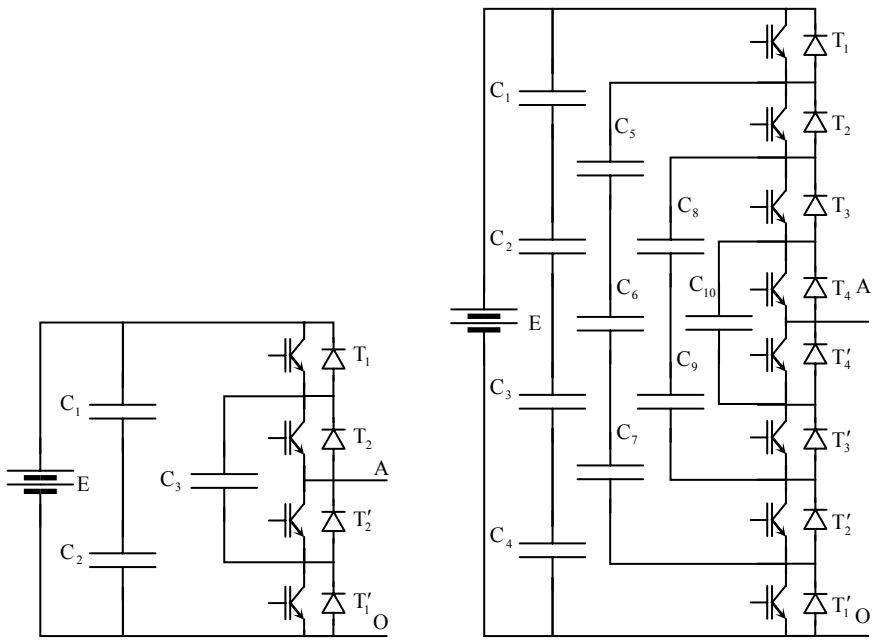


Figure 1.5: 3-level and 5-level flying-capacitor leg.

Furthermore, these capacitors have the same function of the clamping diodes in diode-clamped converter: they keep constant the voltage drop between the busses to which they are connected. For this reason, they are called **clamping capacitors**. The voltage given by (1.13) is also the reverse voltage drop each switch must bear when all capacitors are fully charged as it can be seen applying Kirchhoff's voltage law to the circuit in Figure 1.5.

Like in every converter, some leg switches configurations are not allowed. For instance, considering the 3-level converter, T_2 and T_2' cannot be simultaneously closed because this means a shortcut of C_3. To avoid any problem coming from a possible shortcut of capacitors or sources, T_x and T_x' (where the subscript x substitutes the number of a generic switch) must to be in complementary state. In this way the possible configurations for an n-level leg are:

$$N_{conf} = 2^{n-1}. \qquad \textbf{(1.14)}$$

Obviously, flying-capacitor leg presents intra-phase redundancy because the number of allowed configurations is greater than the number of possible voltage output levels. In Table 1.3 the 3-level converter switching table is presented.

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	1	0	0	E
1	0	0	1	$E/2$
0	1	1	0	$E/2$
0	0	1	1	0

Table 1.3: 3-level flying-capacitor leg relationships between configurations and output voltages.

Switches state								
T_1	T_2	T_3	T_4	T_1'	T_2'	T_3'	T_4'	V_{AO}
1	1	1	1	0	0	0	0	E
1	1	1	0	0	0	0	1	$3E/4$
1	1	0	1	0	0	1	0	$3E/4$
1	0	1	1	0	1	0	0	$3E/4$
0	1	1	1	1	0	0	0	$3E/4$
1	1	0	0	0	0	1	1	$E/2$
1	0	1	0	0	1	0	1	$E/2$
1	0	0	1	0	1	1	0	$E/2$
0	1	1	0	1	0	0	1	$E/2$
0	1	0	1	1	0	1	0	$E/2$
0	0	1	1	1	1	0	0	$E/2$
1	0	0	0	0	1	1	1	$E/4$
0	1	0	0	1	0	1	1	$E/4$
0	0	1	0	1	1	0	1	$E/4$
0	0	0	1	1	1	1	0	$E/4$
0	0	0	0	1	1	1	1	0

Table 1.4: 5-level flying-capacitor leg relationships between configurations and output voltages.

For a 3-level flying-capacitor, there are 4 possible leg configurations and two of them gives the same voltage level presenting intra-phase redundancy as expected. These two configuration have different effects on the capacitor C_3. Indeed, considering an outgoing output current, the configuration with T_1 turned off and T_2 turned on makes C_3 discharging because the capacitor has to feed the load. Whereas, when T_1 is turned off and T_2 is turned off, C_3 and the load are series connected to the source and the current flowing into the capacitor charges it. A proper control can keep the capacitor balanced monitoring its state and choosing the right configuration each time the middle output is required. A similar analysis can be done for the 5-level converter taking into account the effects of all the sixteen configurations shown in Table 1.4.

Considering Table 1.3 and Table 1.4, it is possible to deduce that the voltage applied is proportional to the sum of upper switches states. Assuming that T_x represents the state of a generic upper switch, (1.15) shows this relationship.

$$V_{AO} = \frac{E}{n-1}\sum_{x=1}^{n-1} T_x \ . \qquad \textbf{(1.15)}$$

1.3.2. Characteristics

The main disadvantage of flying-capacitor architecture is capacitors balance. In a 3-level converter there is only one capacitor to keep balanced and the implementation of the control algorithm is quite easy. When the number of level rises, the voltages to keep controlled increase: a greater number of voltage sensors and a more complicated control are needed.

Even for this topology, the switch average currents could be different because they strictly depend on the control choice of redundant states. Some estimations of this value can be done, but is difficult to rate each switch for the exact current value. Like in diode-clamped implementation, a not fully exploitation of some switch is preferred.

The flying-capacitor converter has a very modular circuit as can be seen in Figure 1.6. In Figure 1.6a) an alternative layout for the 3-level converter is shown. This representation highlights the modules making up the flying-capacitor and one of them is separately shown in Figure 1.6b). The only difference among converter modules is the voltage born by the capacitor. After a module has been designed, making up the hardware for a n-level converter is quite easy and fast. Also the maintenance has its own benefits coming from this characteristic.

Another important peculiarity of this converter is the high portability. Indeed the flying-capacitor can substitute a standard 2-level converter even more easily than the diode-clamped because the DC bus capacitor is still present and correctly rated, so there is no need to change it.

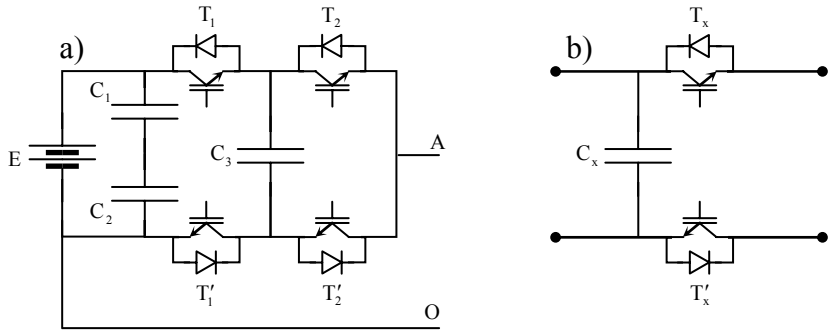


Figure 1.6: a) Alternative 3-level flying-capacitor layout, b) Generic module.

1.4. Cascaded H-bridge

1.4.1. Operating principle

Figure 1.7 shows 3-level and 5-level cascaded H-bridge legs. As usual, the 3-level converter analysis is the simplest and lets understand the operating principle of the modules composing the leg of a generic n-level converter; these modules are often called **cells**. It is well known that H-bridge converters can be modulated with 2-level or 3-level output. In this kind of multilevel converter, all the possible cell output levels are exploited. Some switches configurations are harmful for the converter and they must be avoided; for instance, the switches T_1 and T_1' are not allowed to be turned on at the same time because this situation causes a shortcut of the source. Table 1.1Table 1.5 shows the relationship between the allowed switches configurations and the output of a 3-level cascaded converter.

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	0	0	1	E
1	1	0	0	0
0	0	1	1	0
0	1	1	0	- E

Table 1.5: 3-level cascaded H-bridge leg relationships between configurations and output voltages.

It can be seen that even cascaded converter presents an intra-phase redundancy because there are two different ways to obtain the level 0. Moreover, considering the same DC source voltage, the output level amplitude and the switches reverse voltage drop (given by (1.16)) are greater here than in the diode-clamped or flying-capacitor.

$$V_r = E\,. \qquad \textbf{(1.16)}$$

In order to increase the number of levels more cells have to be cascaded. High and low couple of switches can be defined in the respect of voltage output direction. Considering Figure 1.7 , the couple of switches composed by T_1 and T_1' is the high one, whereas T_2 and T_2' constitute the low couple. The high output of one cell is shortcut to the low output of another one to realize a cascade

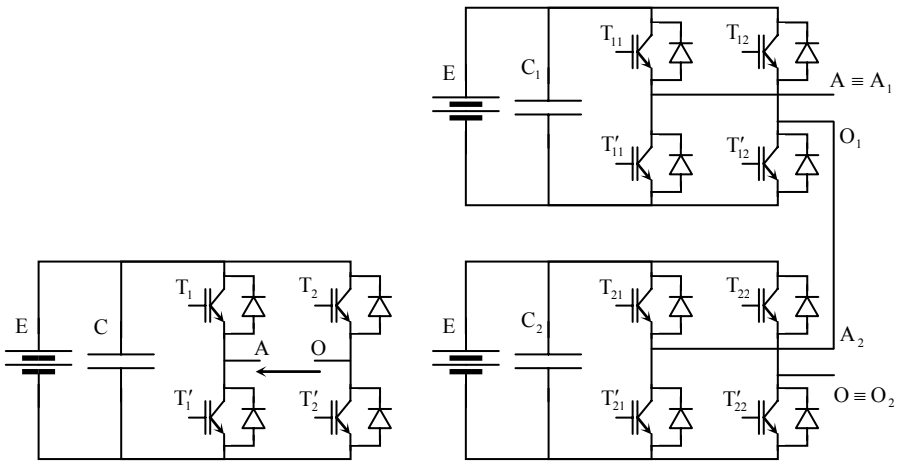


Figure 1.7: 3-level and 5-level cascaded H-bridge leg.

connection between two cells. Each cell in the cascade adds 2 levels more to the output waveform as Table 1.6 shows for a 5-level leg.

Switches state								
T_{11}	T_{12}	T_{21}	T_{22}	T'_{12}	T'_{12}	T'_{21}	T'_{22}	V_{AO}
1	0	1	0	0	1	0	1	2E
1	1	1	0	0	0	0	1	E
1	0	0	0	0	1	1	1	E
1	0	1	1	0	1	0	0	E
0	0	1	0	1	1	0	1	E
1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	- E
0	0	0	1	1	1	1	0	- E
0	1	0	0	1	0	1	1	- E
1	1	0	1	0	0	1	0	- E
0	1	0	1	1	0	1	0	- 2E

Table 1.6: 5-level cascaded H-bridge leg relationships between configurations and output voltages.

Applying Kirchhoff's voltage law to the 5-level leg, the total output voltage V_{AO} results to be the sum of single cell output voltages as (1.17) shows for a converter composed by m cells each one supplying an output voltage V_{AOj}.

$$V_{AO} = \sum_{j=1}^{m} V_{AOj} \,. \qquad \textbf{(1.17)}$$

Unfortunately, one more insulated source is required for each cell in the cascade to eliminate possible shortcuts. For example, considering a 5-level converter and the last configuration of Table 1.6, switches T'_{21} and T'_{12} make a shortcut of the lowest source if it is not insulated from the upper one.

A direct comparison between this cascaded converter and other multilevel topologies presented till here cannot be done because of different level amplitude. Imagining a substitution of the converter in an existing system, the better comparison hypothesis is to adapt the DC bus for the new converter keeping the same voltage value and splitting it. In this way, the voltage step amplitude for a n-level diode-clamped or flying-capacitor is given by (1.13) where E is the total bus DC voltage. Whereas the voltage step amplitude of a cascade converter is given by (1.18).

$$\frac{2E}{n-1}. \qquad \textbf{(1.18)}$$

The cascade H-bridge was the founder of cascade converter family and the simplest one. Each type of single-phase multilevel converter can be cascaded to obtain a leg. In this way, the levels each cell adds increase and is a good compromise between the required insulated sources and the number of output levels.

1.4.2. Characteristics

Cascade H-bridge converter is a very modular solution based on a wide commercialized product. This has a good repercussion on the reliability and the maintenance of the system since the cells have high availability, intrinsic reliability and a relatively low cost.

The main disadvantage of this converter consists in requiring several insulated sources that are not available in all applications. For instance, there are high costs in making insulated sources for induction motor drive systems because it requires isolation transformers. At the same time, this disadvantage makes cascade converters more suitable for photovoltaic or battery fed applications than the other types. Indeed, photovoltaic panels can easily be rearranged in several insulated sources to feed cascade H-bridge cells. A similar operation can even be done with battery banks.

Moreover, the insulated sources can be substituted with capacitors when the converter is used as active filter. In such kind of applications, the active power through the converter is theoretically zero, so there is no need to have power sources. Anyway, the converter has its own losses and the capacitors have to supply a little active power that discharges them. A simple control, sensing the voltage of each capacitor and exploiting either the intra-phase or joint-phase redundancies, can be done to avoid this problem. In this way, the active power to feed the converter is absorbed from the net and the capacitors feed reactive power only.

There are other several application dependent ways to exploit intra-phase redundancy proper of this converter. As an example, considering a three-phase system and a vector modulation, control can choose among the redundant configurations the one which needs the fewest commutations to be reached.

While there are no limitations on the level of diode-clamped or flying-capacitor, which can be even or odd, cascade H-bridge can have only odd numbers of levels; indeed the first cell gives three levels whereas the others always add two levels more.

1.5. Multi Point Clamped (MPC)

1.5.1. Operating principle

Multi Point Clamped (**MPC**) are so called since in their architecture there are several points clamped to specific voltages using some components. Even diode-clamped converter belong to this family because the bus between two switches is clamped by a clamping diode. Furthermore, when

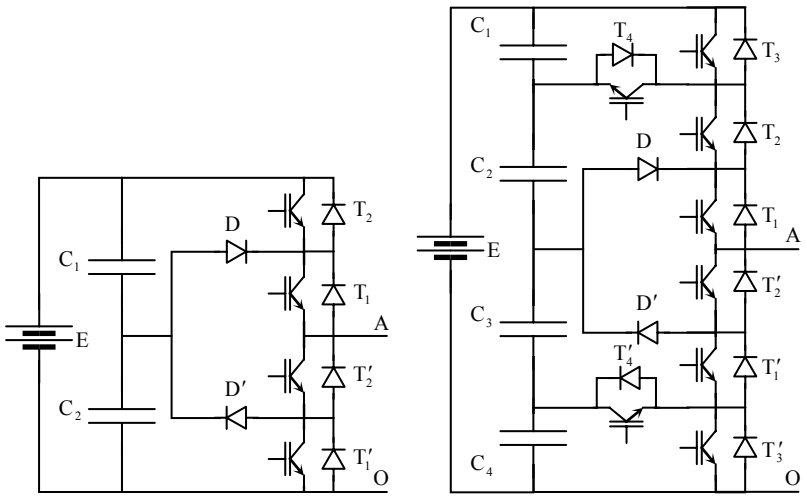


Figure 1.8: 3-level and 5-level Multi Point Clamped leg.

the number of voltage level is odd, the converters are called **Neutral Point Clamped** (**NPC**) because the neutral point is clamped. For the purpose of this book, MPC is used to univocally refer to the converters presented in Figure 1.8. In [31], a 4-level MPC converter is presented for UPS application showing a comparison with a 4-level diode-clamped. The 3-level leg is identical to a 3-level diode-clamped and Table 1.1 gives its modulation law. The two topologies can be told apart only when the output levels are more than three. As Figure 1.8 shows, the 5-level leg is completely different: in MPCs the voltages are clamped using couples switch-diode instead of using a simple diode.. Anyway, given a number of levels, the number of switches needed by MPC is the same needed by diode-clamped. The control of MPC leg is more complicated in the respect of other topologies. Even this kind of converter allows to find complementary couples of switches, as shown in Figure 1.8. The constrain so introduced is not physiologically necessary, but it is a simple way to simplify the control scheme and the switching table.

Switches state								
T_1	T_2	T_3	T_4	T_1'	T_2'	T_3'	T_4'	V_{AO}
1	1	1	0	0	0	0	1	E
1	1	0	1	0	0	1	0	$^{3E}/_{4}$
1	0	1	0	0	1	0	1	$^{E}/_{2}$
1	0	0	1	0	1	1	0	$^{E}/_{2}$
0	0	1	0	1	1	0	1	$^{E}/_{4}$
0	0	0	1	1	1	1	0	0

Table 1.7: 5-level MPC leg relationships between configurations and output voltages.

Furthermore, to avoid shortcut, T_3 and T_4 must be complementary controlled. The same must happens for T_3' and T_4'. Table 1.7 is a possible switching table for a 5-lrvel MPC leg; there is an intra-phase redundancy only for the middle level. Anyway, it is better to have T_4 turned on in order to limit the reverse voltage drop upon T_2. In this way, Table 1.7 looses one configuration.

The study of the modulation of this leg is quite complicated and introduces particular switching functions fully discussed in [32, 33]. Dependently on the switching table used, the maximum reverse voltage drop over the components changes and a preliminary analysis must be done to choose the suitable component. Moreover, the switches in the middle of the leg must carry twice the voltage of the others.

1.5.2. Characteristics

The main disadvantage of MPC is complex control they require. A specific hardware is necessary to implement the control: for instance a multilevel PWM comparator (analog or digital) can give the level required, but a proper switching table, implemented in a E^2PROM, must convert it in gate signals which define the leg configuration.

On the other hand, given a number of output levels, the number of components required for MPC is the lowest among all multilevel converters. This has a good repercussion on its production and maintenance costs.

Moreover, a comparison between MPC and diode-clamped can be done considering the path of the load current. Considering the scheme of 5-level converter presented in Figure 1.4, the load current has always to flow through four components among diodes and switches. In 5-level MPC of Figure 1.8 the greatest number of components through which the load current has to flow is three. There is a difference of one component which can be significant in the computation of losses and efficiency.

Regarding the portability, this converter is fully equivalent to a diode-clamped because the two topologies present the same DC bus structure.

1.6. Other topologies

1.6.1. Hybrid converter

All the multilevel converters presented in this paragraph are derived from the basic topologies. They are called hybrid topologies because they are a mongrel between two basic topologies or they are even composed by the same topology, but with different modulations of the stages.

Mixed-level hybrid multilevel cells [29] belong to this family. In this kind of converter, the H-bridge cells of cascaded leg are substituted by diode-clamped or flying-capacitor. Mixed-level hybrid multilevel cells converter is well suited for high-voltage high-power applications because of the reduction of required insulated sources in the respect of a cascade H-bridge with the same number of output levels. Figure 1.9a) shows a 9-level converter implemented using two diode-clamped cells.

When the cells have different DC bus voltages, the converter is called **asymmetric hybrid multilevel cells** [29]. In this way, the cells can also have different switching frequencies allowing the use of low frequency devices like GTO. A 5-level converter composed by one IGBTs and one GTOs H-bridge cell is presented in Figure 1.9b). Considering the leg presented, the lowest cell is modulated with a low frequency, but drives the greatest voltage. In this way, its output is kept constant for a long time in the period, switching only four times. The upper cell is used to compensate the output to obtain the reference. This structure works properly only if (1.19) is complied.

$$E_L = 2E_H . \qquad \textbf{(1.19)}$$

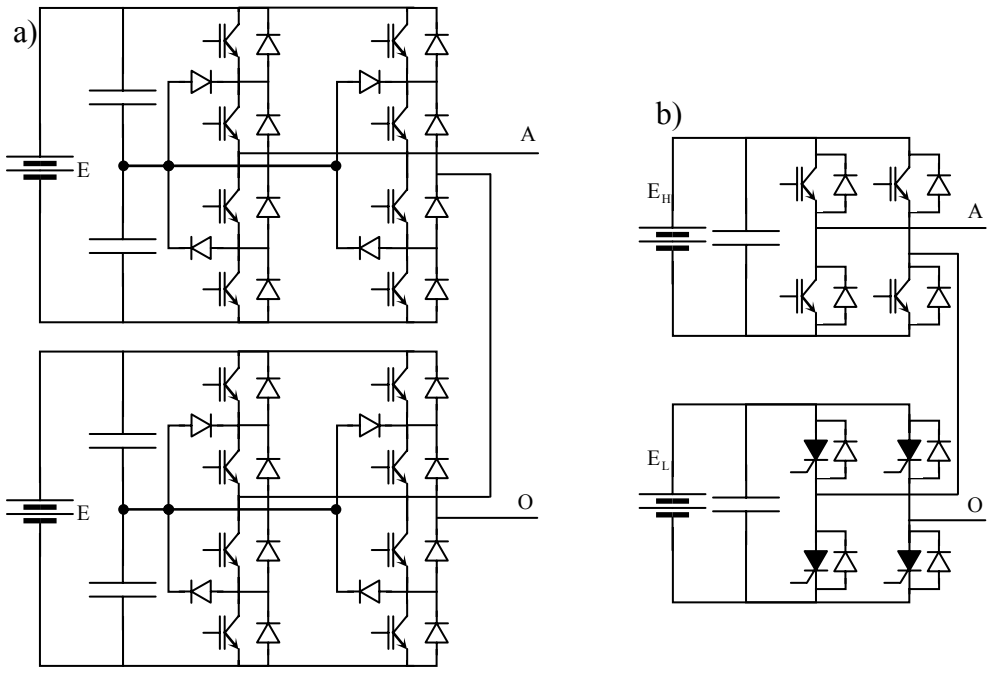


Figure 1.9: Hybrid converters; a) Mixed-level cells; b) Asymmetric cells.

1.6.2. Soft-switching converters

S**oft switched multilevel inverters** are presented in literature [29, 33-46] considering several different implementations. The aim of soft-switch inverters is to reduce the switching losses increasing the efficiency of multilevel converters. For the cascade inverter, because each inverter cell is a 2-level circuit, the implementation of soft-switching is not at all different from that of conventional 2-level inverters. For diode-clamped or flying-capacitor inverters, however, the choices of soft-switching circuit can be found with different circuit combination [34-40]. Although, zero-current switching is possible [41], most literature proposed zero-voltage-switching types including Auxiliary Resonant Commuted Pole (ARCP), coupled inductor with Zero-Voltage Transition (ZVT) and their combinations. Figure 1.10 shows an example of combining the ARCP and coupled-inductor ZVT techniques for a flying-capacitor 3-level inverter.

The auxiliary switches T_{x2}, T_{x3}, D_{x2} and D_{x3} are used to assist the inner main switches T_2 and T_3 to achieve soft-switching. With L_{r23} as coupled inductor, the bridge-type circuit formed by T_{x2}, T_{x3}, T_2 and T_3 forms a 2-level coupled-inductor ZVT. The basic principle of a 2-level ZVT can be found in [42-46] . For the outer main switches, the soft-switching relies on T_1, T_4, T_{x1}, T_{x4}, D_{x1} and D_{x4}, coupled inductor L_{r14} and split-capacitor pair C_2 to form an ARCP type soft-switching inverter. Detailed soft-switching circuit operation for inner and outer devices can be found in [34-36].

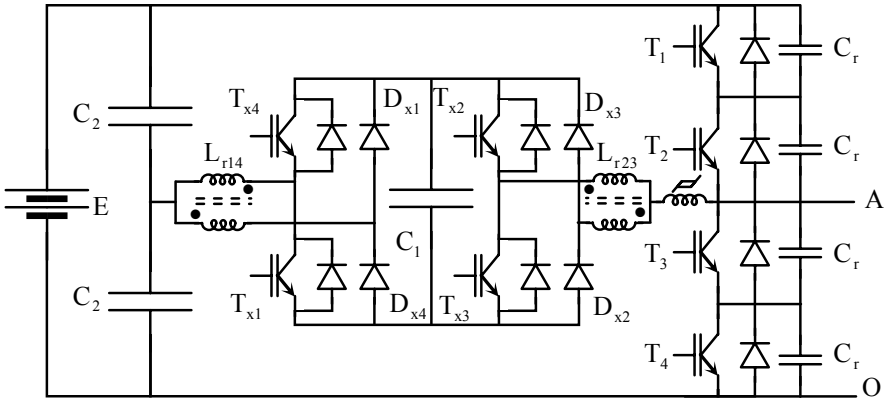


Figure 1.10: Zero-voltage-switching flying-capacitor inverter circuit.

1.6.3. Dual 2-level 3-phase cascade inverters

In Figure 1.11, another interesting multilevel topology is implemented cascading two standard 3-phase inverters with a six-wire open-end load in between [47-50]. It is equivalent to a 3-level 3-phase converter which will require three insulated sources if it is implemented as cascade H-bridge. In this way, the required insulated sources are only two. Moreover, the converter is composed by wide commercialized and very reliable parts which make its implementation quite easy. It is well suited for automotive applications in which splitting the batteries bank is possible.

A commercial DSP can easily drive this architecture which requires only six independent gate signals provided by microcontrollers designed for standard back-to-back applications.

Unfortunately, the number of levels can not be increased because there is no way to cascade more than two 3-phase inverters. Furthermore, the insulation between the two sources is critical for

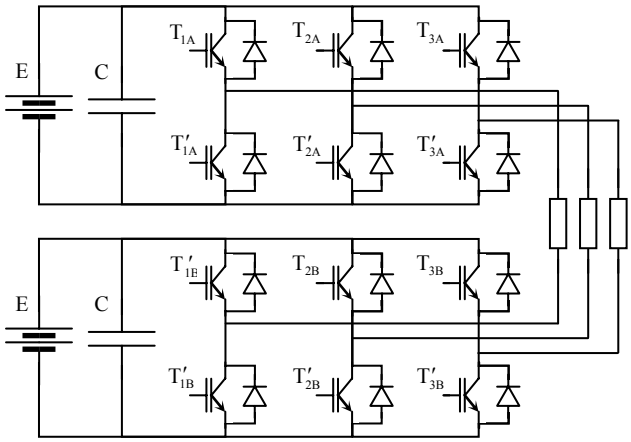


Figure 1.11: Dual 2-level 3-phase cascade converter.

the correct multilevel operation of the system because the common mode current flow must be avoided.

In [47] a solution to cut off one sources is presented. However four auxiliary switches are needed to break the common mode current path when the applied voltage has a common mode component; obviously, the control became more sophisticated. Another possibility to avoid common mode current flow, when the inverter is fed by only one source, is presented in [49]. The modulation applies only 3-phase voltages with zero common mode. In this way the available output vectors coincide with the vertices of a hexagon, like for standard 3-phase inverters, but they are doubled: there is an augmentation of the delivered power, but the quality of the output does not better.

Chapter 2

Multilevel modulation

2.1. Introduction

2.1.1. General considerations

In this chapter, several multilevel modulation strategies are discussed to introduce the reader in this charming world which is grooving more and more. The high number of switches composing a multilevel converter may lead to the conclusion that complex algorithms are necessary. Fortunately, all the modulation used for standard 2-level converters can be easily adapted to multilevel converters.

The modulation algorithm used to drive the multilevel converter has to be aimed to give the voltage level required for each leg; the translation in the proper switches configuration is done by other algorithms which can be hardware or software implemented. For instance, an inverter application using a MPC converter can be considered; furthermore it is supposed that the output voltage level is given by an analogue multilevel PWM (Section 2.4). The modulating signals can not directly drive the switches because they are not logically compatible, but they can be considered like a ROM address and used to get back stored configurations. In this way, all the modulation algorithm presented in this chapter can be used in all multilevel applications.

Actually, there are some modulation algorithms which produce outputs suited for particular multilevel topologies like the **multi-carrier based PWM** (Section 2.4) and the diode-clamped converters: in this case, the modulating signals are logically compatible with the required switches configuration which can be directly driven.

Moreover, the selection among redundant configuration is not a duty of the modulation algorithm. First of all, the aim of redundant configurations must be defined for the application. After determining the voltage applied to the load, the control system can choose among all the possible configurations the best one to accomplish the defined purpose. The aims of redundant configurations choice are many: it is possible to balance capacitors charges, to improve the switching pattern, to balance the current flowing through the switches and so on. Nevertheless redundant configurations by them selves represent the same state of the converter and their choice must be secondary in the respect of applying the correct output voltage, even when it is critical.

2.1.2. Modulations classification

There are several ways to classify modulation techniques; in [28] and [30] two possible ways are presented. Here, the way shown in [30] is adopted and graphically presented in Figure 2.1. The distinction between **multilevel modulation** and **multilevel control** has been done. Multilevel modulations are meant to produce an average output voltage proportional to the reference given by some external algorithm, while multilevel controls are meant to apply an output voltage calculated by them selves, like **Multilevel Direct Torque Control** (**MDTC**).

The switching frequency can subdivide multilevel modulations into three classes: **fundamental**, **mixed** and **high switching frequency**. Fundamental switching frequency modulations produce switch commutations at output fundamental frequency and can be aimed to cancel some particular low frequency harmonic. In this class there are **Space Vector Control** (**SVC**) and **selective harmonic elimination**. In **Space Vector Control** (**SVC**) the complex plain is divided in several hexagonal zones defining the proximity of the reference to the nearest generable vector which is definitely applied. In selective harmonic elimination the output is a staircase wave with steps duration optimized to cancel the specified harmonics; however the number of harmonics which can be eliminated at the same time is proportional to the number of converter levels. Mixed switching frequency modulations are those in which switches commutate at different frequency, like **hybrid multilevel modulation**, and are particularly suited for hybrid converters: different cells can easily commutate at different frequencies. **High switching frequency modulations** are the adaptation of standard PWM to multilevels and they are meant to switch at very high frequency, about 10 to 20 kHz. Among them, there are **Space Vector PWM** (**SVPWM**) and **Phase Shifted PWM** (**PSPWM**) and a subclass called **level shifted PWM**. **Phase Opposition** (**PO**), **Opposition Disposition** (**OD**) and **Alternate Opposition Disposition** (**AOD**) **modulation**s belong to this last level. SVPWM is the extension of the standard 2-level Space Vector Modulation to a greater number of levels. In PSPWM several phase-shifted references are used to generate the control pulses. PO, OD and AOD exploit only one reference waveform which is compared with carries covering all the range of reference variation. The number of used carriers is equal to $n-1$.

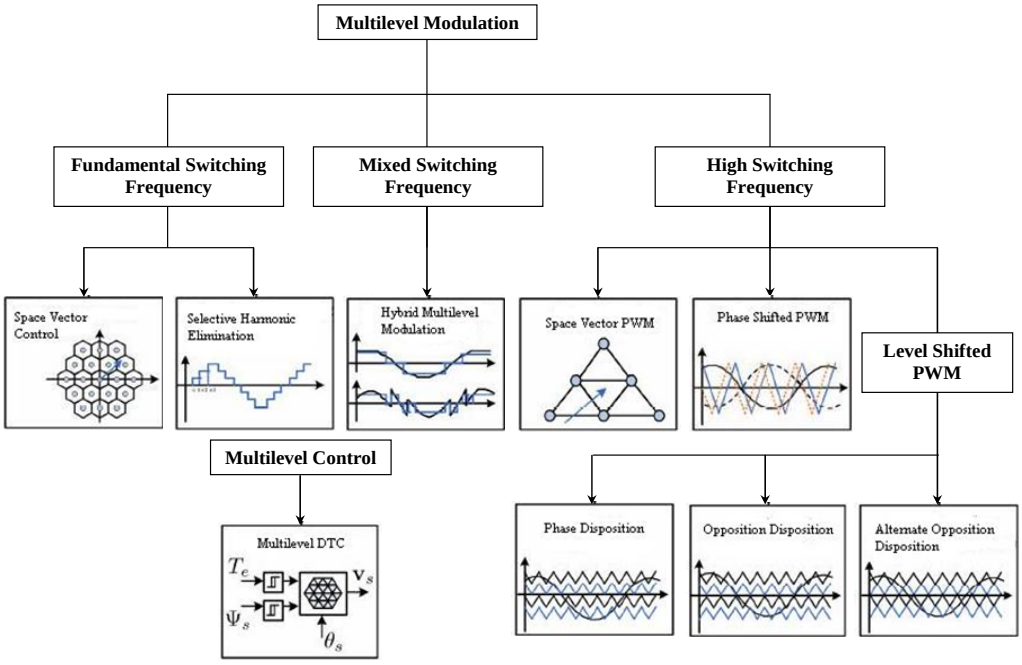


Figure 2.1: Classification tree for multilevel modulations.

2.2. Fundamental switching frequency modulations

2.2.1. Space Vector Control (SVC)

SVC, as the name suggests, is a vector modulation technique. In the complex plain, the possible vectors can be seen as vertices of a triangular grid. In Figure 2.2a) a single element of this grid, an equilateral triangle, is highlighted. Its medians drown in the figure posses a particular property: they subdivide the triangle in three zones defining the sets of points which are the nearest to one of the vertices. Drawing the medians of all the triangles of the grid creates hexagonal meshes centred in each vertex and determines the sets of points closest to each generable vector.

In Figure 2.2b) the hexagonal meshes of a 5-level converter are shown together with all the equilateral triangles of the grid and a generic vector $\bar{v}$. Surely the vector $\bar{v}$ will lay in one of the hexagonal regions determining, in this way, its closest generable vector which has to be applied to the output.

In a period of time, as in PWM cycle, SVC does not produce an output vector with the same DC value of the reference. This determines an error which is not compensated, but the aim of the modulation is to choose among all the generable vectors the one which minimizes it. If the reference is a vector rotating at a constant angular speed the output voltage waveform will be a symmetric staircase.

This kind of modulation is particularly suited for multilevel converter with a high number of levels because the error made is getting smaller and smaller increasing the levels. So it is unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference due to the high density of vectors the multilevel converter present when their number of levels is quite high. Obviously, SVC is definitely unreliable when it applied to a standard 2-level or even to a 3-level inverter because the ripple on the output voltage becomes unacceptable.

Moreover, the switching frequency of each switch is equal to the fundamental, meaning reduced commutation losses and the possibility to apply this modulation even to slow devices like GTO for high power applications.

The performances of this modulation are compared in [52] with a PWM technique asserting the good behaviour in terms of voltage THD using a 11-level three-phase inverter composed by five cascaded H-bridge for each leg. As presented in [53], SVC can be used to control even current source converters using current vectors instead of voltage ones.

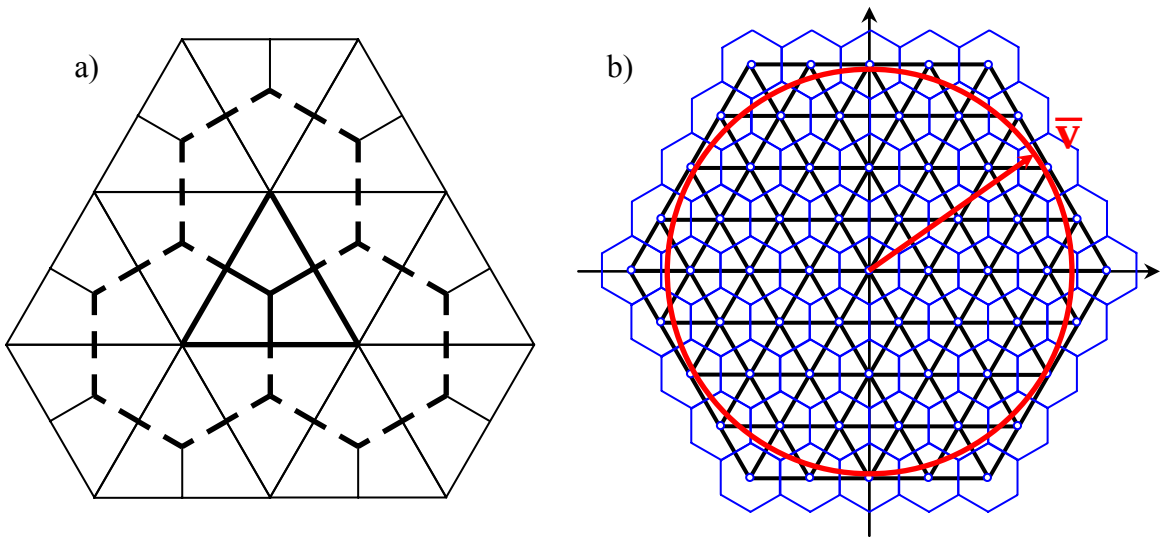


Figure 2.2: SVC principle for a 5-level converter: a) Proximity zones definition; b) Vector choice.

2.2.2. Selective harmonic elimination

In Figure 2.3 the output waveform of a 7-level selective harmonic elimination is shown. It is possible to define three switching angles in correspondence of the rising edges which describe univocally the wave due to its symmetrical properties. By Applying Fourier series analysis, the amplitude of any odd m^{th} harmonic of the stepped waveform can be expressed as (2.1), whereas the amplitudes of all even harmonics are zero.

$$h_m = \frac{4}{m\pi}\sum_{k=1}^{3}\left[V_k \cos(m\alpha_k)\right]. \qquad \textbf{(2.1)}$$

In (2.1), V_k is the k^{th} level of DC voltage and α_k is the k^{th} switching angle. Considering a generic n-level converter, a generalization of (2.1) can be done and it is expressed in (2.2) with the same meaning of the symbols.

$$h_m = \frac{4}{m\pi}\sum_{k=1}^{n}\left[V_k \cos(m\alpha_k)\right]. \qquad \textbf{(2.2)}$$

Obviously, all the switching angles must satisfy $\alpha_1 < \alpha_2 < \alpha_3 < \ldots < \alpha_n < \pi/2$.

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $n-1$ harmonic contents can be removed from the voltage waveform. The selection of the switching angles is usually aimed to remove the most important low-frequency harmonics because the high frequency harmonics can be readily eliminated by an additional filter circuit.

Accordingly to (2.2), to keep the number of eliminated harmonics constant, all switching angles must be less than $\frac{\pi}{2}$ because, if this condition is not satisfied, the proposed scheme will no longer exist. This is a heavy constrain upon the range of variation of the modulation index and it is getting more and more binding as the number of converters levels increases. For instance, in a 7-level equally-stepped waveform, the modulation index allowing the elimination of three harmonics can only vary between 0.5 and 1.05. To adopt the proposed scheme when the modulation indexes is above 0.5, it is necessary to reduce the number of removed harmonics, i.e. the levels used in the modulation are reduced from seven to five and so the switching angles will become only two. Consequently, the output THD will worsen.

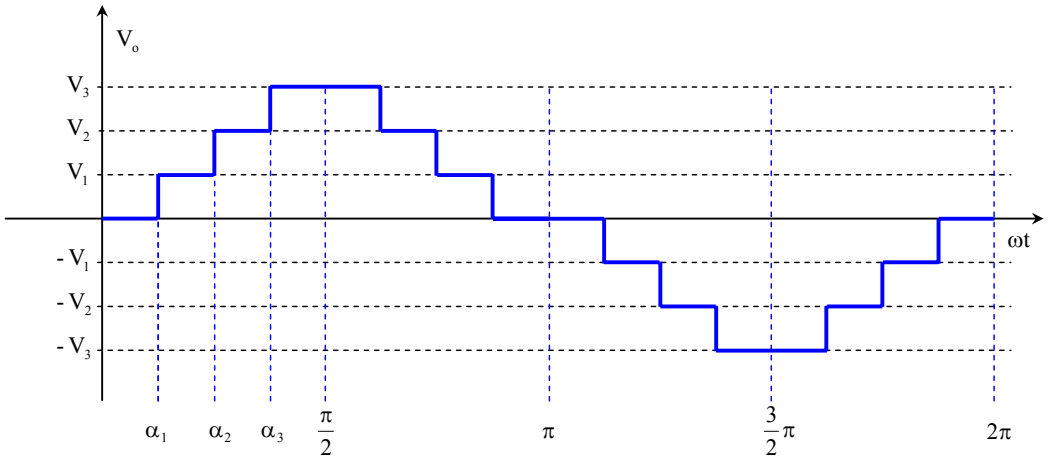


Figure 2.3: Selective harmonic elimination output waveform of a 7-level converter.

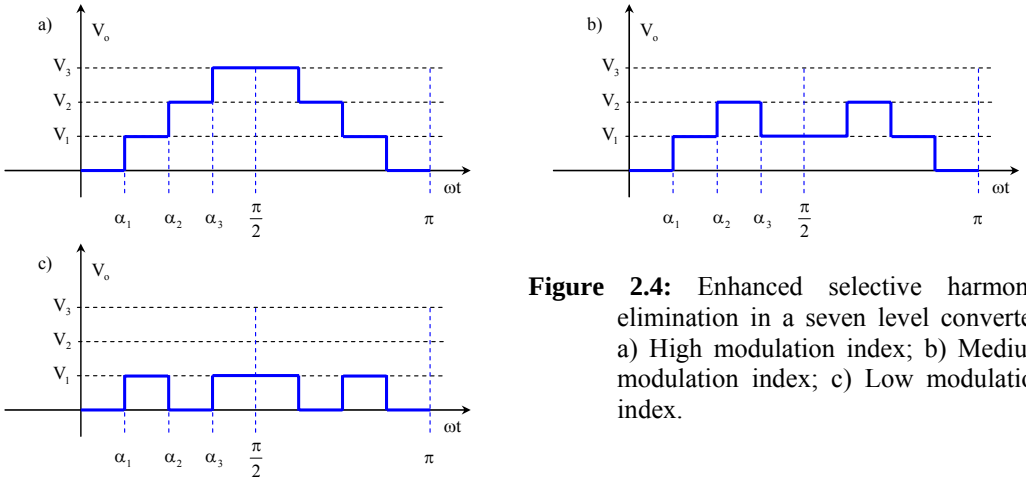


Figure 2.4: Enhanced selective harmonic elimination in a seven level converter. a) High modulation index; b) Medium modulation index; c) Low modulation index.

In [54, 55] is presented a generalization of selective harmonic elimination, a way to achieve a wide range of modulation index with minimized THD of the synthesized waveforms. The enhanced method for a 7-level converter is illustrated in Figure 2.4 in which the positive half-cycles are shown with different modulation indexes. In this case the range of modulation index can be subdivided in three zones, such as high, medium and low. An output waveform with high modulation index is shown in Figure 2.4a). Whenever α_3 is greater than $\frac{\pi}{2}$, this waveform no longer exists. Therefore, the output waveform must eliminate one level without loosing degree of freedom: it is done as Figure 2.4b) shows for middle modulation indexes. Something similar will happen even for low modulation indexes, i.e. the output waveform looses another level when the computed switching angles are greater than $\frac{\pi}{2}$, as Figure 2.4c) illustrates.

In general, a stepped waveform, which comprises n switching angles, can be divided into n modulation index zones. By using this technique, low switching frequencies and minimized harmonic contents can be achieved even at low modulation indexes. (2.3) is a generalized expression for harmonic content for multilevel stepped waveform.

$$h_m = \frac{4}{m\pi}\left[\pm V_1\cos(m\alpha_1) \pm V_2\cos(m\alpha_2) \pm \ldots \pm V_n\cos(m\alpha_n)\right]. \qquad \textbf{(2.3)}$$

In (2.3) the positive sign implies the rising edge and the negative sign implies the falling edge of the waveform in correspondence of the considered switching angle.

2.3. Mixed switching frequency modulations

2.3.1. Hybrid multilevel modulation

Hybrid multilevel converters may need different modulation strategies for the different stages composing them. For instance, a cascade H-bridge converter composed by one GTOs stage and one IGBTs stage may require two different switching frequencies, one for high-speed and one for low-speed devices. In this way, the output waveform, being the sum of the single stage outputs, presents the two frequencies in its harmonic content. In [56, 57] a mixed frequency modulation is presented for the 5-level hybrid cascade H-bridge converter shown in Figure 2.5a). It is constituted of one IGBTs cell and one GTOs cell cascaded. The GTOs are rated for twice the voltage of IGBTs , so the total maximum voltage is $3E$ where E is the DC bus voltage of the IGBTs cell. In this way the GTOs stage can supply up to $2E$.

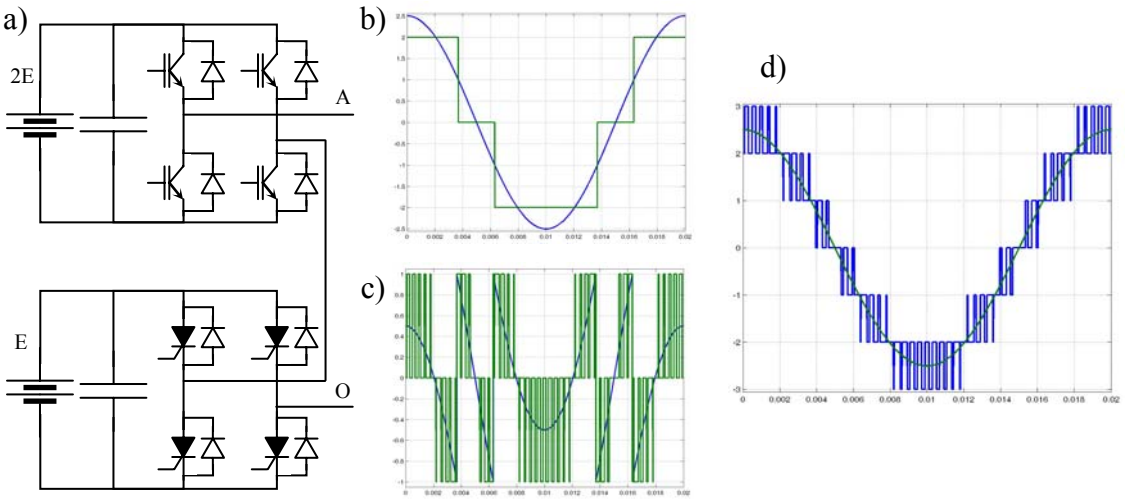


Figure 2.5: Hybrid modulation. a) hybrid converter; b) Low-frequency stage reference and output voltages; c) High-frequency stage reference and output voltages; d) Total reference and output voltages.

Figure 2.5b) and c) show, respectively, the reference and the output waveforms of the low-frequency and the high-frequency stages in per unit referred to E. The low-frequency stage is modulated comparing the total reference with two fixed levels: +1 and -1 in per unit as depicted in Figure 2.6a). When the total reference V_r^* is greater than 1 the GTOs bridge produces the maximum voltage, i.e. $2E$. When the total reference is between 1 and -1, the GTOs bridge produces zero voltage. Finally, when the reference is lower than -1, the GTO output is $-2E$. In this way the stepped output waveform shown in Figure 2.5d) is obtained.

The high-frequency stage must compensate the error between the desired and the lo-frequency output. The high-frequency reference V_{rl}^* is created subtracting the output if the low-frequency stage from the total reference as shown in the scheme of Figure 2.6c). The reference V_{rl}^* is the input into a 3-level modulator shown in Figure 2.6b). The high-frequency reference and output are shown in Figure 2.5c).

The sum of low-frequency and high-frequency outputs is the total output V_o shown in Figure 2.5d) together to the total reference.

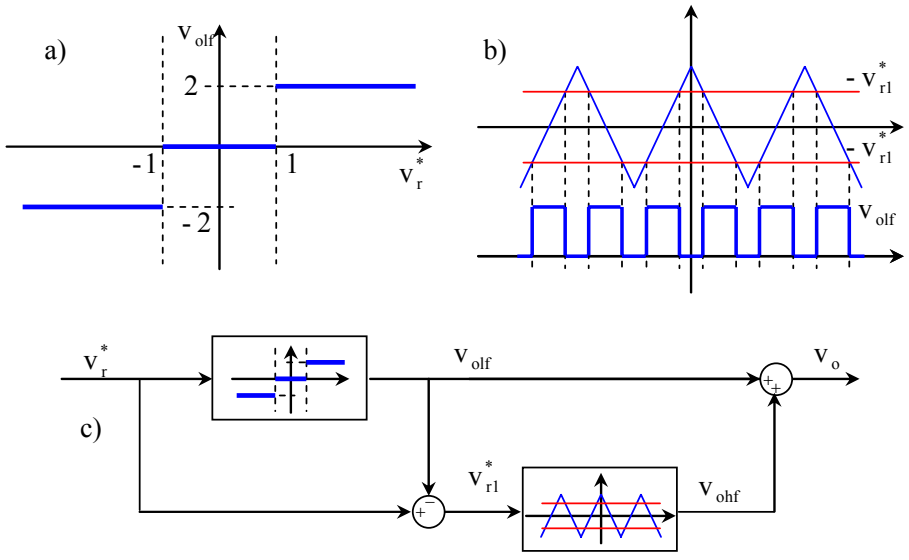


Figure 2.6: Hybrid modulation. a) Low-frequency modulation; b) High-frequency modulation; c) Total output voltage reconstruction.

This method is useful when the ratio between the DC bus voltages of the different stages is well defined. In the present application, the correct ratio is 1:2 because any total reference between 3 and -3 can be continuously generated. Indeed, if the IGBTs bridge DC bus voltage was $0.5E$ and the GTOs bridge dc voltage was $2E$, it would be impossible to generate a reference equal to E.

The advantage of this modulation technique is the high power it allows to drive exploiting different kinds of devices. Moreover the output waveform presents a quite good THD even if it is composed by low-frequency harmonics.

2.4. High switching frequency modulations

2.4.1. Space Vector PWM (SVPWM)

The high-frequency modulations involve the principle to generate an output voltage with the same mean value of the reference in a fixed period of time called **cycle**. Usually, the period is about 66.6 – 50 μs because the correspondent switching frequency (15 – 20 kHz) is suitable for the commercial devices and is so high that human hearing can not hear it.

The Space Vector PWM generate the output voltage as the weighted mean of the three vectors adjacent to the reference in the d-q plane. The weights, called **duty-cycles**, must be determined to obtain the desired output. In [58, 59] a way to implement the SVPWM is presented. In [58, 59] the modulation of a 7-level converter is studied. For the purpose of this dissertation, the same technique is proposed for a 5-level converter to be in agreement with the other paragraphs which are inherent to 5-level architectures.

In Figure 2.7a) the space vectors generated by a 5-level converter are shown. The reference space vector is defined by (2.4), where v_a, v_b and v_c are the phase voltages of the converter.

$$\bar{v} = v_a e^{j0} + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}. \qquad \textbf{(2.4)}$$

The vectors can be subdivided into six major triangular sectors (I to VI) and the details of sector I are given in Figure 2.7b). The coordinates of the vector $\bar{v}$ in the d-q plane are given by (2.5).

$$\begin{cases} v_d = v_a - \frac{1}{2}(v_b + v_c) \\ v_q = \frac{\sqrt{3}}{2}(v_b - v_c) \end{cases}. \qquad \textbf{(2.5)}$$

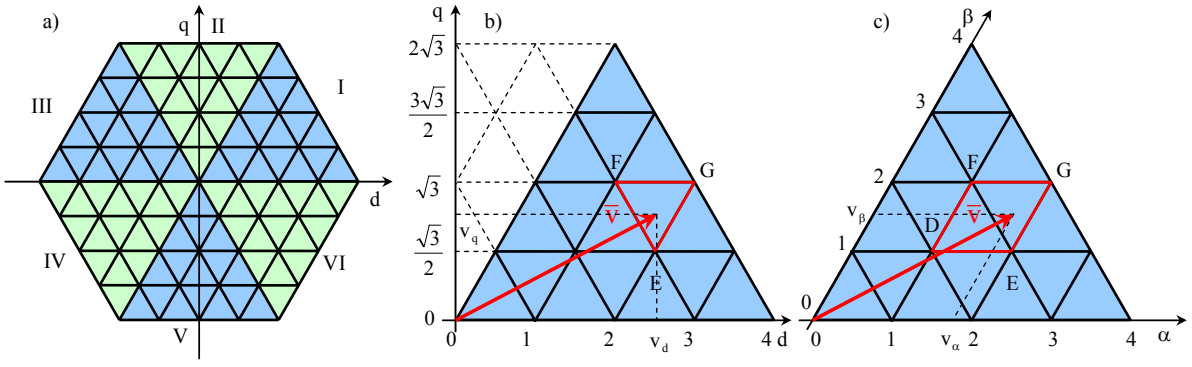


Figure 2.7: Space Vector PWM. a) Voltage vectors of 5-level converter; b) Space vector in the d-q plane; c) Space vectors in the 60° coordinate system.

The coordinate of all the space vectors of sector I can be seen in Figure 2.7b), assuming a unity DC supply voltage. The optimum solution to generate the reference is to apply the three nearest vectors; for instance, to generate the vector $\bar{v}$ of Figure 2.7b) the vectors determining the triangle EFG must be applied.

$$\begin{cases} \bar{v}_E = \frac{5}{2} + j\frac{\sqrt{3}}{2} \\ \bar{v}_F = 2 + j\sqrt{3} \\ \bar{v}_G = 3 + j\sqrt{3} \end{cases} . \qquad \textbf{(2.6)}$$

The vector expressions given in (2.6) uses Cartesian coordinates and the way to manage Cartesian coordinate system to find reference position and duty-cycles will be show in (Section 5.2.2); now the problem will be faced using 60° coordinate system as shown in Figure 2.7c). The relationship between Cartesian and 60° coordinate system is given by (2.7), where $v = \sqrt{v_d^2 + v_q^2}$ and $\theta = \text{atan}\left(\frac{v_q}{v_d}\right)$ are the polar representation of the generic vector $\bar{v} = v_d + jv_q$, v_α and v_β are the coordinates in the new system.

$$\begin{cases} v_\alpha = v\left(\cos\theta - \frac{\sin\theta}{\sqrt{3}}\right) \\ v_\beta = \frac{2v}{\sqrt{3}}\sin\theta \end{cases} . \qquad \textbf{(2.7)}$$

The 60° coordinate system require the determination of the sector in which the vector lies before applying the transformation from Cartesian system, but it definitely simplifies the assessment of the triangle which includes the reference. Indeed, supposing that the reference vector is lying in triangle EFG like in Figure 2.7c), the coordinate of the vector $\bar{v}_D$ will be used to determine its location. In 60° reference these coordinates are:

$$\begin{cases} v_{D\alpha} = \lfloor v_\alpha \rfloor \\ v_{D\beta} = \lfloor v_\beta \rfloor \end{cases} . \qquad \textbf{(2.8)}$$

The square brackets in (2.8) substitute round toward zero function, i.e. applying this function to the real number 1.75, it will be $\lfloor 1.75 \rfloor = 1$.

The coordinates of $\bar{v}_D$ indicate the reference vector lies in one of the two triangles highlighted in Figure 2.7c), DEF or EFG. In the respect of $\bar{v}_D$, the coordinates of the other vertices ($\bar{v}_E$, $\bar{v}_F$ and $\bar{v}_G$) are given by (2.9).

$$\begin{cases} (v_{E\alpha}, v_{E\beta}) = (v_{D\alpha}, v_{D\beta} + 1) \\ (v_{F\alpha}, v_{F\beta}) = (v_{D\alpha} + 1, v_{D\beta}) \\ (v_{G\alpha}, v_{G\beta}) = (v_{D\alpha} + 1, v_{D\beta} + 1) \end{cases} . \qquad \textbf{(2.9)}$$

To further discriminate whether the reference vector is in triangle DEF or in EFG, the following criterion can be used:

$$\begin{cases} \overline{v} \in \text{DEF} & \leftrightarrow & \left(v_\alpha + v_\beta\right) \geq \left(v_{E\alpha} + v_{E\beta}\right) \\ \overline{v} \in \text{EFG} & \leftrightarrow & \left(v_\alpha + v_\beta\right) < \left(v_{E\alpha} + v_{E\beta}\right) \end{cases}. \quad \textbf{(2.10)}$$

After the determination of the vectors involved in the reconstruction of the output voltage $\overline{v}$, their duty-cycles must be calculated using the volt-second balancing principle shown in (2.11).

$$\begin{cases} \overline{v} = \delta_E \overline{v}_E + \delta_F \overline{v}_F + \delta_G \overline{v}_G \\ 1 = \delta_E + \delta_F + \delta_G \end{cases}. \quad \textbf{(2.11)}$$

In (2.11), $\overline{v}$ is the reference voltage vector, $\overline{v}_E$, $\overline{v}_F$ and $\overline{v}_G$ are the voltage defining the vertices of triangle EFG and δ_E, δ_F and δ_G are their duty-cycles. The first of (2.11) can be decomposed into α-axis and β-axis yielding to (2.12).

$$\begin{cases} v_\alpha = \delta_E v_{E\alpha} + \delta_F v_{F\alpha} + \delta_G v_{G\alpha} \\ v_\beta = \delta_E v_{E\beta} + \delta_F v_{F\beta} + \delta_G v_{G\beta} \\ 1 = \delta_E + \delta_F + \delta_G \end{cases}. \quad \textbf{(2.12)}$$

Substituting (2.9) in (2.12) and solving the system to determine δ_E, δ_F and δ_G, the duty-cycles are determined.

$$\begin{cases} \delta_E = \left(v_{D\alpha} - v_\alpha\right) + 1 \\ \delta_F = \left(v_{D\beta} - v_\beta\right) + 1 \\ \delta_G = 1 - \left(\delta_E + \delta_F\right) \end{cases}. \quad \textbf{(2.13)}$$

Similarly, if the reference vector lied in triangle DEF, the duty-cycles δ_D, δ_E and δ_F, for vectors $\overline{v}_D$, $\overline{v}_E$ and $\overline{v}_F$, would be given by

$$\begin{cases} \delta_E = v_\beta - v_{D\beta} \\ \delta_F = v_\alpha - v_{D\alpha} \\ \delta_D = 1 - \left(\delta_E + \delta_F\right) \end{cases}. \quad \textbf{(2.14)}$$

Using only the last two sets of equations it is possible to determine duty-cycles for the vectors involved in the generation of the output. The equations are definitely simple and their implementation on a digital control system follows to be easy. Moreover, the presented algorithm does not depend on the number of converter levels.

2.4.2. Phase shifted PWM (PSPWM)

Phase shift PWM [57, 60, 61] involves the same principle of standard 2-level PWM to gate the switches using the comparison between two signals, reference and carrier, but exploit more than one

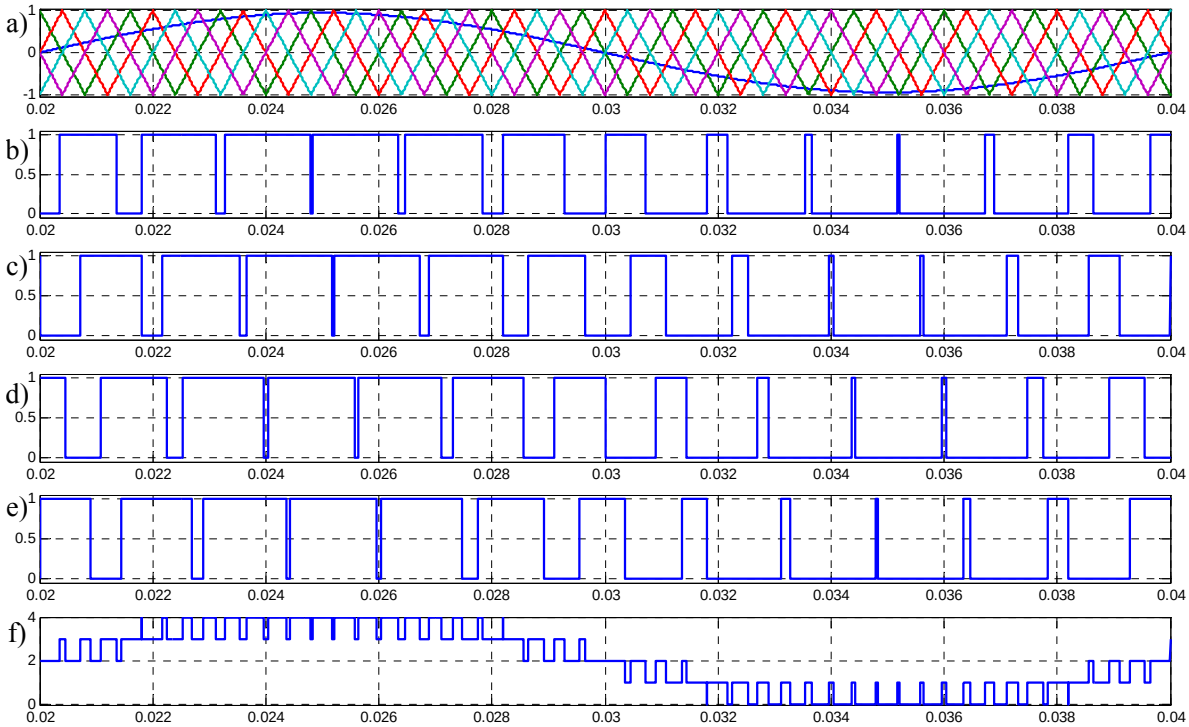


Figure 2.8: Phase Shift PWM waveforms for 5-level converters in per unit. a) Carriers and reference; b) - e) Comparison signals; f) Output waveform.

carrier to generate the driving signals. The required carriers, all with the same amplitude and frequency, depend on the number of levels: in a converter with n levels**,** $n-1$ carriers are necessary. As the name suggests, the carriers have to be displaced, shifting their phases. The phase shift can be done choosing any delay, but the minimum harmonic distortion of the output is achieved using the delay Δ given by (2.15), where T_S is the switching period.

$$\Delta = \frac{T_S}{n-1}. \qquad \textbf{(2.15)}$$

Figure 2.8a) shows the four carriers needed to drive a 5-level converter shifted with a delay equal to a quarter of T_S. In the presented case, the reference is common for all the carriers even if there are some versions of PSPWM which involve more references [57, 61]. The comparison signals between each carrier and the reference are shown in Figure 2.8b) – e).

Figure 2.8f) shows the output waveform generated as sum of all the comparison signals. In this way, the output switching frequencies results to be higher than carrier one. (2.16) gives, for a n-level converter, the relationship between output and carrier switching frequencies, f_{out} and f_{car} respectively.

$$f_{out} = (n-1)f_{car}. \qquad \textbf{(2.16)}$$

Moreover, due to the particular disposition of the carriers, the output is generated switching among the two levels nearest to the reference. This is the reason why the chosen delay minimizes output harmonic content.

This kind of modulation is particularly suited for cascade H-bridge because the comparison signals can directly drive converter switches [57, 61], while some hardware is necessary in between for other topologies.

2.4.3. Level shifted PWM (LSPWM)

Level Shifted PWMs [57, 60-64] use more carriers, with the same amplitude and frequency, but translated in level as pictures in Figure 2.9 show for a 5-level converter. The number of carriers needed to generate the driving signals for a n-level converter is the same as PSPWM, that is $n-1$. There are three major kinds of LSPWMs depending on how the carriers are disposed. The most evident method, depicted in Figure 2.9a), is called **Phase Disposition** (**PD**).

The interval of possible voltage reference values is subdivided into one zone for each carrier which modulates the output only when the reference belong to its zone. When the reference does not belong to a zone, associated carrier comparison output is fixed to high or low level: it is high when the reference is above the carrier, vice versa it is low when the reference is under the carrier. The comparison output, obtained in this way, and its negation can directly drive a couple of switches in diode-clamped. The sum of all the comparison outputs, shown in Figure 2.9b), is a signal proportional to the instantaneous required output level.

The **Phase Opposition Disposition** (**POD**) uses the same translation of carriers as PD, but the carrier associated to negative levels are in opposition of phase as depicted in Figure 2.9c). Figure 2.9d) shows the signal obtained as sum of comparison output signals. Even in POD this signals is proportional to the level required.

The **Alternative Phase Opposition Disposition** (**APOD**), depicted in Figure 2.9e), has the carriers alternatively in phase or in opposition. Figure 2.9f) shows the output required by this kind of modulation.

As it can be seen comparing Figure 2.9b), d) and f), the difference among these three LSPWMs is related to the symmetry of the output they produce. Indeed, POA and APOD have odd symmetry, while PD positive half-wave can be mirrored and translated to coincide with the negative one.

Each switch commutates at the carrier frequency only when the reference belong to the zone related. Otherwise the switch is hold, but the converter is still commutating. This means that the switching frequency of the converter is equal to the carrier frequency (f_{car}), but the average switching frequency of the single switch (f_{sw}) is lower and, for a n-level converter, it is given by (2.17).

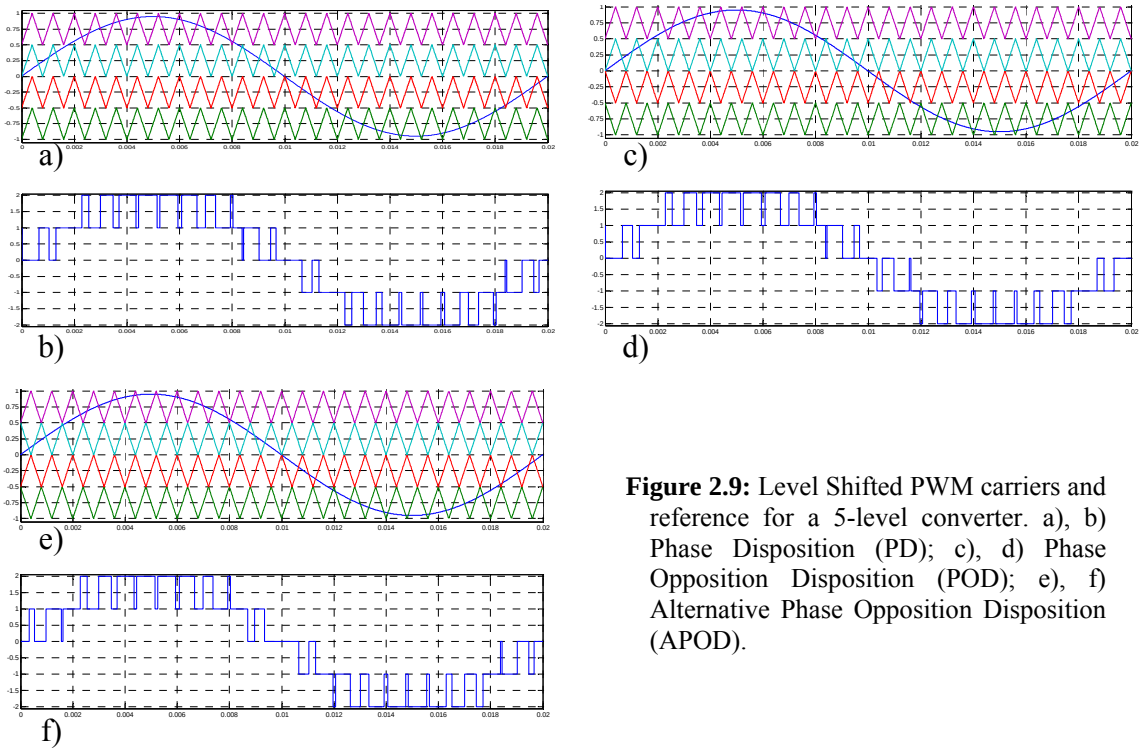


Figure 2.9: Level Shifted PWM carriers and reference for a 5-level converter. a), b) Phase Disposition (PD); c), d) Phase Opposition Disposition (POD); e), f) Alternative Phase Opposition Disposition (APOD).

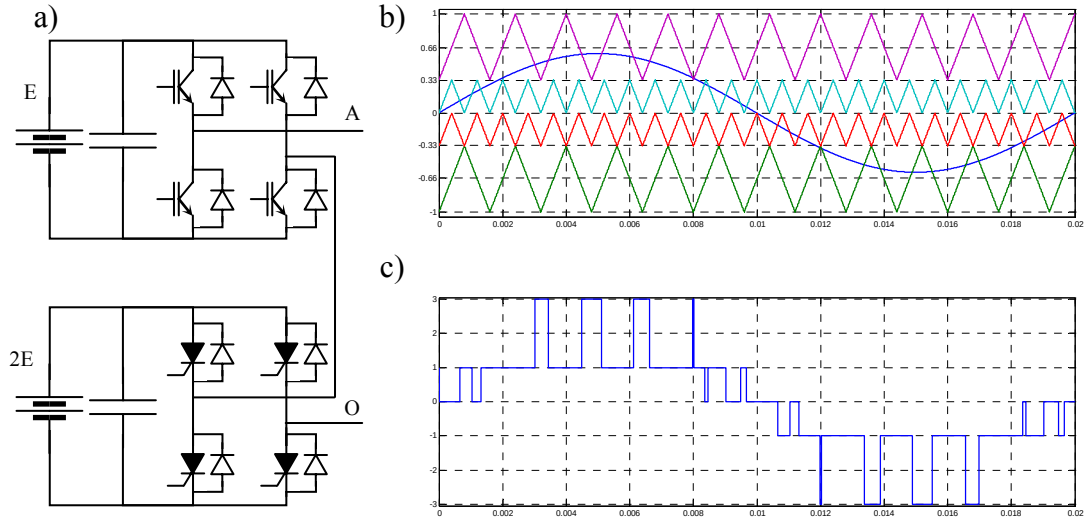


Figure 2.10: Hybrid cascaded H-bridge using PD with different carrier frequencies. a) Converter topology; b) Carriers and reference; c) Output.

$$f_{sw} = \frac{f_{car}}{(n-1)}. \qquad \textbf{(2.17)}$$

Anyway, the carrier frequency has to be suited for the characteristics of the chosen switch, so LSPWMs do not really allow to increase the output frequency as PSPWM does.

In some application like hybrid multilevels (Figure 2.10a)), the converter can be implemented using different types of switch, with different performances regarding maximum born voltage and switching frequency [61]. In theses cases the carriers can have different frequencies and amplitudes as shown in Figure 2.10b). The carriers with high frequency and low amplitude are associated to the fast switches, while the other carriers drive the slow ones. In Figure 2.10c), the output is shown and the different amplitudes and frequencies, attributable to the different carries for the two bridges, are evident.

2.5. Multilevel Direct Torque Control (MDTC)

2.5.1. Direct Torque Control Principle

To conclude the chapter about the modulation strategies Multilevel Direct Torque Control is presented. All the modulations described above can work without knowing the nature of the system, that is it is not necessary to know the property of the load: when the reference is determined, the modulation algorithm can apply it. In DTC the reference to be applied is directly calculated from the equation of the load, usually an **Induction Motor** (**IM**), but even a **Permanent Magnet Synchronous Machine** (**PMSM**). In [65-68] there is a good explanation of DTC principles related to a standard 3-phase 2-level **Voltage Source Inverter** (**VSI**). In the following, a short description of DTC is presented, just to introduce to its extension to multilevel VSI.

Considering Park transform of IM equations, it is possible to write (2.18), where $\bar{\varphi}_s$ is the stator flux, $\bar{v}_s$, $\bar{i}_s$ and R_s are the stator voltage, current and resistance respectively.

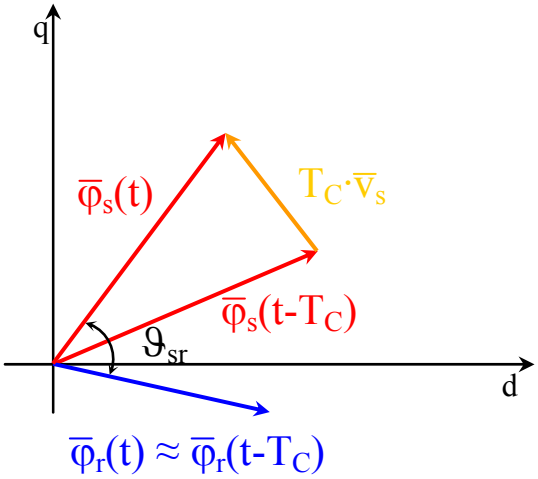


Figure 2.11: DTC Principles: vector representation of the stator an rotor fluxes during a sample interval T_C.

$$\frac{d\overline{\varphi}_s}{dt} = \overline{v}_s - R_s \overline{i}_s . \qquad \textbf{(2.18)}$$

Ignoring the contribution of the current, which can be considered small in the respect of the stator voltage, the variation of stator flux can be ascribed all to the voltage applied. So, a proportional relationship between flux variation and voltage in a given cycle T_C can be found by discretizing (2.18).

$$\Delta\overline{\varphi}_s \approx T_C \overline{v}_s . \qquad \textbf{(2.19)}$$

Analyzing the equation binding the stator and rotor fluxes (φ_s and φ_r) to the torque (T_e), it is possible to find that an augmentation of the angle between fluxes (ϑ_{sr}) means an augmentation of torque, as (2.20) shows, where M, σL_s and p are the mutual inductance, the leakage inductance and number of poles respectively.

$$T_e = \frac{3}{2}\frac{p}{2}\frac{M}{(\sigma L_s)^2}\varphi_s \varphi_r \sin(\vartheta_{sr}). \qquad \textbf{(2.20)}$$

From low pass filter relationship between stator and rotor fluxes it can be assumed that a fast variation of the stator flux angular speed will reflect in an increment of the angle ϑ_{sr}, as Figure 2.11 schematically shows. So, imposing a particular stator voltage, it is possible to control either the stator flux amplitude and the torque. The vector $\Delta\overline{\varphi}_s \approx T_C \overline{v}_s$ can be decomposed in the component parallel and perpendicular to the stator flux; the parallel component modifies the stator flux amplitude while the perpendicular component controls the torque.

2.5.2. Application of DTC to multilevels

The DTC algorithm can even be applied to multilevel VSI exploiting more than the eight vectors available in standard DTC. Lots of algorithms have been proposed to extend DTC concept to multilevel converters [69-71]. The differences among the algorithms concern several aspects of the system, like the voltage selection schemes, the exploitation of the topology implemented, the control regulators, etc.

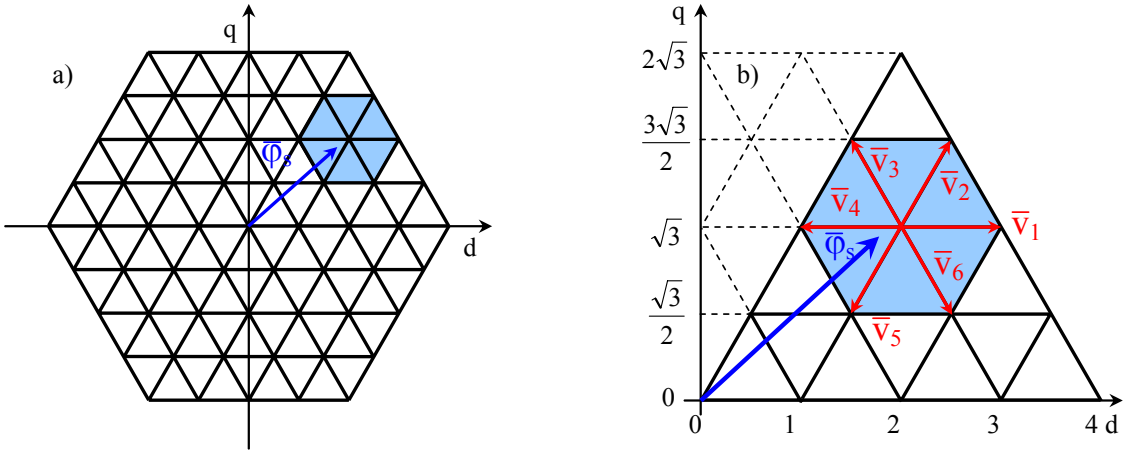


Figure 2.12: Multilevel DTC. a) Vectors generated by a 5-level converter and reference; b) Zoom of the area near to the reference and the six vectors which can be applied.

For the purpose of this dissertation, the implementation given in [71] is shortly examined applying it to a 5-level converter, to be in agreement with the previous descriptions. In Figure 2.12a) all the possible vectors generable by a 5-level converter are depicted as the vertices of the triangular grid. In particular the position of the stator flux is assumed to be given by the vector $\overline{\varphi}_s$ which is lying in the highlighted hexagon. The control strategy must choose among the vectors nearest to flux the one which cancels torque and flux errors. These vectors are drawn in red in Figure 2.12b) and they were given a name: $\overline{v}_1$, $\overline{v}_2$, $\overline{v}_3$, $\overline{v}_4$, $\overline{v}_5$ and $\overline{v}_6$. Accordingly to standard DTC technique, the vector minimizing torque contribution (i.e. $\overline{v}_2$ and $\overline{v}_5$) are not used.

The other four vectors can be used exploiting their properties above torque and flux. The vector $\overline{v}_1$ is used to increase the flux and to decrease the torque; applying $\overline{v}_3$ both flux and torque increase; $\overline{v}_4$ has opposite effects than $\overline{v}_1$ and $\overline{v}_6$ is used when both flux and torque have to be decreased.

The DTC principle is very simple and lead to a fast executing algorithm, even if the determination of flux position inside each triangle can be a very hard job for the microcontroller due to the big number of calculation needed to manage all the triangular zones the grid created.

In Figure 2.13 is shown the control scheme adopted in [37]. The scheme is aimed to control the switching frequency calculating the delay in the application of the new configuration which will

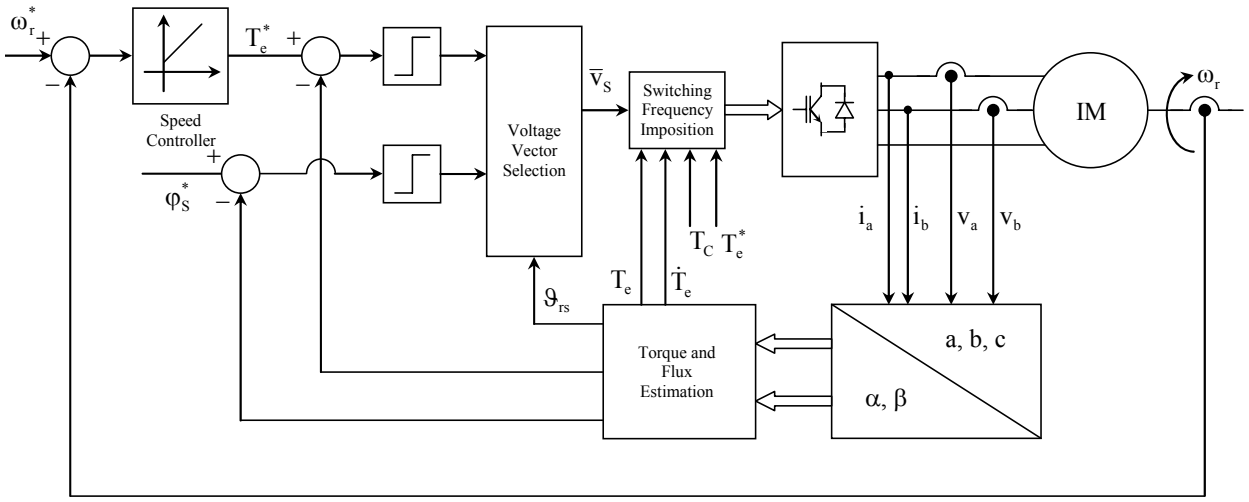


Figure 2.13: Multilevel DTC control scheme with switching frequency imposition.

ensure zero torque error in the following sampling period imposing one commutation per cycle. The joint-phase and the intra-phase redundancies can ensure the control of correct operation of the system, for instance, keeping constant the capacitor voltage. Obviously, there are several ways to use the great number of vectors and redundant configurations multilevel converters can generate.

Chapter 3

Dual 2-level inverter

3.1. Introduction

3.1.1. Topology description

In Section 1.6.3 the dual 2-level inverter has been shortly introduced presenting the topology shown in Figure 3.1. This topology consists of two standard 3-phase 2-level inverters with AC sides connected to the same 3-phase open-end 6-wire load and the DC sides connected to two different voltage sources. It could be said that the dual 2-level inverter is a derivation of the 3-level cascade H-bridge like standard 3-phase inverter is for the single-phase converter: in both cases the strong bond among the phases is exploited to reduce the number of required components.

Moreover, in Figure 3.2 two topologies exploiting one single source are shown. In Figure 3.2a) the series configuration is obtained splitting the single source through the two capacitors feeding the inverters. Similarly, the parallel connection in Figure 3.2b) has DC busses parallel connected to the same source.

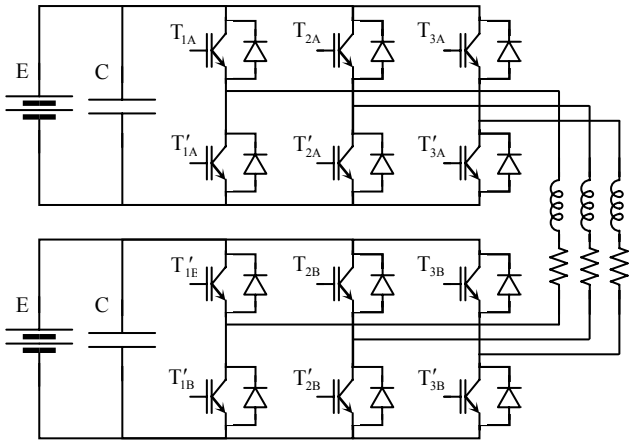


Figure 3.1: Dual 2-level inverter with two sources.

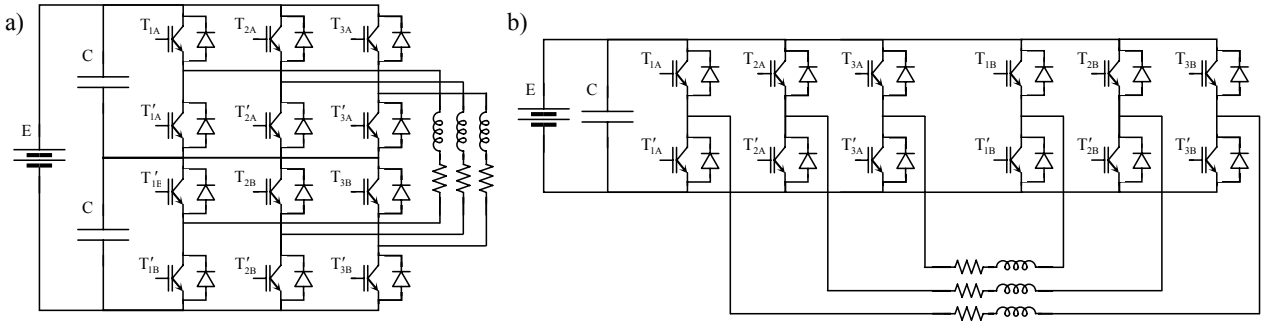


Figure 3.2: Dual 2-level inverter with one source. a) Series configuration; b) Parallel configuration.

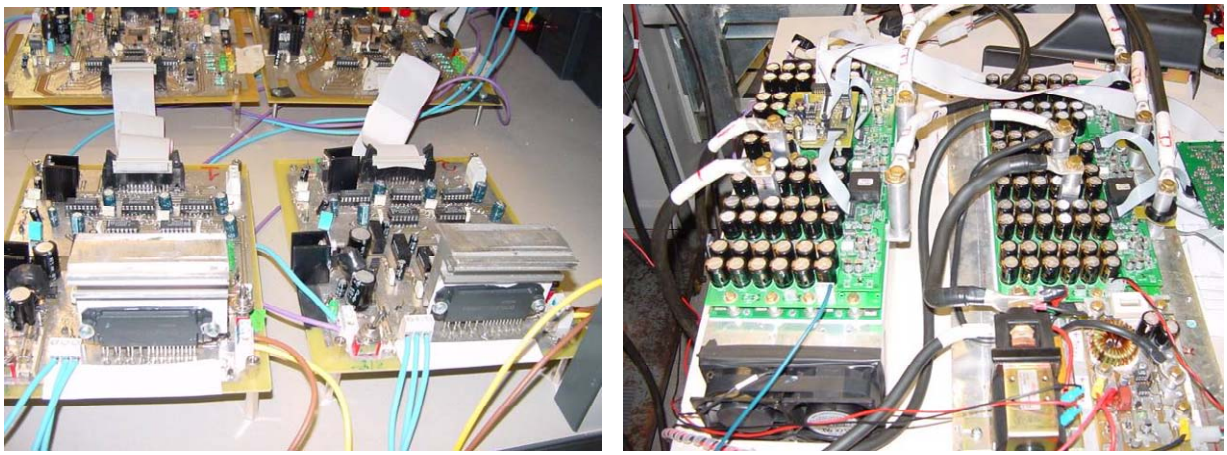
Independently of the configuration, this converter is implemented using two standard 3-phase inverters. The advantage of this choice is the great availability and the high reliability of the components because they are standards wide commercialized. Moreover, some integrated solution is available for low rated system like the IRAMS10UP60 produced by International Rectifier.

The single-source configurations present the evident advantage to easily substitute a previous converter in an existent system because they require a single DC bus. Anyway, they have a serious drawback. Due to their topology, common mode current can flow through the load. The effect of common mode current flow is different in series and parallel configurations. In the first case, the current flowing into the load leads to the unbalance of the capacitor voltages: one of them will discharge to zero voltage while the other one will reach DC bus voltage. This means that the converter will work like a standard 2- level 3-phase inverter after the transient time which is quite short. On the other hands, in parallel configuration, the common mode current flowing into the load increases the RMS value of the phase current without any contribution to the delivered power.

The two-sources topology has been implemented in a reduced scale and in a full scale size. The reduced scale, shown in Figure 3.3a), is rated 48V DC bus voltage and 10A RMS phase current, while the full scale, Figure 3.3b), is rated 180V DC bus voltage and 220A RMS phase current. The theoretical approach presented in the following chapter mainly concerns implemented topology, but it can be easily adapted to the other two.

3.1.2. Applications

There are at least two applications in transport where the capability to supply an electric motor by using two separate sources could be of a great interest in the next future. The first one concerns



a) b)

Figure 3.3: Pictures of power stages. a) Reduced scale (48V, 10A); b) Full scale (180V, 220A).

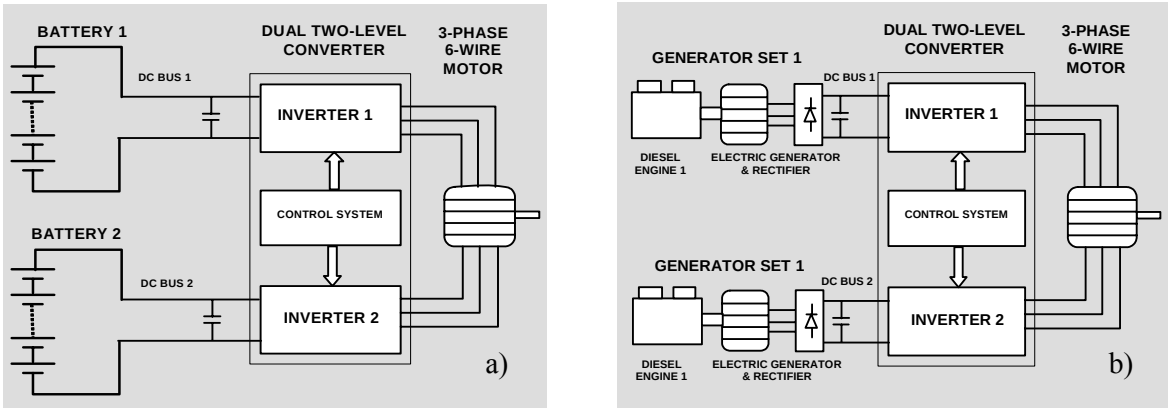


Figure 3.4: Basic schemes using dual 2-level inverter. a) Battery powered electric system; b) diesel-electric propulsion system.

battery powered electric vehicles. The second one is related to hybrid thermal-electric powertrains which are under development for both automotive and ship propulsion.

The battery powered electric vehicles such as electric fork lift trucks and industrial trucks in the power rating lower than 20kW represent more than half of the market and are frequently preferred to thermal engine vehicles for the undeniable economical and environmental advantages inherent in the electric traction.

In modern battery powered industrial electric vehicles, the standard solution for traction system is given by a 2-level inverter feeding a 3-phase induction motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V) for safety reasons. With this solution it is quite difficult to realize an AC drive for a power rating higher than 20kW, due to the high cost of the resulting high-current semiconductor power switches of the inverter. This problem limits the expansion of AC drive and, consequently, the penetration of electric vehicles on this market.

Several solutions have been proposed in order to reduce the current rating of the power switches. The 6-phase machine supplied by a 6-phase inverter [72-75] allows sizing the power switches at half the rated current of an equivalent 3-phase scheme, but requires the implementation of a 6-phase machine. The multi-phase drive solution with 7 or more phases further reduces the power sizing of the converter legs, increases the reliability of the drive, but requires special machine design and complex control hardware [76].

An interesting solution is given by the use of a multilevel inverter, which is implemented with semiconductor devices having a voltage rating lower than the voltage applied to the motor. Several topologies of multilevel converters have been proposed for low voltage applications in the previous chapters. Among these, the dual 2-level inverter can be conveniently used with a battery supply, due to the simplicity to obtain two electrically separated DC sources. The basic scheme of this specific application is given in Figure 3.4a).

An important feature of the dual 2-level inverter, presented in this chapter, is the capability to regulate the power sharing between the two sources yielding to an optimal control of the charge level of the two battery banks.

The second application regard hybrid powertrains which are developed, in series configuration, for the thermal-electric traction system of heavy vehicles (industrial vehicles, trains, busses, etc…) and for the thermal-electric ship propulsion.

An attractive solution for hybrid powertrains could be implemented using the dual 2-level inverter as it is represented in Figure 3.4b). This scheme is based on the use of two diesel-generator units supplying the two inputs of the dual 2-level inverter connected to the motor. In this system the two generating units are controlled in order to operate always with the best efficiency with the respect of the power demanded by the electric motor connected to the vehicle wheels or to the ship screw. This is made possible by using the dual 2-level inverter power sharing feature. A very

interesting characteristic of this system is the capability to operate at high efficiency in the low power range (less than 50%). In fact, the multilevel converter can be supplied from a single side, keeping off one diesel engine. This work condition yields to a reduced fuel consumption.

3.2. Analysis of the system

3.2.1. Generable voltage vectors

The dual 2-level inverter is composed by twelve switches driven dually in couples to avoid source shortcuts. This means that the possible states of the system, called **configurations**, depend on six variables which give the state of each leg. These variables can assume only two values and so the number of all the allowed configurations N_{conf} is given by (3.1).

$$N_{conf} = 2^6 = 64 . \qquad \textbf{(3.1)}$$

In this converter it is quite difficult to identify one phase, cut it off from the system and make it work similarly. This means it is difficult to analyse a part of the converter taken out from the rest due to the strong bond among the phases. It is not possible to distinguish between intra-phase and joint-phase redundancies. Anyway, among the 64 configurations there are a lot of redundant situations. Indeed, as it will be shown in the following, the dual 2-level inverter can generate only 18 active vectors and 1 null vector. To prove this, the system depicted in Figure 3.5 is considered. It is the dual 2-level inverter feeding a 6-wire open-end load. There are two sources and they are supposed to be equal. In Figure 3.5, the directions used for voltage reference are even shown. The two inverters composing the converter produce two different systems of line-to-line voltages clearly labelled in the picture by $\{v_{12A}, v_{23A}, v_{31A}\}$ and $\{v_{12B}, v_{23B}, v_{31B}\}$. Independently of the DC bus connection, the load phase voltages v_1, v_2 and v_3 can be related to line-to-line voltages by using (3.2).

$$\begin{cases} v_1 - v_2 = v_{12A} - v_{12B} \\ v_2 - v_3 = v_{23A} - v_{23B} \\ v_3 - v_1 = v_{31A} - v_{31B} \end{cases} . \qquad \textbf{(3.2)}$$

Given both line-to-line voltages sets $\{v_{12A}, v_{23A}, v_{31A}\}$ and $\{v_{12B}, v_{23B}, v_{31B}\}$, imposed by the two inverters respectively, the system represented in (3.2) is undefined because the three equations

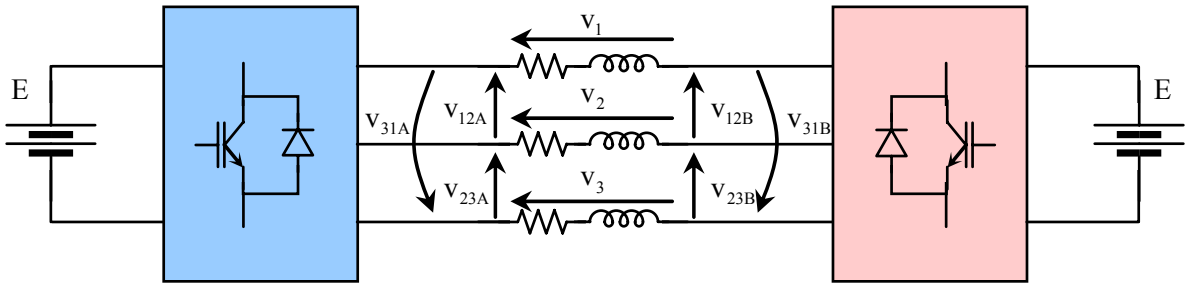


Figure 3.5: Dual 2-level inverter with two sources. Phase and line-to-line voltages for both inverters.

are linear dependent. Moreover, in case of two independent sources and linear balanced load, the load phase common mode voltage is zero.

$$v_1 + v_2 + v_3 = 0\,. \tag{3.3}$$

Considering (3.3), the system in (3.2) can be rearranged in the form expressed by (3.4).

$$\begin{cases} v_1 = \dfrac{v_{12A} - v_{31A}}{3} - \dfrac{v_{12B} - v_{31B}}{3} \\ v_2 = \dfrac{v_{23A} - v_{12A}}{3} - \dfrac{v_{23B} - v_{12B}}{3} \\ v_3 = \dfrac{v_{31A} - v_{23A}}{3} - \dfrac{v_{31B} - v_{23B}}{3} \end{cases}. \tag{3.4}$$

For each set of line-to-line voltages, a related system of phase voltages can be defined. Among all the possible phase voltage sets, the one having a zero sum can be chosen. The desired sets of phase voltages $\{e_{1A}, e_{2A}, e_{3A}\}$ and $\{e_{1B}, e_{2B}, e_{3B}\}$ are given by (3.5).

$$\begin{cases} e_{1A} = \dfrac{v_{12A} - v_{23A}}{3} \\ e_{2A} = \dfrac{v_{23A} - v_{31A}}{3} \\ e_{3A} = \dfrac{v_{31A} - v_{12A}}{3} \end{cases} \qquad \begin{cases} e_{1B} = \dfrac{v_{12B} - v_{23B}}{3} \\ e_{2B} = \dfrac{v_{23B} - v_{31B}}{3} \\ e_{3B} = \dfrac{v_{31B} - v_{12B}}{3} \end{cases}. \tag{3.5}$$

Introducing (3.5) in (3.4), (3.6) are obtained.

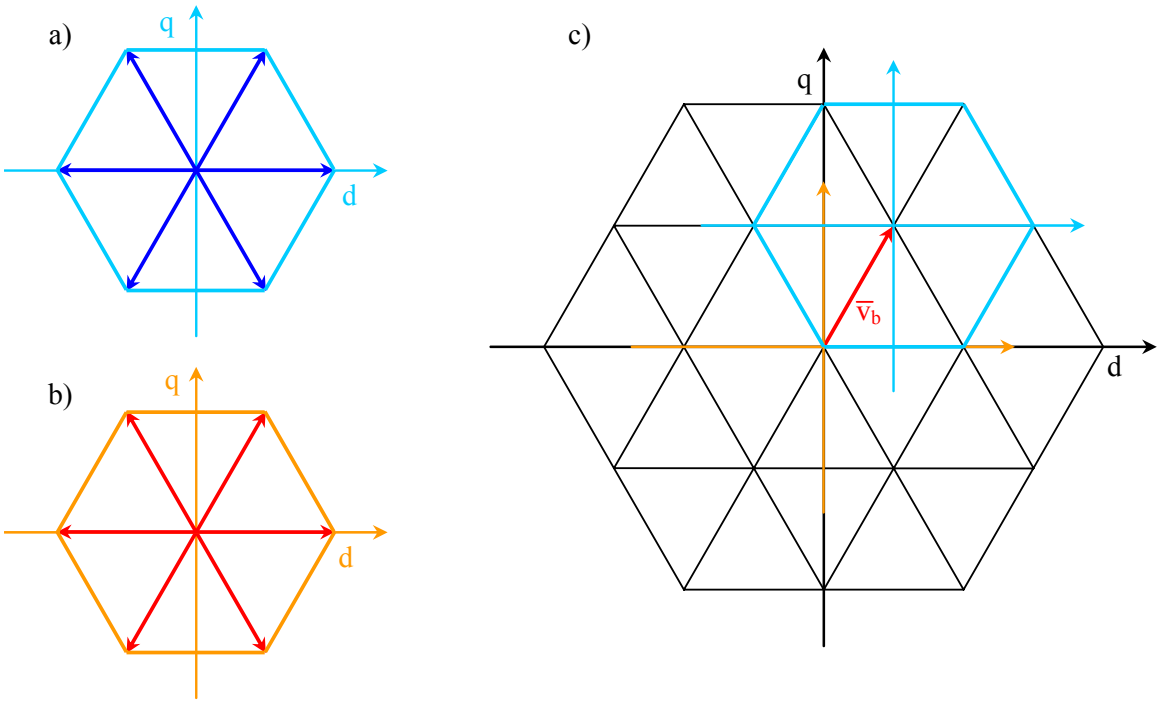


Figure 3.6: Generable vectors in d-q plane. a) and b) Vectors generated by standard 2-level 3-phase inverters; c) Vectors generated by the dual 2-level inverter.

$$\begin{cases} v_1 = e_{1A} - e_{1B} \\ v_2 = e_{2A} - e_{2B} \\ v_3 = e_{3A} - e_{3B} \end{cases}. \tag{3.6}$$

Park transform can be applied to the system given in (3.6) without caring for the common mode voltage. Being $\bar{e}_A$ and $\bar{e}_B$ the complex vectors associated to the phase voltage systems defined in (3.5), (3.7) gives the complex vector $\bar{v}$ related to the load phase voltages, exploiting the linearity of the operator.

$$\bar{v} = \bar{e}_A - \bar{e}_B . \tag{3.7}$$

Both vectors $\bar{e}_A$ and $\bar{e}_B$ can assume all the values defined by the allowed configurations of a standard 2-level 3-phase inverter can assume. It is well known that these configuration are 8, in particular there are 6 active vectors and 1 null vector as depicted in Figure 3.6a) and b). In Figure 3.6c) all the vectors generable by the dual 2-level inverter are shown as vertices of the triangular grid. They are given by the vector subtraction of the vector generated by each inverter. By another point of view, they can be seen as the vector generated by one inverter whose reference frame is translated by the vector applied by the other inverter.

The amplitude of the base vector $\bar{v}_b$ depends on the choice made for the coefficient of Park transform; in the hypothesis that $\frac{2}{3}$ has been chosen, the amplitude of the base vector is given by (3.8).

$$|\bar{v}_b| = \frac{2}{3}E . \tag{3.8}$$

The generable vector with the greatest amplitude is twice the base vector. With this information, the determination of maximum rotating vector amplitude is possible Considering Figure 3.7, the maximum amplitude for a rotating vector is geometrically given by the length of the segment $\overline{AO}$. Being the triangle ABO right, the cathetus $\overline{AO}$, which is equal to the amplitude of the maximum rotating vector v_{MR}, can be easily found:

$$v_{MR} = \frac{4}{3}E\cos(30°) = \frac{2}{\sqrt{3}}E . \tag{3.9}$$

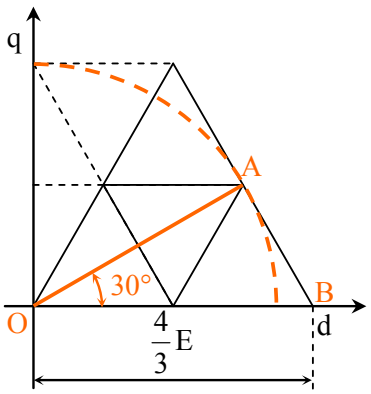


Figure 3.7: Maximum rotating vector determination.

A similar discussion can be done for dual 2-level inverter fed by a single source. Obviously, the common mode current will flow in the system, so load common mode voltage will not be zero even when the load is balanced and linear. This has to be taken into account by the modulation and will be described in Section 3.2.3.

3.2.2. Relationship between leg states and voltage vectors

In the previous section, the vectors generated by the dual 2-level inverter were found out analyzing the 3-phase systems composing it. The converter is composed by six legs, each one can assume two states,: high or low.

A **state function** can be defined to describe the state of each leg. The state function s_x is a real function where the subscript x identifies a specific leg as Figure 3.8 shows. It is useful to assume s_x is equal to 1 when the state of the leg is high, i.e. the leg output voltage is equal to the battery voltage. Otherwise s_x is equal to 0 when the leg output voltage is zero. Defining the state function in this way it is easy to find a relationship between the state of each leg (s_{1A}, s_{2A}, s_{3A}, s_{1B}, s_{2B} and s_{3B}) and the respective output voltage (e_{1A}, e_{2A}, e_{3A}, e_{1B}, e_{2B} and e_{3B}). These relationships are given by (3.10).

$$\begin{cases} e_{1A} = Es_{1A} \\ e_{2A} = Es_{2A} \\ e_{3A} = Es_{3A} \end{cases} \qquad \begin{cases} e_{1B} = Es_{1B} \\ e_{2B} = Es_{2B} \\ e_{3B} = Es_{3B} \end{cases}. \tag{3.10}$$

Park transform can be applied to these two sets of equation, and the complex vectors $\bar{e}_A$ and $\bar{e}_B$ will be found. In (3.11) it is assumed to be $\bar{\alpha} = e^{j\frac{2}{3}\pi}$.

$$\begin{cases} \bar{e}_A = \frac{2}{3}\left(e_{1A} + e_{2A}\bar{\alpha} + e_{3A}\bar{\alpha}^2\right) \\ \bar{e}_B = \frac{2}{3}\left(e_{1B} + e_{2B}\bar{\alpha} + e_{3B}\bar{\alpha}^2\right) \end{cases}. \tag{3.11}$$

Even the common mode voltages e_{0A} and e_{0B}, associated to the complex vectors, can be found. They are given by (3.12).

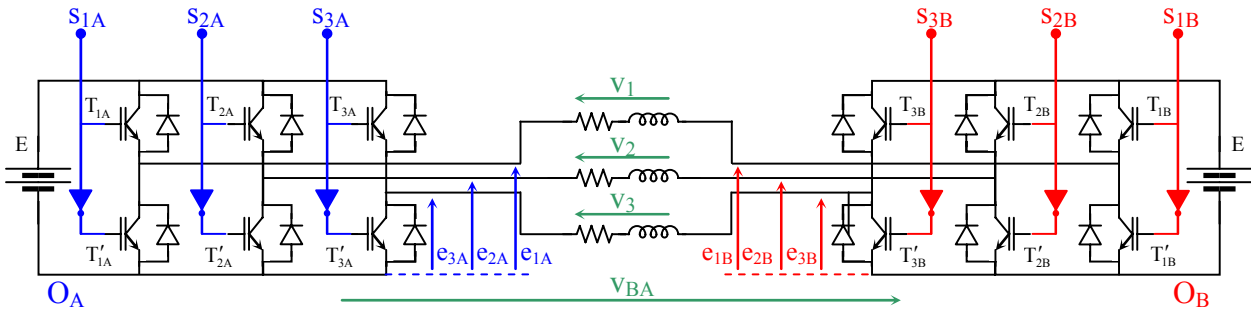


Figure 3.8: Leg states in a dual 2-level inverter.

$$\begin{cases} e_{0A} = \dfrac{e_{1A} + e_{2A} + e_{3A}}{3} \\ e_{0B} = \dfrac{e_{1B} + e_{2B} + e_{3B}}{3} \end{cases} . \qquad \textbf{(3.12)}$$

Substituting (3.10) in (3.11), the relationship between the states of the legs of each inverter and its output voltage vector is found:

$$\begin{cases} \bar{e}_A = E\dfrac{2}{3}\left(s_{1A} + s_{2A}\bar{\alpha} + s_{3A}\bar{\alpha}^2\right) = E\bar{s}_A \\ \bar{e}_B = E\dfrac{2}{3}\left(s_{1B} + s_{2B}\bar{\alpha} + s_{3B}\bar{\alpha}^2\right) = E\bar{s}_B \end{cases} . \qquad \textbf{(3.13)}$$

In (3.13), the terms into round brackets, together to the coefficients at their left, are the Park transform of the two inverter leg state sets $\bar{s}_A$ and $\bar{s}_B$. Considering (3.7), the load phase voltage vector $\bar{v}$ can be expressed using the states of both inverters.

$$\bar{v} = \bar{e}_A - \bar{e}_B = E\left(\bar{s}_A - \bar{s}_B\right). \qquad \textbf{(3.14)}$$

The equation just presented can be expanded substituting to $\bar{s}_A$ and $\bar{s}_B$ their dependency on the leg states. This will bring to (3.15).

$$\begin{aligned} \bar{v} &= E\frac{2}{3}\left[\left(s_{1A} + s_{2A}\bar{\alpha} + s_{3A}\bar{\alpha}^2\right) - \left(s_{1B} + s_{2B}\bar{\alpha} + s_{3B}\bar{\alpha}^2\right)\right] \\ &= E\frac{2}{3}\left[\left(s_{1A} - s_{1B}\right) + \left(s_{2A} - s_{2B}\right)\bar{\alpha} + \left(s_{3A} - s_{3B}\right)\bar{\alpha}^2\right] \\ &= E\frac{2}{3}\left[s_1 + s_2\bar{\alpha} + s_3\bar{\alpha}^2\right] = E\bar{s} \end{aligned} . \qquad \textbf{(3.15)}$$

Equation (3.15) deserves an explanation because it contains the passage from the point of view of two separated inverters to the one of a single converter. The vector $\bar{v}$ is considered as function of all the six states subdivided by their belonging to one inverter or the other. Then the corresponding phases on the inverters are coupled and the states of the whole converter legs s_1, s_2 and s_3 are found. Finally, the passage from these states to the single complex number $\bar{s}$ representing them has been done.

Because the single inverter leg states can assume two values (0 and 1), the whole converter leg states can be equal to -1, 0 and 1. There is an evident redundancy when the whole converter state is zero because it can derive from two different situations as Table 3.1 shows.

s_{xA}	s_{xB}	s_x
1	1	0
1	0	1
0	1	-1
0	0	0

Table 3.1: States of each inverter versus leg sate of the whole converter

The effect of these redundancies can be seen considering the number of all the possible combinations of the whole converter leg states. This number is 27 which is obviously less than the number of possible configurations but it gives some information about the intra-phase and the joint-phase redundancies of the converter. All the redundancies internal to the whole converter leg state can be considered intra-phase. Instead the redundancies inside the 27 combinations just found are to be considered as joint-phase.

States			Characteristics				
s_1	s_2	s_3	v_d	v_q	v	θ	Vector number
1	1	1	0,000	0,000	0	N.A.	0
1	1	0	0,500	0,866	1	60°	2
1	1	-1	1,000	1,732	2	60°	14
1	0	1	0,500	-0,866	1	-60°	6
1	0	0	1,000	0,000	1	0°	1
1	0	-1	1,500	0,866	1,732	30°	7
1	-1	1	1,000	-1,732	2	-60°	18
1	-1	0	1,500	-0,866	1,732	-30°	12
1	-1	-1	2,000	0,000	2	0°	13
0	1	1	-1,000	0,000	1	180°	4
0	1	0	-0,500	0,866	1	120°	3
0	1	-1	0,000	1,732	1,732	90°	8
0	0	1	-0,500	-0,866	1	-120°	5
0	0	0	0,000	0,000	0	N.A.	0
0	0	-1	0,500	0,866	1	60°	2
0	-1	1	0,000	-1,732	1,732	-90°	11
0	-1	0	0,500	-0,866	1	-60°	6
0	-1	-1	1,000	0,000	1	0°	1
-1	1	1	-2,000	0,000	2	180°	16
-1	1	0	-1,500	0,866	1,732	150°	9
-1	1	-1	-1,000	1,732	2	120°	15
-1	0	1	-1,500	-0,866	1,732	-150°	10
-1	0	0	-1,000	0,000	1	180°	4
-1	0	-1	-0,500	0,866	1	120°	3
-1	-1	1	-1,000	-1,732	2	-120°	17
-1	-1	0	-0,500	-0,866	1	-120°	5
-1	-1	-1	0,000	0,000	0	N.A.	0

Table 3.2: The 27 possible configurations accordingly to the whole converter phase states. The value of the module and the projections on d-q axes have to be multiplied by the factor 2/3 E.

In Table 3.2 all the 27 combinationss are shown and the output voltage vector they produce is decomposed in d-q axes and in polar coordinates. Both the Cartesian coordinates and the amplitude of the output vector are given in per unit in the respect of the factor $\frac{2}{3}E$. Moreover in Table 3.2 the redundant vectors are highlighted by different colours. It can be noticed that the null vector can be done using three different combinations of whole converter leg states. Other redundancies are related to the vector of amplitude $\frac{2}{3}E$, which can be generated in two different ways. The last column of the table shows the name which univocally identifies each vector. It is to be compared to Figure 3.10 showing all the active vectors in d-q plane and their identification numbers. In this picture, the joint-phase redundancies are highlighted by the whole converter leg states written in grey background: some vectors are generated by more than one combination.

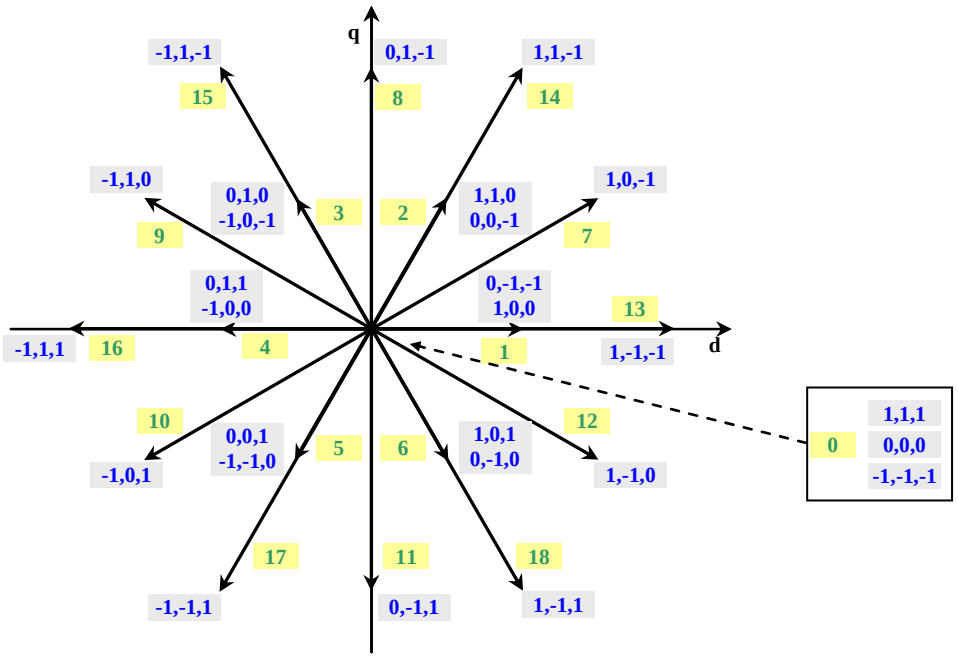


Figure 3.10: Vectors produced by dual 2-level inverter: identification numbers and whole converter leg states.

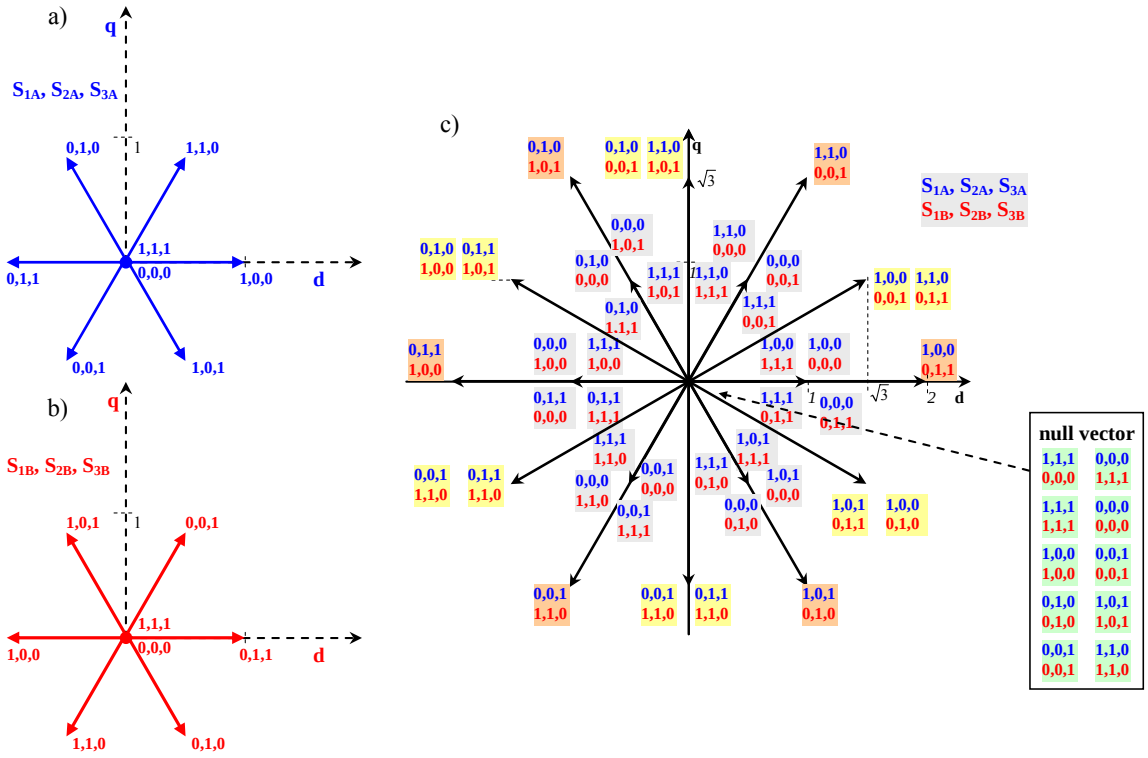


Figure 3.9: Voltage vectors produced by the dual 2-level inverter. a) Voltage vectors produced by inverter A; b) Voltage vectors produced by inverter B in reverse notation; c) Voltage vector produced by the whole converter.

Similar considerations can be done about the redundant configurations of the whole converter. Table 3.3 shows output vectors produced by the dual 2-level inverter considering all the possible configurations of the six leg states.

n	S_{1A}	S_{2A}	S_{3A}	S_{1B}	S_{2B}	S_{3B}	v_d	v_q	v	θ°	v_1	v_2	v_3	e_0	Num.
0	0	0	0	0	0	0	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
1	0	0	0	0	0	1	0,50	0,87	1,00	60	0,5	0,5	-1,0	-1	**2**
2	0	0	0	0	1	0	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	-1	**6**
3	0	0	0	0	1	1	1,00	0,00	1,00	0	1,0	-0,5	-0,5	-2	**1**
4	0	0	0	1	0	0	-1,00	0,00	1,00	180	-1,0	0,5	0,5	-1	**4**
5	0	0	0	1	0	1	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	-2	**3**
6	0	0	0	1	1	0	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	-2	**5**
7	0	0	0	1	1	1	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	-3	**0**
8	0	0	1	0	0	0	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	1	**5**
9	0	0	1	0	0	1	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
10	0	0	1	0	1	0	0,00	-1,73	1,73	-90	0,0	-1,5	1,5	0	**11**
11	0	0	1	0	1	1	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	-1	**6**
12	0	0	1	1	0	0	-1,50	-0,87	1,73	-150	-1,5	0,0	1,5	0	**10**
13	0	0	1	1	0	1	-1,00	0,00	1,00	180	-1,0	0,5	0,5	-1	**4**
14	0	0	1	1	1	0	-1,00	-1,73	2,00	-120	-1,0	-1,0	2,0	-1	**17**
15	0	0	1	1	1	1	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	-2	**5**
16	0	1	0	0	0	0	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	1	**3**
17	0	1	0	0	0	1	0,00	1,73	1,73	90	0,0	1,5	-1,5	0	**8**
18	0	1	0	0	1	0	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
19	0	1	0	0	1	1	0,50	0,87	1,00	60	0,5	0,5	-1,0	-1	**2**
20	0	1	0	1	0	0	-1,50	0,87	1,73	150	-1,5	1,5	0,0	0	**9**
21	0	1	0	1	0	1	-1,00	1,73	2,00	120	-1,0	2,0	-1,0	-1	**15**
22	0	1	0	1	1	0	-1,00	0,00	1,00	180	-1,0	0,5	0,5	-1	**4**
23	0	1	0	1	1	1	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	-2	**3**
24	0	1	1	0	0	0	-1,00	0,00	1,00	180	-1,0	0,5	0,5	2	**4**
25	0	1	1	0	0	1	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	1	**3**
26	0	1	1	0	1	0	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	1	**5**
27	0	1	1	0	1	1	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
28	0	1	1	1	0	0	-2,00	0,00	2,00	180	-2,0	1,0	1,0	1	**16**
29	0	1	1	1	0	1	-1,50	0,87	1,73	150	-1,5	1,5	0,0	0	**9**
30	0	1	1	1	1	0	-1,50	-0,87	1,73	-150	-1,5	0,0	1,5	0	**10**
31	0	1	1	1	1	1	-1,00	0,00	1,00	180	-1,0	0,5	0,5	-1	**4**
32	1	0	0	0	0	0	1,00	0,00	1,00	0	1,0	-0,5	-0,5	1	**1**
33	1	0	0	0	0	1	1,50	0,87	1,73	30	1,5	0,0	-1,5	0	**7**
34	1	0	0	0	1	0	1,50	-0,87	1,73	-30	1,5	-1,5	0,0	0	**12**
35	1	0	0	0	1	1	2,00	0,00	2,00	0	2,0	-1,0	-1,0	-1	**13**
36	1	0	0	1	0	0	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
37	1	0	0	1	0	1	0,50	0,87	1,00	60	0,5	0,5	-1,0	-1	**2**
38	1	0	0	1	1	0	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	-1	**6**
39	1	0	0	1	1	1	1,00	0,00	1,00	0	1,0	-0,5	-0,5	-2	**1**
40	1	0	1	0	0	0	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	2	**6**
41	1	0	1	0	0	1	1,00	0,00	1,00	0	1,0	-0,5	-0,5	1	**1**
42	1	0	1	0	1	0	1,00	-1,73	2,00	-60	1,0	-2,0	1,0	1	**18**
43	1	0	1	0	1	1	1,50	-0,87	1,73	-30	1,5	-1,5	0,0	0	**12**
44	1	0	1	1	0	0	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	1	**5**
45	1	0	1	1	0	1	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
46	1	0	1	1	1	0	0,00	-1,73	1,73	-90	0,0	-1,5	1,5	0	**11**
47	1	0	1	1	1	1	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	-1	**6**
48	1	1	0	0	0	0	0,50	0,87	1,00	60	0,5	0,5	-1,0	2	**2**
49	1	1	0	0	0	1	1,00	1,73	2,00	60	1,0	1,0	-2,0	1	**14**
50	1	1	0	0	1	0	1,00	0,00	1,00	0	1,0	-0,5	-0,5	1	**1**
51	1	1	0	0	1	1	1,50	0,87	1,73	30	1,5	0,0	-1,5	0	**7**
52	1	1	0	1	0	0	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	1	**3**
53	1	1	0	1	0	1	0,00	1,73	1,73	90	0,0	1,5	-1,5	0	**8**
54	1	1	0	1	1	0	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**
55	1	1	0	1	1	1	0,50	0,87	1,00	60	0,5	0,5	-1,0	-1	**2**
56	1	1	1	0	0	0	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	3	**0**
57	1	1	1	0	0	1	0,50	0,87	1,00	60	0,5	0,5	-1,0	2	**2**
58	1	1	1	0	1	0	0,50	-0,87	1,00	-60	0,5	-1,0	0,5	2	**6**
59	1	1	1	0	1	1	1,00	0,00	1,00	0	1,0	-0,5	-0,5	1	**1**
60	1	1	1	1	0	0	-1,00	0,00	1,00	180	-1,0	0,5	0,5	2	**4**
61	1	1	1	1	0	1	-0,50	0,87	1,00	120	-0,5	1,0	-0,5	1	**3**
62	1	1	1	1	1	0	-0,50	-0,87	1,00	-120	-0,5	-0,5	1,0	1	**5**
63	1	1	1	1	1	1	0,00	0,00	0,00	N.A.	0,0	0,0	0,0	0	**0**

Table 3.3: Switches configurations and related output voltage vectors (in p.u.).

The null vector is given by nine configurations. Comparing Table 3.2 and Table 3.3, it can be seen that seven intra-phase redundancies are related to the null output vector deriving from s_1, s_2

and s_3 equal to zero. Each one of the other two combinations producing null output are given by a single configuration. Each one of the six shortest vectors is obtained using six different configurations. The middle vectors, which are univocally determined by the whole converter leg states, are given by two different configurations. A single configuration still gives each one of the six longest vectors.

Figure 3.9a) and b) show the vectors produced by each configuration of inverter A and inverter B respectively. Figure 3.9b) depicts the voltage vectors in **reverse notation** to make the sum in (3.14) easier. Reverse notation means that drawn voltage vectors for inverter B include the minus appearing in the equation, so all the subtractions are transformed in sums. Figure 3.9c) shows the vectors generated by the dual 2-level inverter. In the picture all the configurations generating a specific vector are written near it. The backgrounds of these configurations are in different colours classifying the vectors on the basis of their length: null, short, middle and long. Obviously, for the reasons explained above, there is a relationship between the redundancies and the length of the vectors, so the different colours even identify the number of configuration giving each vector.

3.2.3. Common mode voltage

To conclude the analysis of the dual two level inverter, some considerations about common mode voltage and its effect on the voltage between the negative pole of DC busses, O_A and O_B, can be done. Referring to Figure 3.11, Kirchhoff's voltage law applied to the close path of each phase gives (3.16).

$$\begin{cases} e_{1A} = v_1 + e_{1B} + v_{BA} \\ e_{2A} = v_2 + e_{2B} + v_{BA} \\ e_{3A} = v_3 + e_{3B} + v_{BA} \end{cases}. \qquad \textbf{(3.16)}$$

Summing all the equation and introducing the common mode component given by (3.12), the following equation is obtained.

$$v_{BA} = \frac{e_{1A} + e_{2A} + e_{3A}}{3} - \frac{e_{1B} + e_{2B} + e_{3B}}{3} - \frac{v_1 + v_2 + v_3}{3} = e_{0A} - e_{0B} - v_0 . \qquad \textbf{(3.17)}$$

Applying Gauss theorem to the dashed line drawn in Figure 3.11, it can be noticed that the sum of the three load currents (i_1, i_2 and i_3) must be zero. In case of symmetrical and linear load, even the sum of the load phase voltage must be zero: i.e. the load phase common mode voltage v_0 is zero. In this way, (3.17) can be simplified.

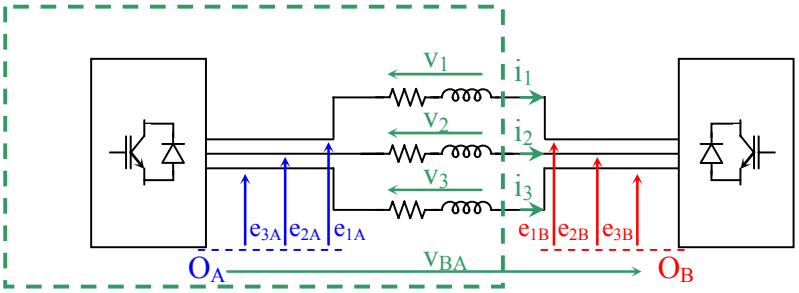


Figure 3.11: Common mode voltage. Gauss theorem applied to the dual 2-level inverter: two insulated sources assure that the sum of load currents is zero.

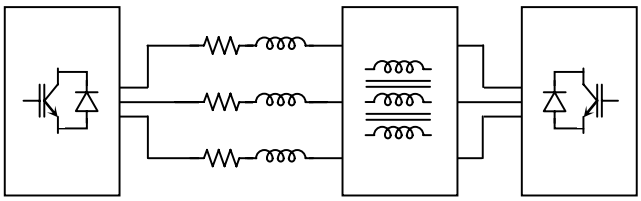


Figure 3.12: Common mode reactance in series to the load to avoid common mode current flow.

$$v_{BA} = e_{0A} - e_{0B} = e_0 . \qquad \textbf{(3.18)}$$

The meaning of (3.18) is simple: the common mode voltage produced by the converter (i.e. the difference between the common mode voltages each inverter produces) is compensated by the voltage fluctuation of DC busses negative poles. In this way, the common mode voltage which avoid the load phase common mode current flow, is obtained. The 15th column of Table 3.3 gives the value of common mode voltage each configuration produces. It can be seen that e_0 can assume values between 3 and -3 referred to the DC bus voltage.

Common mode voltage is not a problem when the sources are insulated, but in the topologies with a single source some precaution has to be taken in order to avoid common mode current flow. Among all the various ways to minimize the common mode current, the simplest is to put a common mode reactance in series to the load as Figure 3.12 explains.

The common mode reactance is a 3-phase reactive component which maximizes its reactance at the common mode sequence. In this way, the electrical circuit related to the common mode current has high impedance. The main drawback of this method is to require a quite expensive additional component which is not present in common applications. Anyway a 3-phase transformer can be used as common mode reactance in applications including it. The primary windings are fed by the dual 2-level inverter while the secondary windings are star connected to avoid common mode current flow.

Other solutions have been studied in literature regarding particular modulation strategies avoiding the instantaneous common mode voltage. One of them, presented in [49], can be shortly described as follow. Considering Table 3.3, it can be seen that some configurations produce zero

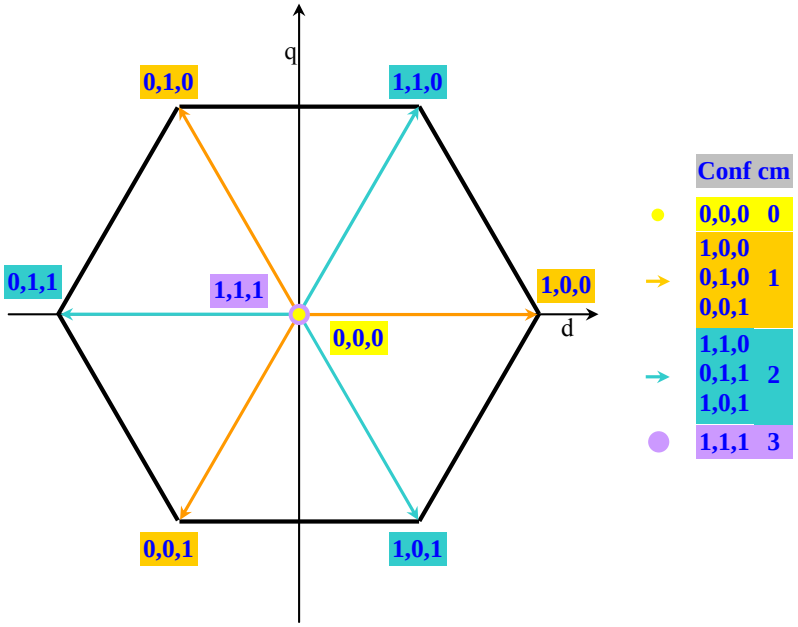


Figure 3.13: Vectors produced by 3-phase inverter divided in four families on the basis of related common mode voltage.

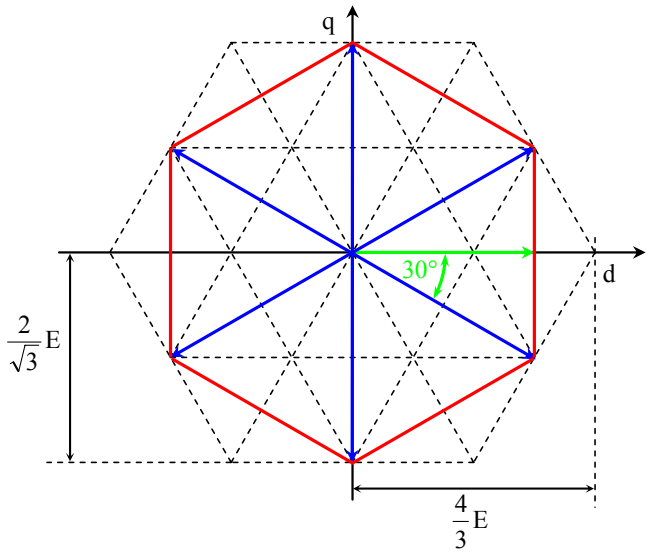


Figure 3.14: Active voltage vectors produced by dual 2-level inverter without common mode. In green is shown the maximum producible rotating vector which is the apothem of the red hexagon.

common mode voltage: this happens because the common mode voltage of both inverters are equal.

For one 3-phase inverter produced vectors can be classified in four families on the basis of related common mode voltage. In Figure 3.13 the configurations of a standard 3-phase inverter, producing the same common mode voltage, are drawn in the same colour with the notation used for inverter H. If both inverters produce output vectors belonging to the same family, common mode voltage will be zero due to (3.18).

In the respect of this bond, the configurations the dual 2-level inverter can assume are 20, among them 12 produce an active vector and 8 the null one. Unfortunately, the 12 configurations related to active vectors are redundant and only six different vectors can be output. These six vectors are depicted in Figure 3.14 in which they are compared to the outputs of the dual 2-level inverter without any bonds It can be seen that the six active vectors are disposed as vertices of a hexagon. This hexagon resembles the standard 3-phase inverter locus, but it is larger and 30° rotated. The maximum rotating vector which can be produced is given by (3.19) accordingly with Figure 3.14.

$$v'_{MR} = \frac{2}{\sqrt{3}} E\cos(30°) = E\,. \qquad \textbf{(3.19)}$$

An interesting comparison can be done among the active powers P_{CMB}, P and P_{3P} delivered by a dual 2-level inverter modulated with and without bonds and a standard 3-phase 2-level inverter respectively. Assuming the vector $\bar{i} = I\cos(\theta)$ represents the load current in all the three cases, it leads to:

$$\begin{aligned} P &= \frac{3}{2}\bar{v}_{MR}\cdot\bar{i} = \sqrt{3}EI\cos(\theta) \\ P_{CMB} &= \frac{3}{2}\bar{v}'_{MR}\cdot\bar{i} = \frac{3}{2}EI\cos(\theta)\,. \\ P_{3P} &= \frac{3}{2}\bar{v}''_{MR}\cdot\bar{i} = \frac{\sqrt{3}}{2}EI\cos(\theta) \end{aligned} \qquad \textbf{(3.20)}$$

As expected the power delivered by dual 2-level inverter without any bonds is twice the power delivered by a standard 3-phase 2-level inverter. The power delivered by the dual 2-level inverter, modulated for no common mode, is n the between.

3.2.4. Dual 2-level inverter with different source voltages

Until here, the study of the dual 2-level inverter has been conducted in the hypothesis the two sources had the same voltage. Some interesting aspects of the converter can be analysed when the two DC bus sources have different values, in particular it is supposed to be $E_A > E_B$ just to fix the problem.

To better understand what is happening when the sources are unequal, two specific 3-phase inverter configurations are considered. Being $\bar{s}_x$ and $\bar{s}_y$ the complex vectors representing the configurations $\{s_{1x}=1,\ s_{2x}=0,\ s_{3x}=0\}$ and $\{s_{1y}=1,\ s_{2y}=1,\ s_{3y}=0\}$ respectively, the output vectors $\bar{v}_1$ and $\bar{v}_2$ given by (3.21) are drawn in Figure 3.15.

$$\begin{aligned}\bar{v}_1 &= E_A\bar{s}_x + E_B\bar{s}_y \\ \bar{v}_2 &= E_A\bar{s}_y + E_B\bar{s}_x\end{aligned} \qquad \textbf{(3.21)}$$

The complex vectors associated to the configurations represent the direction on which the voltage vectors composing $\bar{v}_1$ and $\bar{v}_2$ are laying, in this case 0° and 60° from the d-axis. The amplitude of the voltage vectors is specified by the value of the sources. In Figure 3.15a), the voltage composition shown is obtained when the sources are equal and it leads to the treatment just completed. In Figure 3.15b) the voltage composition regards an interesting case, where $E_A = 2E_B$. The output vectors $\bar{v}_1$ and $\bar{v}_2$ have the same module, given by Carnot's Theorem, but they lay in different directions. This means that some vectors, which were redundant with balanced sources, are decoupled when $E_A \neq E_B$. Choosing a proper ratio between the two sources values increments the number of produced output vectors.

Two cases are presented, when $E_A = 2E_B$ and $E_A = 3E_B$. The vectors produced in both situations are shown in Figure 3.16 as green dots. The vertices of the seven red hexagons represent the translations in d-q plane of the hexagon associated to inverter L by each of the vectors produced by inverter H. The displacement of the output vectors in d-q plane when $E_A = 2E_B$ (Figure 3.16a)) is similar to 4-level converter. The active vectors are 37 and are evenly disposed on the plane. Some redundancies are still present where two vertices belonging to different hexagons are superimposed or when the vector is obtained using a null configuration of either inverter A or inverter B. The most outer vectors can be generated by a single configuration each one. The null vector is generated

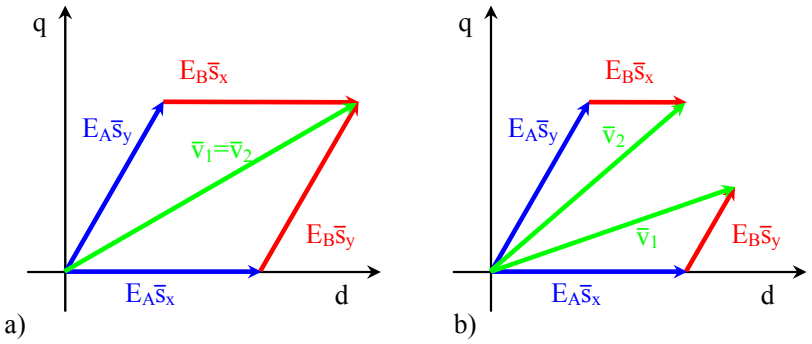


Figure 3.15: Vector compositions. a) The sources are equal; b)The sources are different: E_A=2E_B.

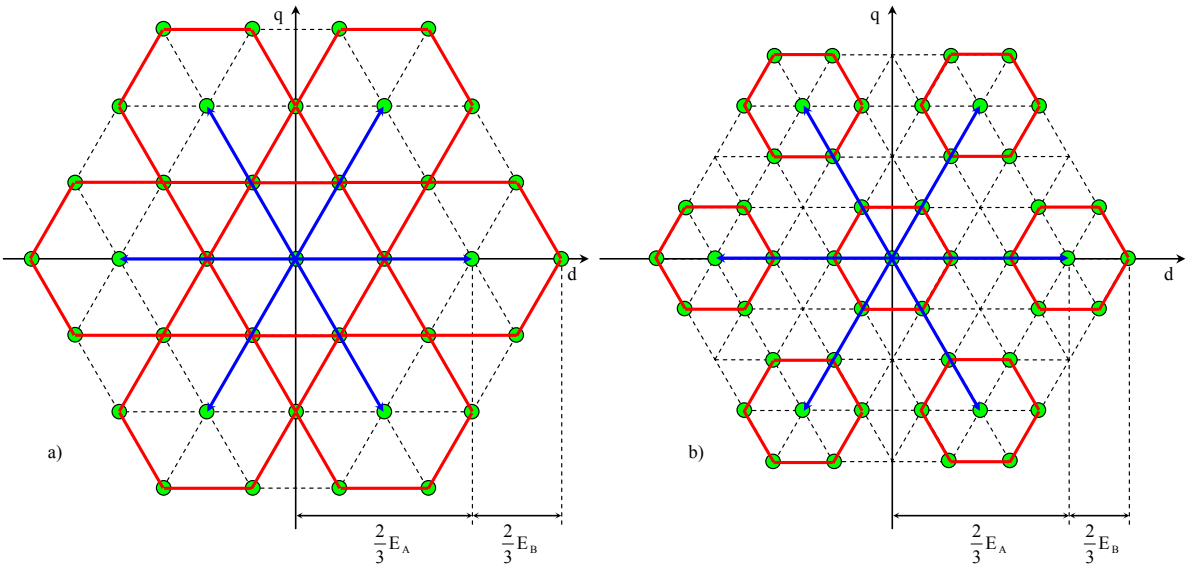


Figure 3.16: Voltage vectors produced in case of different sources. a) E_A is twice E_B; b) E_A is three times E_B.

by four configurations. The vectors in the middle are produced by two or three configurations.

Another interesting situation is depicted in Figure 3.16b) where $E_A = 3E_B$. The active vectors generated are 48 and they are symmetrically, but not evenly disposed on the plane. Considering this particular disposition, there are some regions in which it is difficult to find the best vectors triplet to apply to generate the reference. Anyway, this is a problem which lays outside the purpose of this book. Even in this case there are redundancies. For instance, the null vector can be generated by four configurations and other vectors, involving one inverter producing the null vector, are associated to two configurations.

The second case presented is the most general, because a further increment of the ratio does not increase the number of active vectors, it simply stretches the figure. The redundancies still present depend on the inherent redundancy of the null vector for both the two inverters.

3.3. Analytical approach: complex duty-cycles

3.3.1. Complex duty-cycles definition

In the previous section, the study of the dual 2-level inverter has been conducted considering instantaneous values of the applied vectors. A different approach can be done taking into consideration the mean output voltage. This new approach does not add anything new, but gives a mathematical view of the converter through the **complex duty-cycles**.

Considering Figure 3.8, inverters legs outputs e_{1A}, e_{2A}, e_{3A}, e_{1B}, e_{2B} and e_{3B} can be expressed as function of respective leg state s_{1A}, s_{2A}, s_{3A}, s_{1B}, s_{2B} and s_{3B} by (3.10). Applying Park transform the complex vector representing the inverters output voltages ($\bar{e}_A$, $\bar{e}_B$) and the load phase voltage $\bar{v}$, together to their common mode components (e_{0A}, e_{0B} and v_0), can be found as functions of the inverters states $\bar{s}_A$, $\bar{s}_B$, s_{0A} and s_{0B}.

$$\begin{cases} \bar{v} = E(\bar{s}_A - \bar{s}_B) \\ v_{AB} = E(s_{0A} - s_{0B}) \end{cases}. \qquad \textbf{(3.22)}$$

The complex vectors $\bar{s}_A$ and $\bar{s}_B$ were defined by (3.13), while (3.23) gives the definitions of their common mode components s_{0A} and s_{0B}.

$$s_{0A} = \frac{s_{1A} + s_{2A} + s_{3A}}{3} \qquad s_{0B} = \frac{s_{1B} + s_{2B} + s_{3B}}{3}. \tag{3.23}$$

Unfortunately, the output voltage so obtained is not constant, but changes due to the commutations the converter makes. So, following the reference instant by instant is impossible, but something can be done over the average values in a period. Being T_C the period, it is possible to produce an average output voltage equal to the desired reference $\bar{v}^*$, imposing (3.24).

$$\bar{v}^* = \frac{1}{T_C}\int_0^{T_C} \bar{v}\,dt = \frac{E}{T_C}\int_0^{T_C} (\bar{s}_A - \bar{s}_B)\,dt. \tag{3.24}$$

In some dual 2-level inverter topologies, common mode voltage holds a crucial role and it is necessary to modulate even this components. Even for the common mode voltage, its average value can be synthesised to be equal to a given reference v_{AB}^*.

$$v_{AB}^* = \frac{1}{T_C}\int_0^{T_C} v_{AB}\,dt = \frac{E}{T_C}\int_0^{T_C} (s_{0A} - s_{0B})\,dt. \tag{3.25}$$

The **complex duty-cycles** $\bar{m}_A$ and $\bar{m}_B$, for inverters A and B respectively, can be defined as the mean values of the complex vectors associated to the state functions of each inverter. In the mathematical point of view, (3.26) expresses the definition.

$$\bar{m}_A = \frac{1}{T_C}\int_0^{T_C} \bar{s}_A\,dt \qquad \bar{m}_B = \frac{1}{T_C}\int_0^{T_C} \bar{s}_B\,dt. \tag{3.26}$$

Similarly, two new parameters can be defined for the common mode voltage of each inverter to summarize its average value.

$$m_{0A} = \frac{1}{T_C}\int_0^{T_C} s_{0A}\,dt \qquad m_{0B} = \frac{1}{T_C}\int_0^{T_C} s_{0B}\,dt. \tag{3.27}$$

Introducing (3.26) in (3.24) and (3.27) in (3.25), the relationship among the references $\bar{v}^*$ and v_0^* with the complex duty-cycles can be found as (3.28) and (3.29) show.

$$\bar{v}^* = E\left(\frac{1}{T_C}\int_0^{T_C} \bar{s}_A\,dt - \frac{1}{T_C}\int_0^{T_C} \bar{s}_B\,dt\right) = E(\bar{m}_A - \bar{m}_B) \tag{3.28}$$

$$v_{AB}^* = E\left(\frac{1}{T_C}\int_0^{T_C} s_{0A}\,dt - \frac{1}{T_C}\int_0^{T_C} s_{0B}\,dt\right) = E(m_{0A} - m_{0B}). \tag{3.29}$$

In order to determine the complex duty-cycles and their common mode components, (3.28) and (3.29) have to be inverted.

$$\begin{cases} \left(\overline{m}_A - \overline{m}_B\right) = \dfrac{\overline{v}^*}{E} \\ \left(m_{0A} - m_{0B}\right) = \dfrac{v_{AB}^*}{E} \end{cases} . \qquad \textbf{(3.30)}$$

In (3.30) there are two complex variables and two real variables, whereas there are one complex and one real constraint. It is quite simple to understand that the system present three real degrees of freedom. Two new variables are introduced to parameterize the system: $\overline{m}_S$ and m_{0S}. Their relationships with the complex duty-cycles and common mode components are given by (3.31).

$$\overline{m}_S = \overline{m}_A + \overline{m}_B \qquad\qquad m_{0S} = m_{0A} + m_{0B} . \qquad \textbf{(3.31)}$$

Substituting (3.31) in (3.30) leads to a parametric solution in which the inverters states explicitly depend on the parameters just introduced.

$$\begin{cases} \overline{m}_A = \dfrac{\overline{m}_S}{2} + \dfrac{1}{2}\dfrac{\overline{v}^*}{E} \\ \overline{m}_B = \dfrac{\overline{m}_S}{2} - \dfrac{1}{2}\dfrac{\overline{v}^*}{E} \end{cases} \qquad \begin{cases} m_{0A} = \dfrac{m_{0S}}{2} + \dfrac{1}{2}\dfrac{v_{AB}^*}{E} \\ m_{0B} = \dfrac{m_{0S}}{2} - \dfrac{1}{2}\dfrac{v_{AB}^*}{E} \end{cases} . \qquad \textbf{(3.32)}$$

As last step, applying the inverse transform to (3.32), the state functions for all the legs can be found.

$$\begin{cases} m_{1A} = \dfrac{m_{0A}}{3} + \overline{m}_A \cdot e^{j0} \\ m_{2A} = \dfrac{m_{0A}}{3} + \overline{m}_A \cdot e^{j\frac{2\pi}{3}} \\ m_{3A} = \dfrac{m_{0A}}{3} + \overline{m}_A \cdot e^{j\frac{4\pi}{3}} \end{cases} \qquad \begin{cases} m_{1B} = \dfrac{m_{0B}}{3} + \overline{m}_B \cdot e^{j0} \\ m_{2B} = \dfrac{m_{0B}}{3} + \overline{m}_B \cdot e^{j\frac{2\pi}{3}} \\ m_{3B} = \dfrac{m_{0B}}{3} + \overline{m}_B \cdot e^{j\frac{4\pi}{3}} \end{cases} . \qquad \textbf{(3.33)}$$

Equation (3.33) introduces the parameters m_{1A}, m_{2A}, m_{3A}, m_{1B}, m_{2B} and m_{3B} which are the average values over the period T_C of the state functions of all the six converter legs or, in other words, the **legs duty-cycles** to modulate the desired references. This can be easily seen by (3.34) obtained introducing the definitions of $\overline{m}_A$, $\overline{m}_B$, m_{0A} and m_{0B} in (3.33) and developing the calculations.

$$\begin{cases} m_{1A} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{1A}\,dt \\ m_{2A} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{2A}\,dt \\ m_{3A} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{3A}\,dt \end{cases} \qquad \begin{cases} m_{1B} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{1B}\,dt \\ m_{2B} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{2B}\,dt \\ m_{3B} = \dfrac{1}{T_C}\displaystyle\int_0^{T_C} s_{3B}\,dt \end{cases} . \tag{3.34}$$

Considering that each state function can assume only two values during a period, either 0 or 1, it is clear that leg duty-cycles can assume any real value in the interval $[0;1]$ depending on the ratio between the time the state function is 1 and the period itself.

3.3.2. Limits and degrees of freedom

Due to the relationship between the leg duty-cycles and the complex duty-cycles, it is obvious that the limits of variation just found will have a correspondent in the complex plane. To catch the complex limit two new parameters Δm_A and Δm_B are defined as the differences between the maximum and minimum values of leg duty-cycles of each inverter.

$$\begin{cases} \Delta m_A = \max(m_{1A}, m_{2A}, m_{3A}) - \min(m_{1A}, m_{2A}, m_{3A}) \\ \Delta m_B = \max(m_{1B}, m_{2B}, m_{3B}) - \min(m_{1B}, m_{2B}, m_{3B}) \end{cases} . \tag{3.35}$$

Because of the limits on the leg duty-cycles, even Δm_A and Δm_B can assume only a value between 0 and 1. The further analysis concerns the two 2-level inverters composing the converter considered separately. To be faster, only the analysis of inverter A limits will be explicit because the inverter B behaves similarly. The limit of $\overline{m}_A$, varying Δm_A, can be caught finding out the contouring of the function $\Delta m_A(\overline{m}_A)$.

Ordering the leg duty-cycles on the basis of their values, from the greatest to the smallest, the d-q plane can be subdivided in six sectors as Figure 3.17a) shows. Obviously, the sectors so obtained

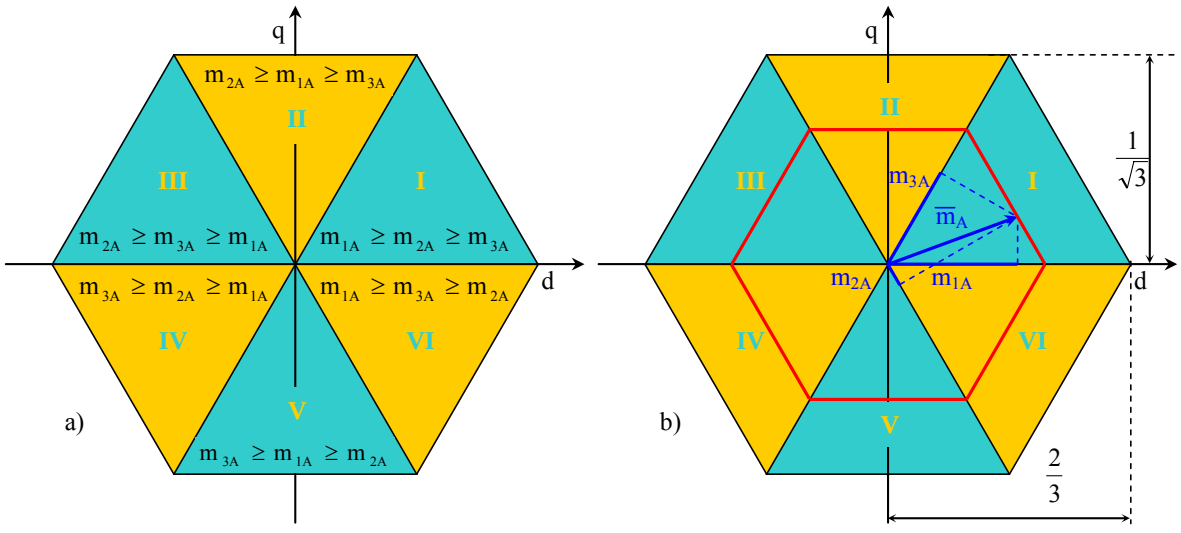


Figure 3.17: Complex duty-cycle limit for inverter A. a) Definition of sectors; b) Determination of contouring and limit.

coincide with the sectors defined in the previous section: it is only a different way to express the same concept. Considering sector I, a generic complex duty-cycle $\overline{m}_A$ can be inverse transformed and obtain its components m'_{1A}, m'_{2A} and m'_{3A} which are the projections of the vector on the phase axes as Figure 3.17b) depicts. They are given by (3.36).

$$\begin{cases} m'_{1A} = \overline{m}_A \cdot e^{j0} \\ m'_{2A} = \overline{m}_A \cdot e^{j\frac{2}{3}\pi} \\ m'_{3A} = \overline{m}_A \cdot e^{j\frac{4}{3}\pi} \end{cases}. \qquad \textbf{(3.36)}$$

Considering the condition defining sector I, $m_{1A} \geq m_{2A} \geq m_{3A}$, a similar relationship can be find involving the new parameters: it has to be $m'_{1A} \geq m'_{2A} \geq m'_{3A}$. Knowing the maximum and the minimum value, it is possible to determine Δm_A.

$$\Delta m_A = m_{1A} - m_{3A} = m'_{1A} - m'_{3A} = \overline{m}_A \cdot e^{j0} - \overline{m}_A \cdot e^{j\frac{4}{3}\pi} = \sqrt{3}\overline{m}_A \cdot e^{j\frac{\pi}{6}}. \qquad \textbf{(3.37)}$$

Keeping constant Δm_A means to keep constant the dot product in (3.37), that is to keep constant the projection of vector $\overline{m}_A$ on the direction of $e^{j\frac{\pi}{6}}$. This condition can be achieved, for any given Δm_A, by vectors laying on the line perpendicular to the bisector of sector I. Doing the same for the other sectors it is possible to draw the contours with a constant Δm_A which are hexagons centred on the origin of the axes, like the red one presented in Figure 3.17b). Imposing $\Delta m_A = 1$, which is its maximum limit, the most outer hexagon can be drawn. Considering (3.37), the amplitude of maximum vector m_{Amax} generable on the direction of $e^{j\frac{\pi}{6}}$ can be found.

$$m_{Amax} = \frac{\Delta m_{Amax}}{\sqrt{3}} = \frac{1}{\sqrt{3}}. \qquad \textbf{(3.38)}$$

In other words, (3.38) gives the value of the most outer hexagon apothem. Consequently, the

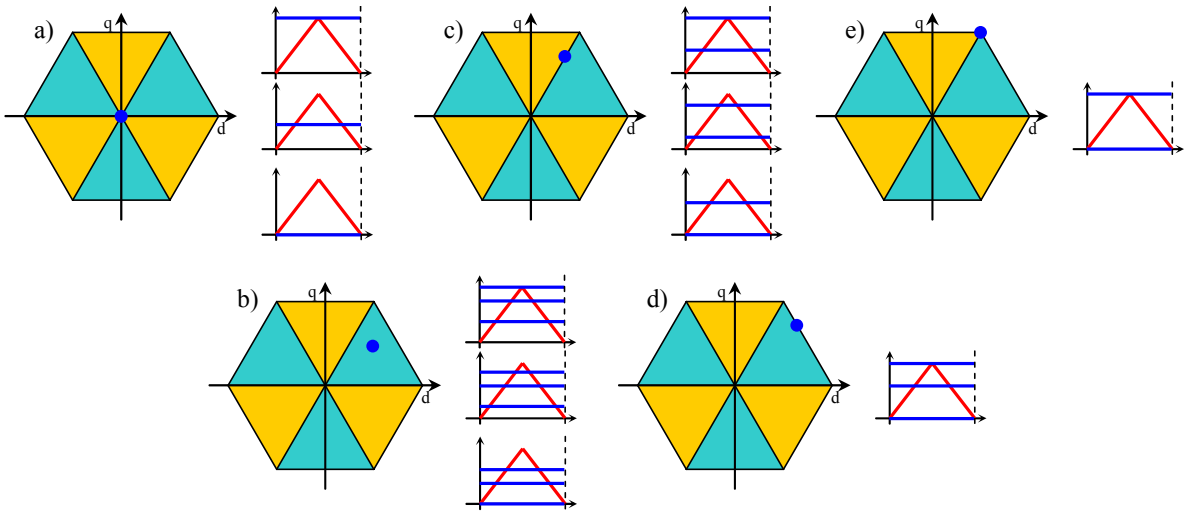


Figure 3.18: Relationship between complex duty-cycle position on d-q plane and possible values for the leg duty-cycles. a) Centred in the origin; b) Generic position inside a sector; c) On border of a sector; d) On the maximum limit; e) In one vertex.

hexagon side is $\frac{2}{3}$ long. After having determined the limit, it is interesting to find out the relationship between the position of vector $\overline{m}_A$ and its related phase components. Considering Figure 3.18, five different cases can be found out. When $\overline{m}_A$ is centred in the origin, all three leg duty-cycles have the same value which can be modified varying m_{0A} as shown in Figure 3.18a). In Figure 3.18b) is depicted the generic situation, when $\overline{m}_A$ is laying inside a sector. In this case all the three leg duty-cycles have different values. The modification of the common mode value means an integral translation of all three duty-cycles. The parameter m_{0A} is limited by the values making the maximum and the minimum duty-cycle to be equal to 1 and 0 respectively. Figure 3.18c) show the case of $\overline{m}_A$ laying on the border of the sector. Two leg duty-cycles assume the same value, while the third one is different. The gap between the two values is proportional to the vector amplitude. The case when the complex duty-cycle reaches the outer border is displayed in Figure 3.18d). One duty-cycle is equal to 1, another is equal to 0 and the third one can assume any value, but for any given position of $\overline{m}_A$ a single triplet m'_{1A}, m'_{2A} and m'_{3A} can exist. Finally, Figure 3.18e) shows the most constraining case, when $\overline{m}_A$ is laying on a vertex: in this situation the three leg duty-cycles can only be equal to 1 or 0 and two of them always coincide.

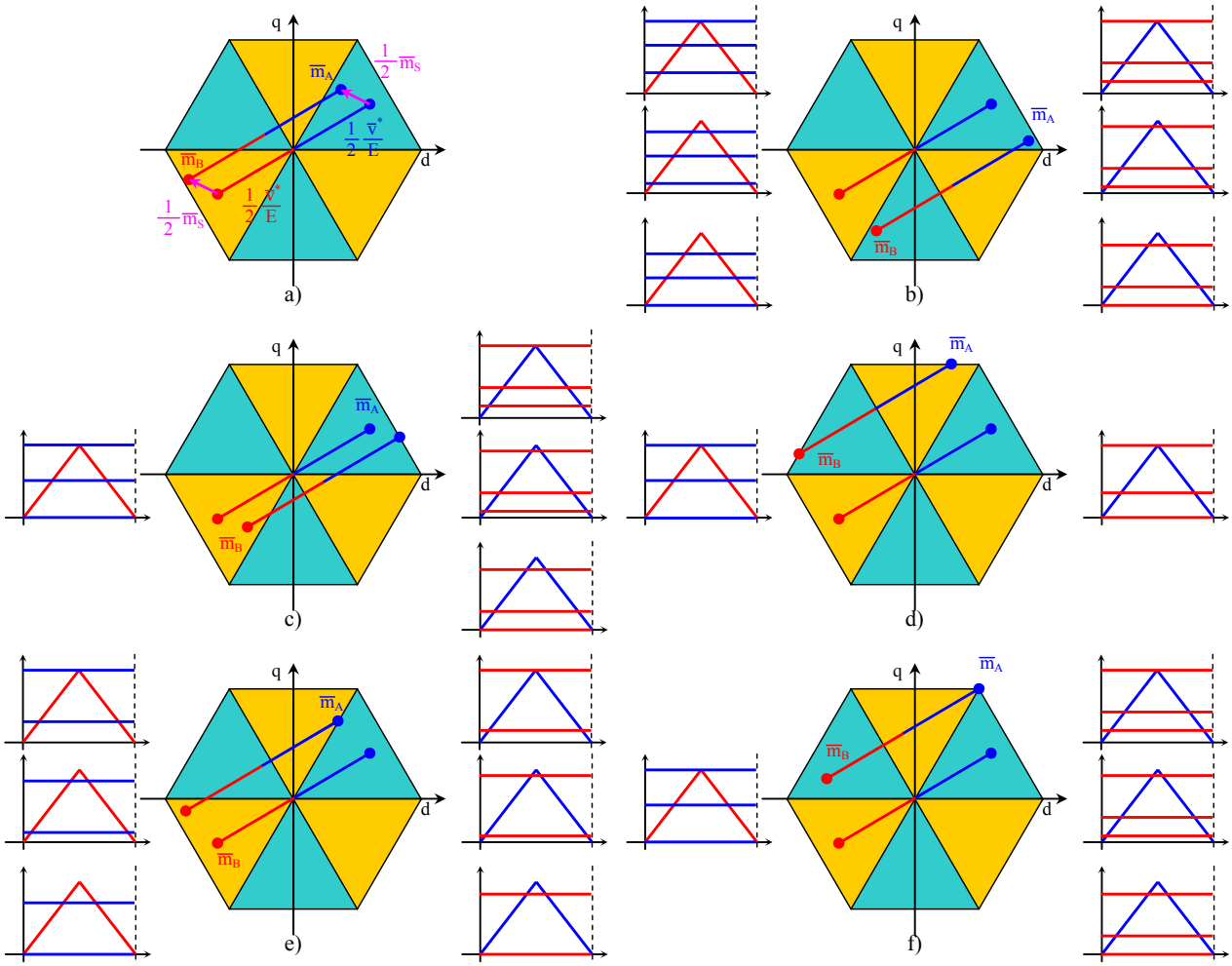


Figure 3.19: Effect of the complex degree of freedom and characterizations of inverters behaviours in main cases. a) The complex degree of freedom can be used to translate the base vector; b) Both complex duty-cycles are inside a sector; c) Inverter A duty-cycle in on the maximum limit; d) Both duty-cycles are on the maximum limit; e) Inverter A duty-cycle is on a sector border; f) Inverter A duty-cycle is on a vertex.

The same considerations can be applied even to inverter B, arriving to similar results. So for both 3-phase 2-level inverters the validity limits are given by two hexagons. To summarize everything in a single diagram, the two complex vectors $\overline{m}_A$ and $\overline{m}_B$ can be drawn in the same picture, like in Figure 3.19a). When the vector $\overline{m}_S$ is equal to zero, $\overline{m}_A$ and $\overline{m}_B$ have the same amplitude, but opposite directions.

$$\begin{cases} \overline{m}_A = +\frac{1}{2}\frac{\overline{v}^*}{E} \\ \overline{m}_B = -\frac{1}{2}\frac{\overline{v}^*}{E} \end{cases}. \qquad \textbf{(3.39)}$$

In Figure 3.19a) this case is shown: $\overline{m}_A$ and $\overline{m}_B$ are represented with one blue and one red dots, linked together by a line. Adding the vectors $\overline{m}_S$ to both of them means an integral translation on the d-q plane keeping their distance constant. So, using $\overline{m}_S$ it is possible to translate the line connecting the vectors to put them in particular positions inside the hexagon.

In Figure 3.19b) both vectors lay inside a sector. This means all the six leg duty-cycles assume different values as shown at sides of the picture. On the left side there are three possible situation for inverter A varying its common mode component m_{0A}, while on the right side there are three possible situations for inverter B varying m_{0B}.

Using $\overline{m}_S$, it is possible to shift $\overline{m}_A$ until it reaches the maximum limit as Figure 3.19c) shows. In this case there is no possibility to modify m_{0A}, while inverter B common mode component can vary until all the three leg duty-cycles assume values between 0 and 1.

Another interesting situation is depicted in Figure 3.19d) where both $\overline{m}_A$ and $\overline{m}_B$ have been translated on the limit: all the leg duty-cycles have fixed values and can not be translated using m_{0A} neither m_{0B}.

In Figure 3.19e), the complex vector $\overline{m}_A$ is superimposed to the border of a sector: this means two of its leg duty-cycles have the same value. However, both m_{0A} and m_{0B} can be used to translate the leg duty-cycles as shown at the sides of the picture.

Finally, Figure 3.19f) shows the last case in which the vector $\overline{m}_A$ is laying on a vertex: m_{0A} can not be varied while m_{0B} can be used to translate m'_{1B}, m'_{2B} and m'_{3B}.

3.3.3. Determination of DC bus currents

After the characterisation of the dual 2-level inverter has been done using $\overline{m}_A$, $\overline{m}_B$, m_{0A} and m_{0B}, the calculation of the currents flowing throughout the DC busses is possible. Considering Figure 3.20, it is possible to determine the inverter A DC current i_A applying Kirchhoff's current law to the positive pole. Considering the directions shown in the picture, (3.40) can be written.

$$i_A(t) = s_{1A}i_{1A} + s_{2A}i_{2A} + s_{3A}i_{3A} = s_{1A}i_1 + s_{2A}i_2 + s_{3A}i_3 . \qquad \textbf{(3.40)}$$

When the upper switch is conducting, the current flows from the positive pole to the phase whereas, when the lower switch is conducting, the current flows from the negative pole to the phase. So, only when the state of a leg is high the current of the corresponding phase contributes to the DC bus current. (3.40) can be integrated to determine the mean value over a period T_C.

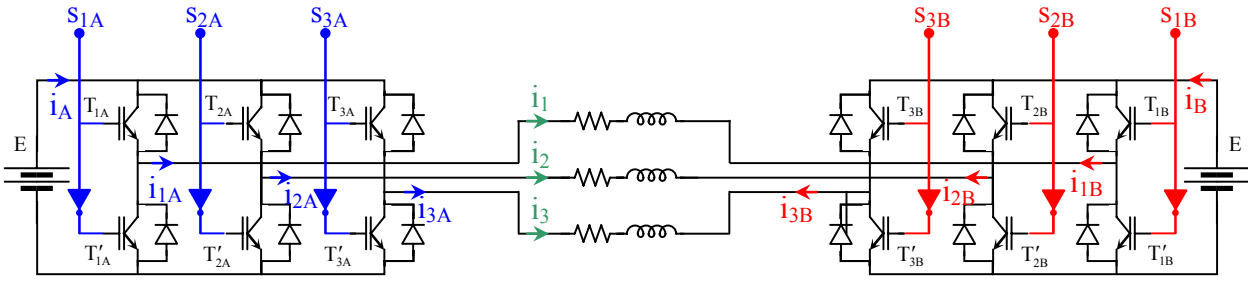


Figure 3.20: Determination of DC bus currents using complex duty-cycles.

$$I_A = \frac{1}{T_C}\int_0^{T_C} i_A(t)dt = \frac{1}{T_C}\int_0^{T_C}\left(s_{1A}i_{1A} + s_{2A}i_{2A} + s_{3A}i_{3A}\right)dt = m_{1A}i_1 + m_{2A}i_2 + m_{3A}i_3 . \quad \textbf{(3.41)}$$

Equation (3.41) is obtained in the hypothesis the current through the load can be considered constant during the integration period, so they can be taken out from the integral. Something similar can be done for inverter B, but it is necessary to be careful about the signs of the currents.

$$i_B(t) = s_{1B}i_{1B} + s_{2B}i_{2B} + s_{3B}i_{3B} = -s_{1B}i_1 - s_{2B}i_2 - s_{3B}i_3 . \quad \textbf{(3.42)}$$

Similarly to inverter A, even for inverter B can be calculated the mean value of DC bus current integrating (3.42) during a period.

$$I_B = \frac{1}{T_C}\int_0^{T_C} i_B(t)dt = -\left(m_{1A}i_1 + m_{2A}i_2 + m_{3A}i_3\right). \quad \textbf{(3.43)}$$

To conclude, substituting (3.33) in (3.41) and (3.43), two general equation can be found which tie the mean currents to the complex duty-cycles.

$$\begin{cases} I_A = m_{0A}\left(i_1 + i_2 + i_3\right) + \dfrac{\bar{v}^*}{E}\cdot\left(i_1 e^{j0} + i_2 e^{j\frac{2}{3}\pi} + i_3 e^{j\frac{4}{3}\pi}\right) \\ I_B = -m_{0B}\left(i_1 + i_2 + i_3\right) + \dfrac{\bar{v}^*}{E}\cdot\left(i_1 e^{j0} + i_2 e^{j\frac{2}{3}\pi} + i_3 e^{j\frac{4}{3}\pi}\right) \end{cases} . \quad \textbf{(3.44)}$$

In the case the common mode current is not allowed to flow, (3.44) show how symmetric is the dual 2-level inverter is if properly modulated. Anyway, this kind of mathematical treatment is analysed thoroughly in [77], even if in that paper it is related to a 3-level 3-phase cascade H-bridge converter.

Chapter 4

Analogue modulation

4.1. Introduction

4.1.1. Overview

The simplest way to control the dual 2-level inverter is to use analogue modulation strategies. Due to their simplicity, analogue modulations have been the first approach used in simulations of the structure. Analog modulations are based on the principle to reconstruct the mean value of the desired output during a defined period T_S as Figure 4.1a) shows. The red line is the output needed while the stepped blue line is the given output reconstructed using 0-order holder. The red and the blue signals of Figure 4.1a) have in common the area subtended which can be demonstrated to be proportional to the mean value.

Usually the reconstruction of the desired signal is made using the comparison between a reference and a carrier. Considering Figure 4.1b), the red signal is called **reference** and it is equal to the desired voltage. Anyway the reference needs only to be proportional to the output. The green signal is called **carrier**. The carrier can have several shapes, but the most common is the triangular one, as shown in Figure 4.1b). As happen for the reference, even the carrier is allowed not to sweep from zero to the maximum voltage, but the proportionality coefficient of the reference and the carrier must be the same.

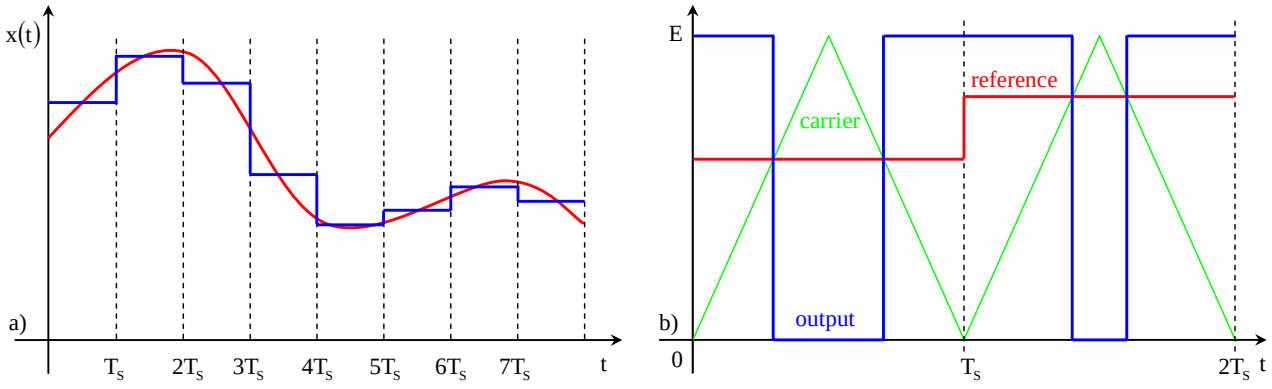


Figure 4.1: Generation of the voltage output using analogue techniques. a) Signal sampling; b) Mean value reconstruction.

The output must be zero when the reference is smaller than the carrier and it must be equal to the maximum available voltage when the reference is greater than the carrier. In this way it can be demonstrated that reference and output have the same mean value.

4.1.2. Classification

There are six legs in the structure of the dual 2-level inverter, as Figure 4.2 shows. All the legs can produce an output voltage equal to zero or to the DC bus voltage, so the outputs assume the same values when both DC busses have the same voltage.

In this way, if the determination of the DC current is not necessary, it is possible to get free from the physical connections and consider three separated H-bridges or two 3-phase inverters. This concept is highlighted in Figure 4.2 considering the two groupings made by the three red lines or by the two blue ones. In any case, one reference for each leg is needed to obtain the proper gating signals. Depending on how the structure is considered, the determination of the phase references is different and leads to different harmonic contents of the output. For all the presented modulations, both **Sinusoidal PWM** (considering three separated H-bridge) and **Generalized PWM** (considering the interconnections among the phases) are discussed.

The first implementation of the control was made considering the converter composed by three independent H-bridge converters each one modulated using a standard 3-level modulation based on triangular shaped carriers. All the multilevel modulation presented in Chapter 2 can be used for this purpose. Another modulation has been developed from the idea to make one inverter commutate using a six-step modulation. The other inverter has to synthesise the difference between the reference and the output of the first converter using a high switching frequency modulation. Moreover, due to the particular shape of the carrier, the two inverters can switch their roles to balance the delivered powers.

In the following several analogue modulation strategies will be presented together to a brief description of their implementation. Moreover, some simulation results will be shown and commented to prove the effectiveness of these modulations. On the basis on what has been said above, analogue modulation strategies will be subdivided in two classes: the modulations which exploit one or more triangular shaped carriers and the modulations using carriers with queer waveforms.

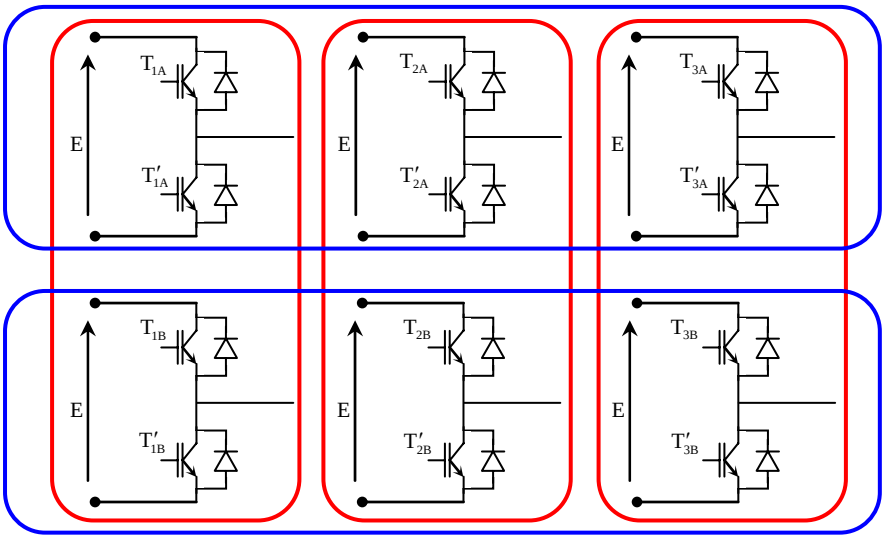


Figure 4.2: Groupings of the legs to highlight the three H-bridges (red lines) or the two 3-phase inverters (blue lines).

4.2. Triangular carrier based modulations

4.2.1. Double reference

The easier way to modulate a H-bridge converter to obtain a 3-level output is to use a single carrier and two references, each one equal to half the voltage desired in the cycle. Considering Figure 4.3a), (4.1) can be written in the hypothesis the two negative poles of battery banks have the same potential.

$$v = e_A - e_B . \tag{4.1}$$

The same has to happen for the instantaneous references: the total reference v^* must be equal to the difference between the references of the two legs, e_A^* and e_B^*, in each instant.

$$v^* = e_A^* - e_B^* . \tag{4.2}$$

If a value for e_A^* was chosen, the reference e_B^* would be still determined for any given v^*. In particular, in the case e_A^* is equal to half v^*, (4.3) can univocally be asserted.

$$\begin{cases} e_A^* = \dfrac{v^*}{2} \\ e_B^* = -\dfrac{v^*}{2} \end{cases} . \tag{4.3}$$

So, from (4.3), it can be seen that the two references have the same amplitude, but they have opposite signs.

To prove the effectiveness of the modulation strategy, the converter has been demanded for a symmetrical 3-phase voltage. In Figure 4.3b), the references for a single phase are depicted: the green one is the total reference, the blue one is upper leg reference and the red one is lower leg reference. The azure triangular waveform is the carrier which sweeps from -1 to +1 for convenience. This means that each leg will give the maximum output voltage when its reference is equal to 1 whereas it will give a null output when its reference is equal to -1. So, the total reference can assume any value between -2 and 2, being the leg reference equal to its half.

Some simulations have been done using a triangular carrier at 10 kHz with three different reference values: 0.5, 1 and 2. With a reference equal to 0.5, the output required is surely included

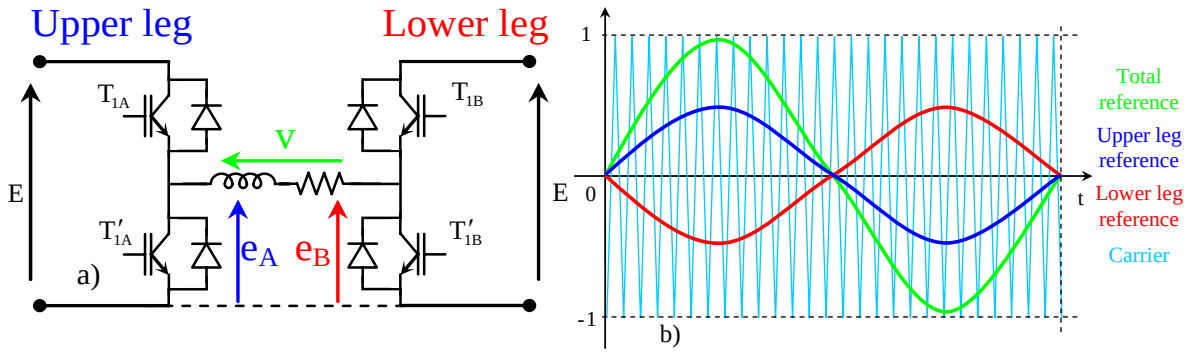


Figure 4.3: H-bridge 3-level modulation using two references. a) Circuit topology and voltages; b) References and carrier used to generate the output.

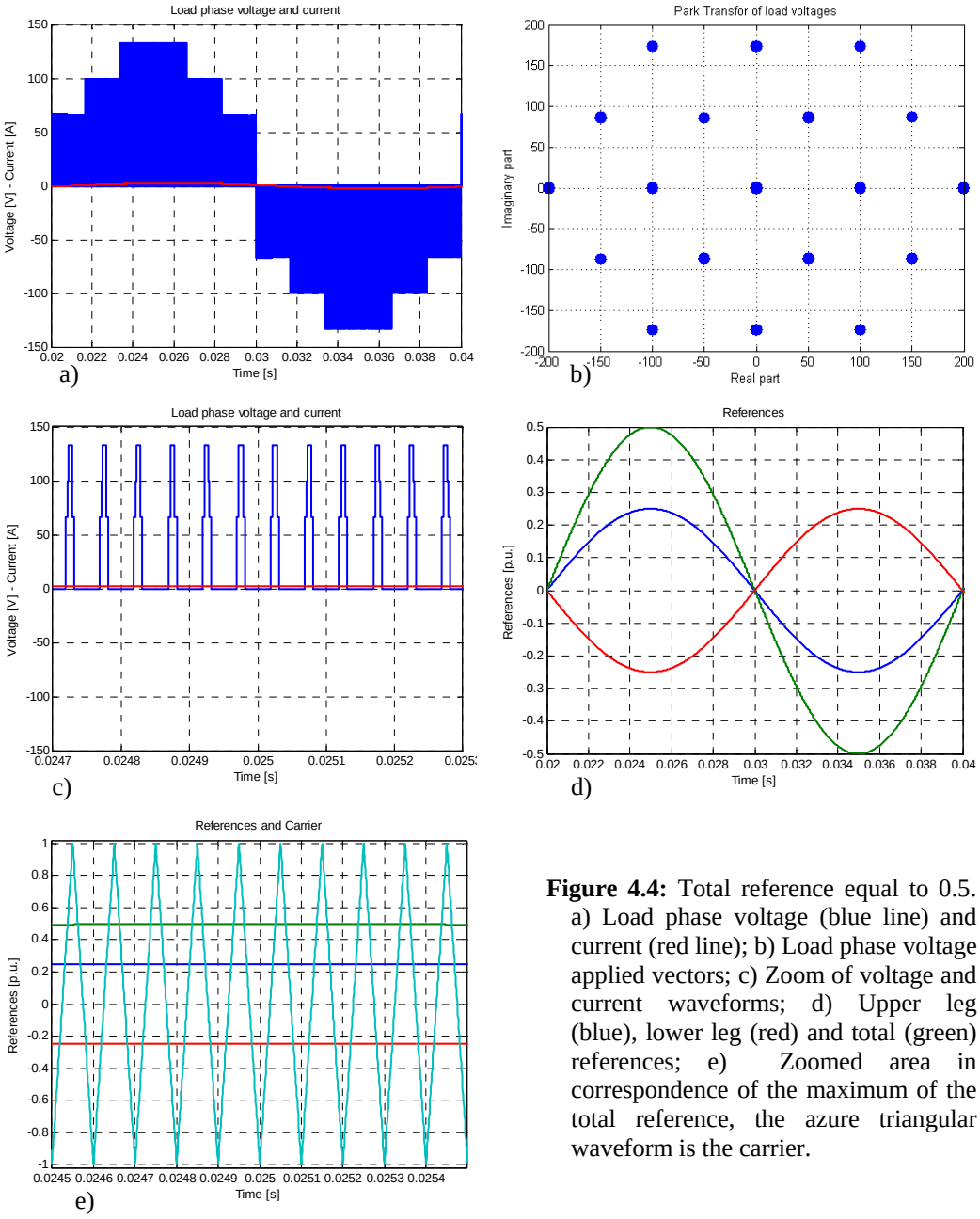


Figure 4.4: Total reference equal to 0.5. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) and total (green) references; e) Zoomed area in correspondence of the maximum of the total reference, the azure triangular waveform is the carrier.

in the inner hexagon, so there is no need to use outer voltage vectors. Unfortunately, this modulation does not synchronize the commutations of the two inverters and the voltage waveform it produces for one load phase can be seen in Figure 4.4a). Figure 4.4b) highlight this problem showing Park's transform of the load phase voltages: it can be clearly seen that all voltage vectors are applied even if only the inner ones are strictly needed. Moreover Figure 4.4c) shows a zoomed area in correspondence of the maximum value of the total reference: obviously the output voltage is synthesised using all the possible positive voltage levels invalidating a proper multilevel modulation.

The references the converter is demanded for are shown in Figure 4.4d). The green one is the total reference and it is a pure sinusoidal wave with amplitude of 0.5 over a maximum of 2. The blue line is the upper leg reference: it is equal to half the total reference with the same phase. The red line in phase opposition is the lower leg reference. Moreover in Figure 4.4e) a zoomed area in correspondence of the maximum value of the total reference is depicted. It clearly shows there is no overmodulation, so the converter works in linear zone as expected.

To conclude the comment to the AC side waveforms, Table 4.1 shows RMS and THD of the load voltage and current. The voltage THD appears to be very good for an open-loop control at low modulation index like in this case.

Load phase voltage	
RMS	38.0549 V
THD	1.9108
Load phase current	
RMS	1.6836 A
THD	0.011891

Table 4.1: Load phase voltage and current RMS and THD with a total reference of 0.5.

Regarding DC busses, some consideration can be done about the input currents and the common mode voltage between the negative poles. Figure 4.5a) shows the DC bus currents of the two inverters: obviously they are discontinuous depending on the state of the legs. The low frequency currents spectra are depicted in Figure 4.5b). Because the voltage sources are ideal DC sources, their output voltage does not change, so the delivered power can be assumed to be proportional to the current, that is the DC bus powers and their current waveforms are similar. As it can be seen from Figure 4.5b), the control makes some fluctuation at low frequencies on the delivered power.

The common mode voltage is shown in Figure 4.5c). Its waveform never overcame an absolute value of 35 V. So it has been preferred to plot a zoomed area to better see the voltage level assumed by the common mode voltage. Figure 4.5d) shows the common mode voltage spectrum and

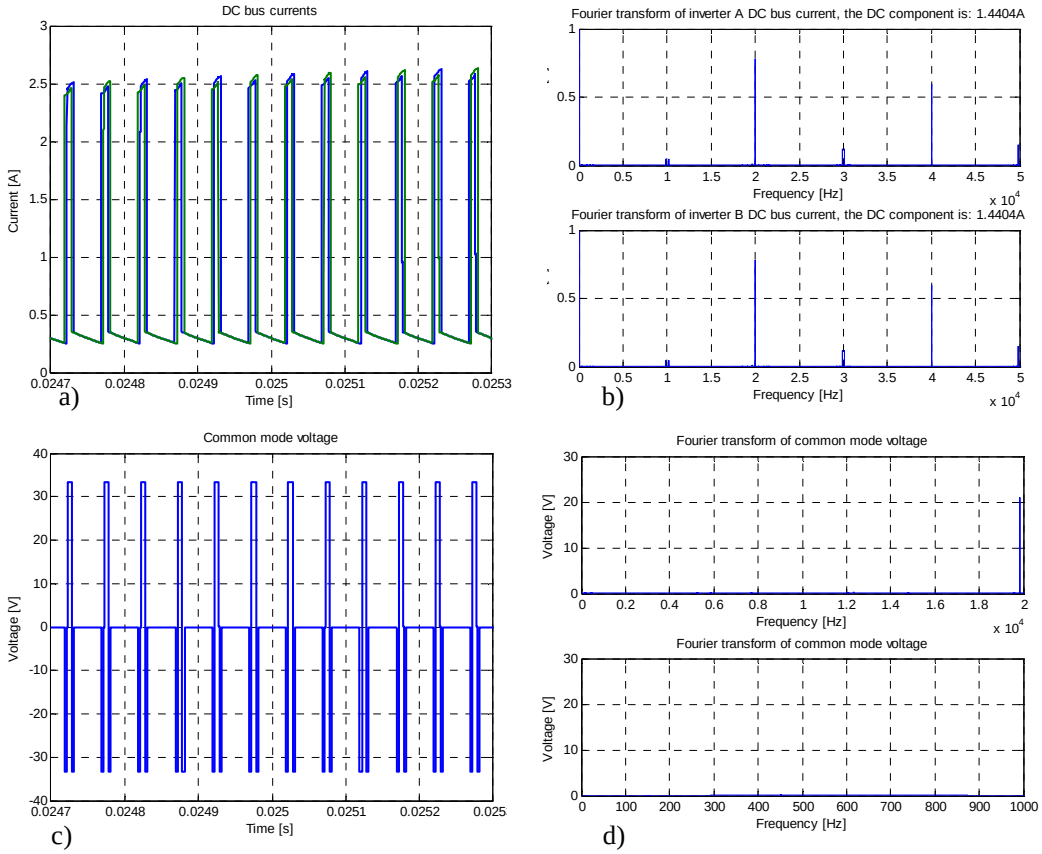


Figure 4.5: Waveforms related to the DC busses with a total reference equal to 0.5. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

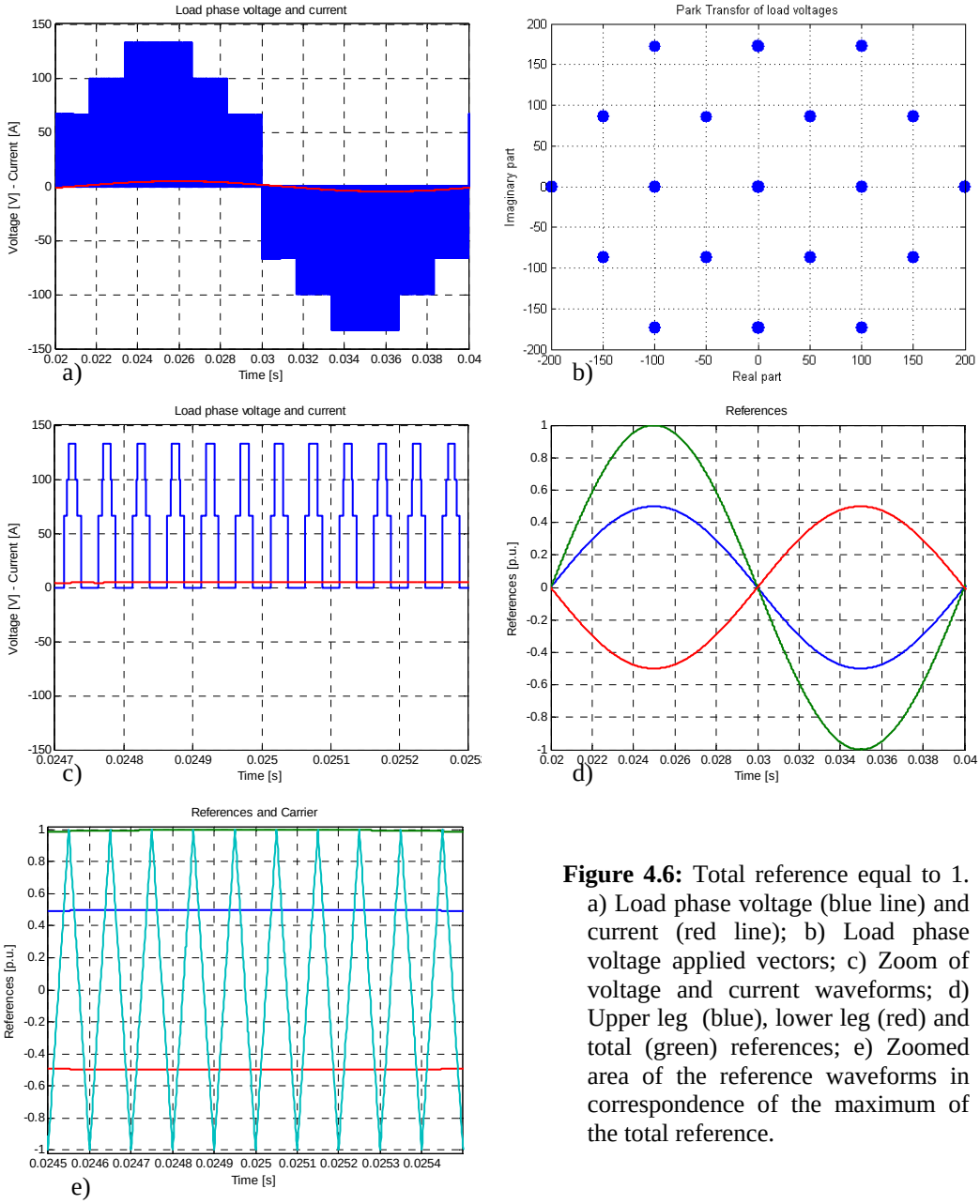


Figure 4.6: Total reference equal to 1. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) and total (green) references; e) Zoomed area of the reference waveforms in correspondence of the maximum of the total reference.

highlights the low frequency harmonics: there are no harmonics before 20 kHz. Even 10 kHz harmonic, which corresponds to the switching frequency, does not exist. This is due to the particular modulation which exploits two references: in this way each leg commutates at 10 kHz, but the mutual effect makes the load phase voltage to commutate at 20 kHz.

Another simulation has been conducted with a total reference equal to 1. Figure 4.6a) shows the load phase voltage and current waveforms. Even in this case the greatest voltage levels are not strictly needed to synthesise the required voltage, but they are still applied. The same concept can be inferred considering Figure 4.6b) which represents the applied voltage vectors: the most outer vectors are used even if they are not necessary. Moreover, looking at Figure 4.6c) the load phase output voltage is always modulated applying even null voltage as well as previous case: this decrease a lot the quality of the output waveform. In Figure 4.6d) the three references are depicted and to prove the modulation is in the linear region. Figure 4.6e) shows the three references in the time window centred on the maximum value of the total reference: both upper and lower leg references are contained between the outermost points of the carrier.

Table 4.2 shows RMS and THD of the load voltage and current. The voltage THD is decreasing in the respect of the previous one. The decrement is quite significant and it is expected to better more and more increasing the reference.

Load phase voltage	
RMS	53.7971 V
THD	1.1505
Load phase current	
RMS	3.367 A
THD	0.0086375

Table 4.2: Load phase voltage and current RMS and THD with a total reference of 1.

The bus DC current waveforms are depicted in Figure 4.7a). They are very close to the correspondent waveforms obtained in the previous case, but their average values are greater. The DC currents low frequencies spectra are depicted in Figure 4.7b), the upper picture is related to inverter A while the lower one concerns inverter B. It can be noted a general increment of harmonic magnitudes. The common mode voltage amplitude is still contained in 35 V as Figure 4.7c) shows. Comparing Figure 4.7d) with Figure 4.5d), it is clear the 20 kHz is decreased to a quarter and the low frequency harmonics are neither present.

Even a simulation with a total reference equal to 2 has been done. The results of the simulation

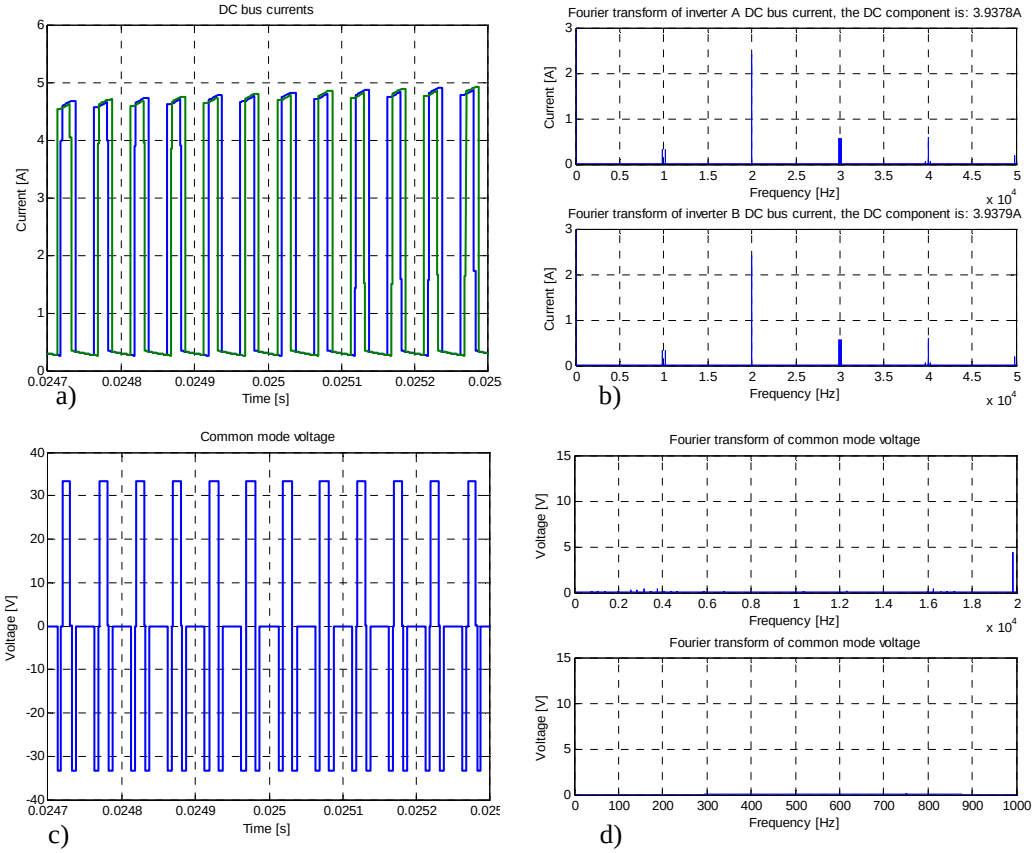


Figure 4.7: Waveforms related to the DC busses with a total reference equal to 1. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

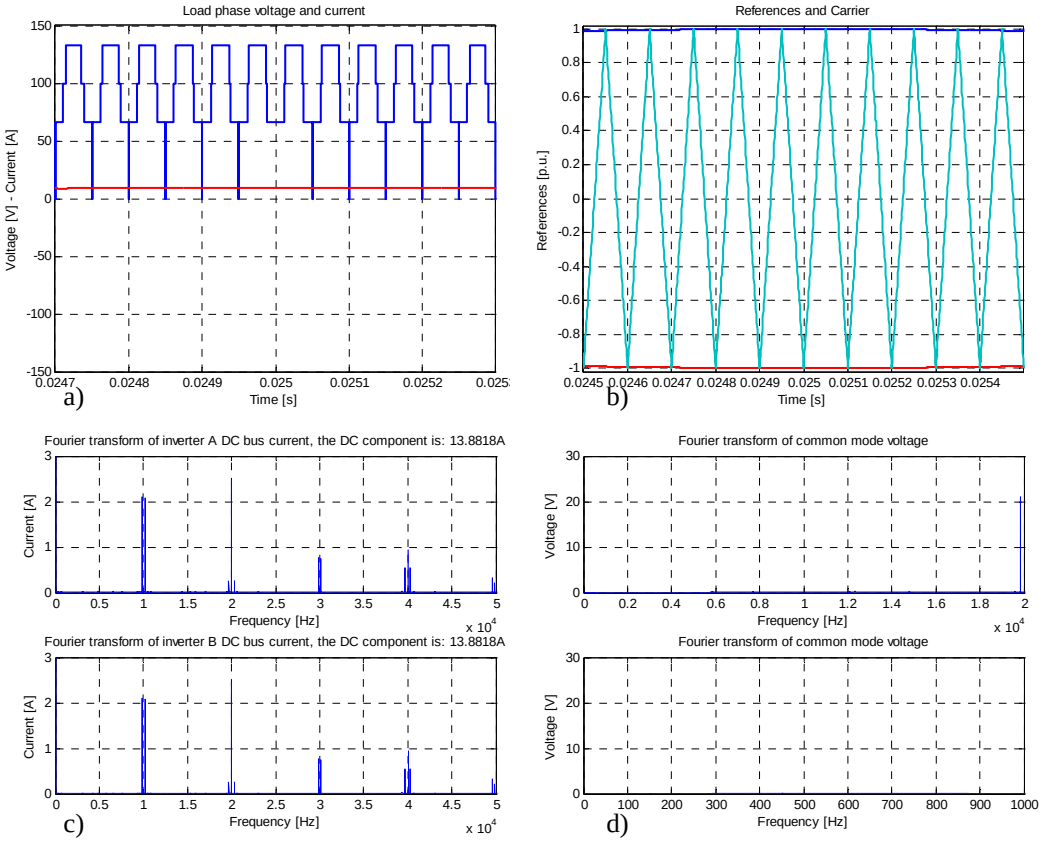


Figure 4.8: Total reference equal to 2. a) Load phase voltage (blue) and current (red) waveforms in the interval centred on the maximum of the total reference; b) Upper leg (blue) and lower leg (red) references compared to the carrier (azure); c) DC currents low frequencies spectra; d) Common mode voltage spectrum at high and low frequencies.

are quite similar to the others. In Figure 4.8a) the load voltage and current waveforms are depicted. They are clearly greater than in the previous cases. Considering upper and lower leg references presented in Figure 4.8b), it can be noted that they are on the verge of carrier extreme points in correspondence of their maximums meaning the limits of the linear zone have almost been reached. Figure 4.8c) shows the DC currents spectra with a quite high harmonic content. The common mode voltage whose high frequencies and low frequencies spectra are depicted in Figure 4.8d) has a waveform very close to the previous cases, with the first fundamental at 20 kHz.

Table 4.3 gives the load voltage and current RMS and THD values. In particular, the THD values are decreased as predicted. The THD can be considered even too small, but all the conducted simulations have been done without dead time which heavily worsen the voltage distortions.

Load phase voltage	
RMS	76.0221 V
THD	0.40011
Load phase current	
RMS	6.7338 A
THD	0.002377

Table 4.3: Load phase voltage and current RMS and THD with a total reference of 2.

The simulations commented have used a sinusoidal pulse width modulator, so the maximum voltage amplitude is limited to half the DC bus voltage for a standard 3-phase inverter. For the presented topology, this maximum limits is overcame because two DC sources are available: a

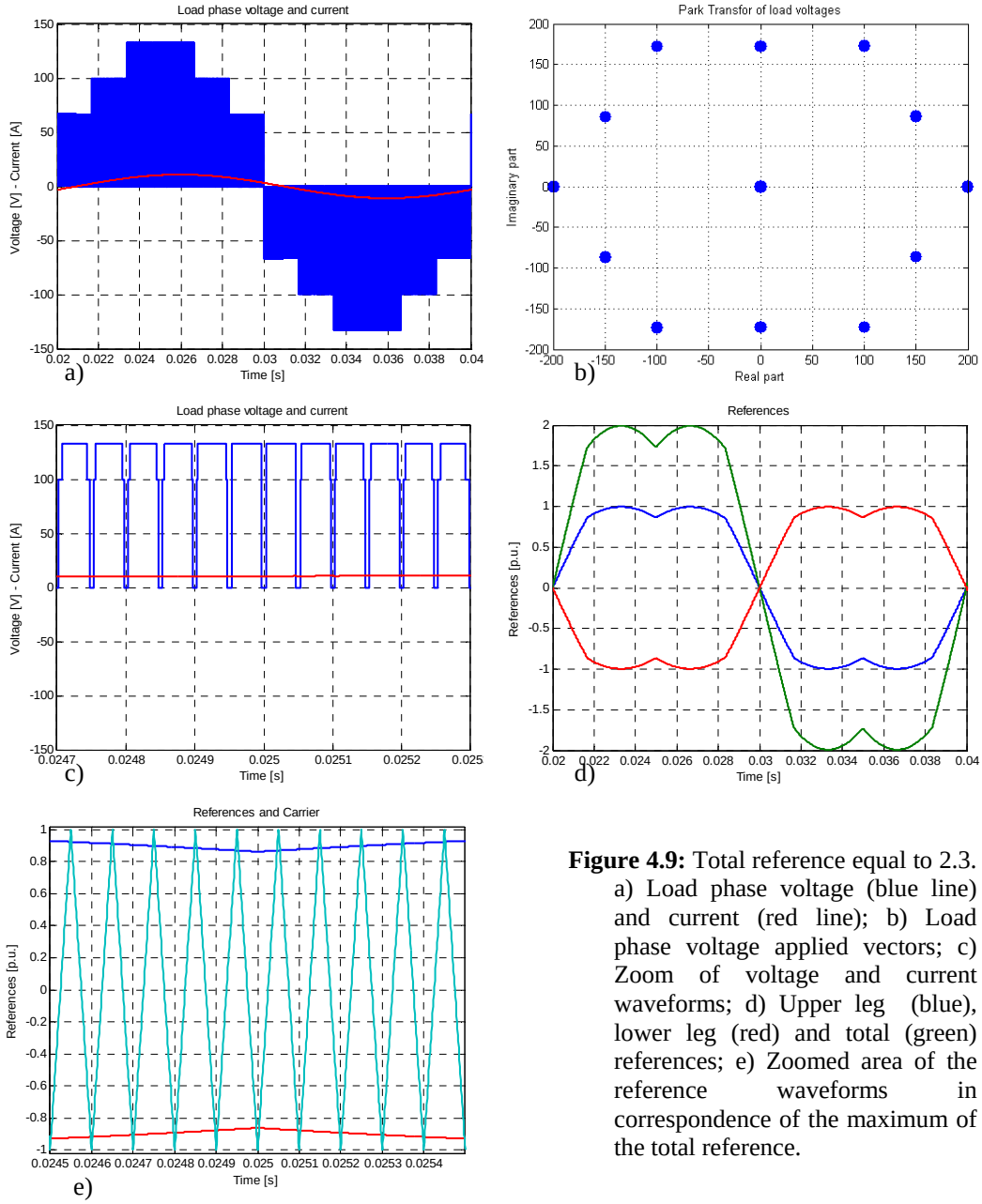


Figure 4.9: Total reference equal to 2.3. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) and total (green) references; e) Zoomed area of the reference waveforms in correspondence of the maximum of the total reference.

sinusoidal modulator can produce a sinusoidal voltage with maximum amplitude equal to the voltage of one DC source as RMS value in Table 4.3 indicates. A **Generalized PWM** (**GPWM**) has been implemented to better exploit the DC busses. With this control, the total reference can be increased of a factor $2/\sqrt{3}$ still remaining in linear region.

Figure 4.9a) shows load phase voltage and current waveforms. Even using SVPMW several positive voltage levels are used to synthesise the positive half-wave, while several negative voltage levels are used for the negative half-wave. Park's transform of load voltages is depicted in Figure 4.9b). Only the outermost vectors and the null one are applied, but the dual 2-level inverter is not yet used properly. In Figure 4.9c), load voltage and current are shown in a restricted time window to better appreciate the voltage levels used when the total reference has its maximum value.

The GPWM does not use a simple sinusoidal waveform as a reference, but something a bit more complicated as Figure 4.9d) highlights. Even in this case, looking at Figure 4.9e), it is possible to assert the converter works in linear region because the references are still contained between carrier peaks, but it is able to supply higher voltage than using a **Sinusoidal PWM** (**SPWM**).

As well as for SPWM simulation, Table 4.4 bear the evidence of a good THD of the load voltage. Obviously, the load current present an even smaller distortion due to the filtering capability of the load.

Load phase voltage	
RMS	85.4235 V
THD	0.32797
Load phase current	
RMS	7.7438 A
THD	0.00192

Table 4.4: Load phase voltage and current RMS and THD with a total reference of 2.3.

To conclude the description of this modulation technique, something can be written about the DC voltage and currents. Figure 4.10a) shows the DC currents flowing through the two DC busses

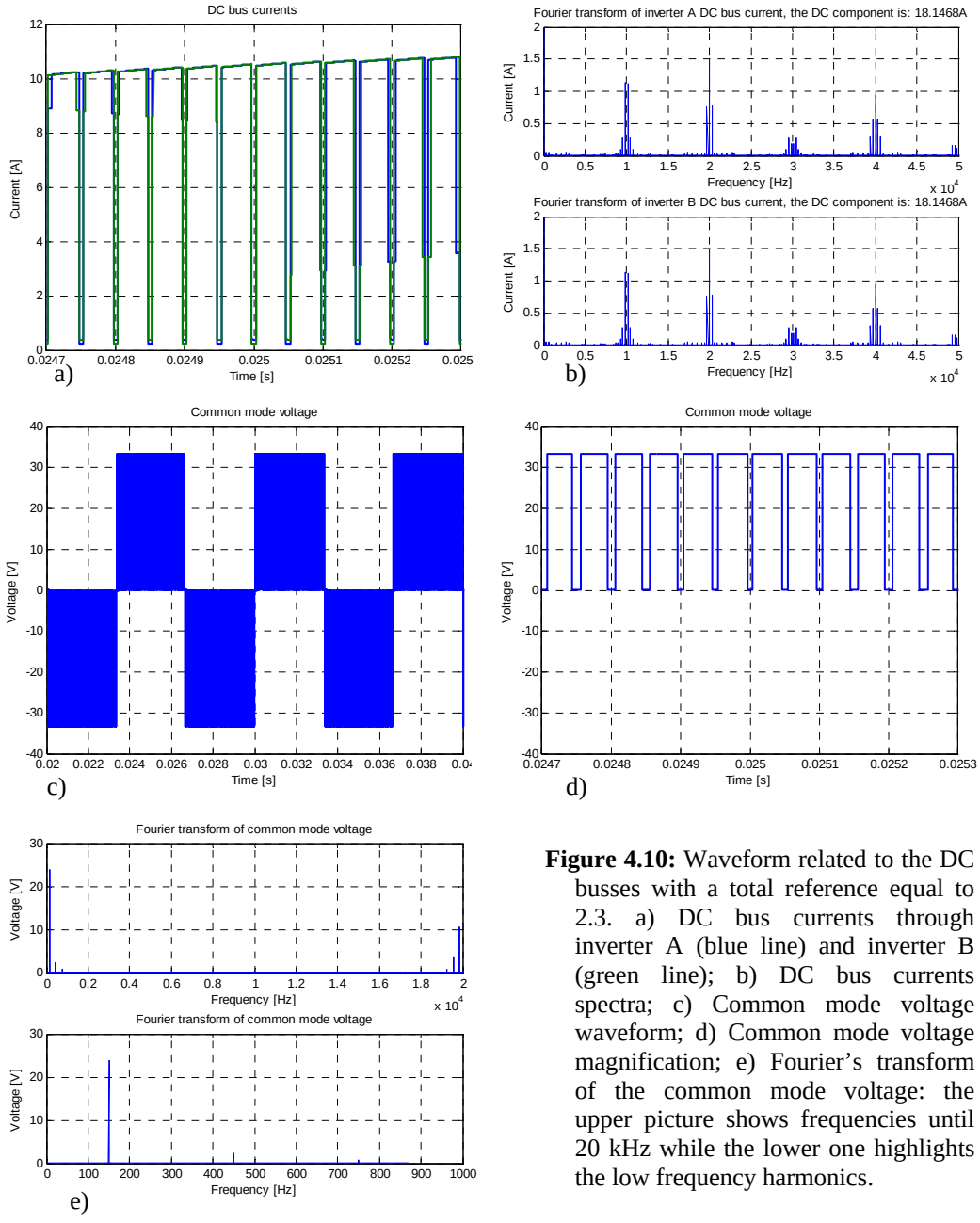


Figure 4.10: Waveform related to the DC busses with a total reference equal to 2.3. a) DC bus currents through inverter A (blue line) and inverter B (green line); b) DC bus currents spectra; c) Common mode voltage waveform; d) Common mode voltage magnification; e) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency harmonics.

and Figure 4.10b) depicts their spectra. Using a GPWM instead of a SPWM shift the harmonics to higher frequencies: indeed the greatest harmonic content is over the 10 kHz and not at low frequencies. Figure 4.10c) shows the common mode voltage waveform, which is quite different now: a 50 Hz component can be clearly seen. Figure 4.10d) shows a magnification of the common mode voltage in correspondence of total reference maximum: the common mode voltage is modulated using two voltage levels only. The high frequencies and low frequencies spectra in Figure 4.10e) clearly highlight the presence of these harmonics, which there were not using a SPWM.

4.2.2. Two carriers

Another way to achieve multilevel modulation is to use a modulator with two carriers, one associated to the upper leg and another one associated to the lower leg. Figure 4.11 shows how the two carrier are disposed. The upper leg carrier is a triangular wave sweeping from 0.5 to 1, while the lower leg carrier goes from 0 to 0.5. In this way, only one leg commutates at one time and the total output is given by the overall effects of both legs. With the representation of Figure 4.11, the output is obtained as the sum of the single leg outputs, so the gating signals of the lower leg must be neglected to achieve (4.1) which is still valid.

There are several dispositions of the carrier different from the one presented in Figure 4.11 which is the most intuitive. Accordingly with Chapter 2, the carriers in Figure 4.11 are in Phase Disposition, but even a Phase Opposition Disposition can be used. The difference between the two choices can be seen in the harmonic spectra but this comparative analysis is beyond the purposes of this chapter.

Some simulations have been conducted considering either a SPWM and a GPWM, using references giving the same output voltages as in the previous case. Using the carriers shown in Figure 4.11, the reference 0.25, 0.5, 1 and 1.15 have been used to achieve the same output conditions. The last reference can be applied only using a GPWM, while the converter can be demanded for the others with both modulator types: similarly to the previous case, standard SPWM is used in the first three simulations.

Considering a reference equal to 0.25, Figure 4.12a) shows the load phase voltage and current. A smaller number of voltage level is used if compared with Figure 4.4a) even if the same output voltage is demanded. The same concept can be derived from the comparison between Figure 4.12b) and Figure 4.4b): using two carriers only the inner active vectors are used to synthesise the desired output, while the two reference modulation involves several outermost vectors. Considering Figure 4.12c), the magnification of the load voltage clearly put in evidence the converter modulate using only three adjacent levels achieving a better multilevel modulation. Figure 4.12d) depicts the

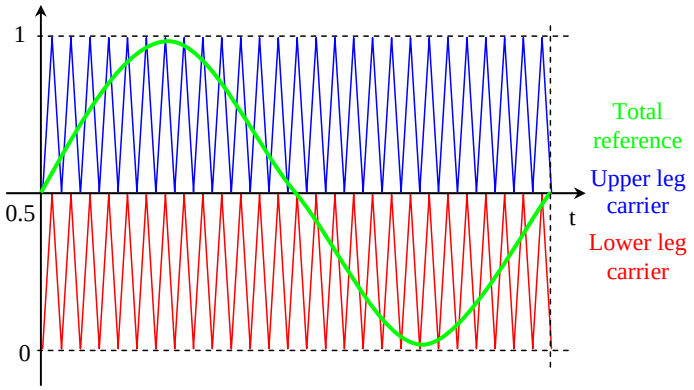


Figure 4.11: H-bridge 3-level modulation using two carriers. Total reference and carriers used to generate the output.

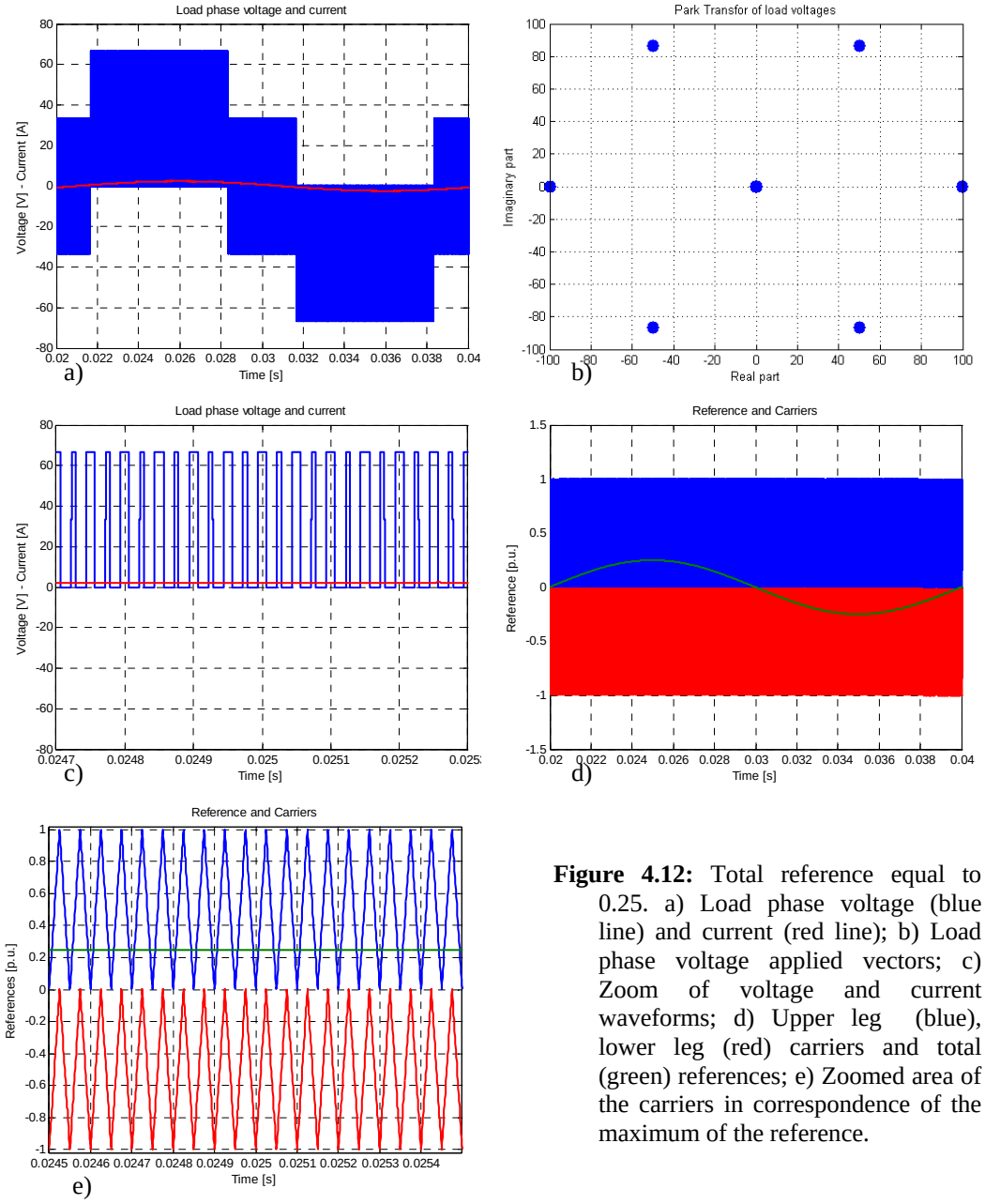


Figure 4.12: Total reference equal to 0.25. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) carriers and total (green) references; e) Zoomed area of the carriers in correspondence of the maximum of the reference.

situation concerning carriers and reference. The two carriers are clearly visible and the reference is contained in between the furthest points of the carriers meaning the modulation is in the linear zone.

Table 4.5 reports the RMS and THD for the load phase voltage and current. Comparing this with Table 4.1 it is evident there are smaller values of voltage RMS and THD due to the better

Load phase voltage	
RMS	30.2936 V
THD	1.3955
Load phase current	
RMS	1.6835 A
THD	0.0063318

Table 4.5: Load Phase voltage and current RMS and THD with a reference of 0.25.

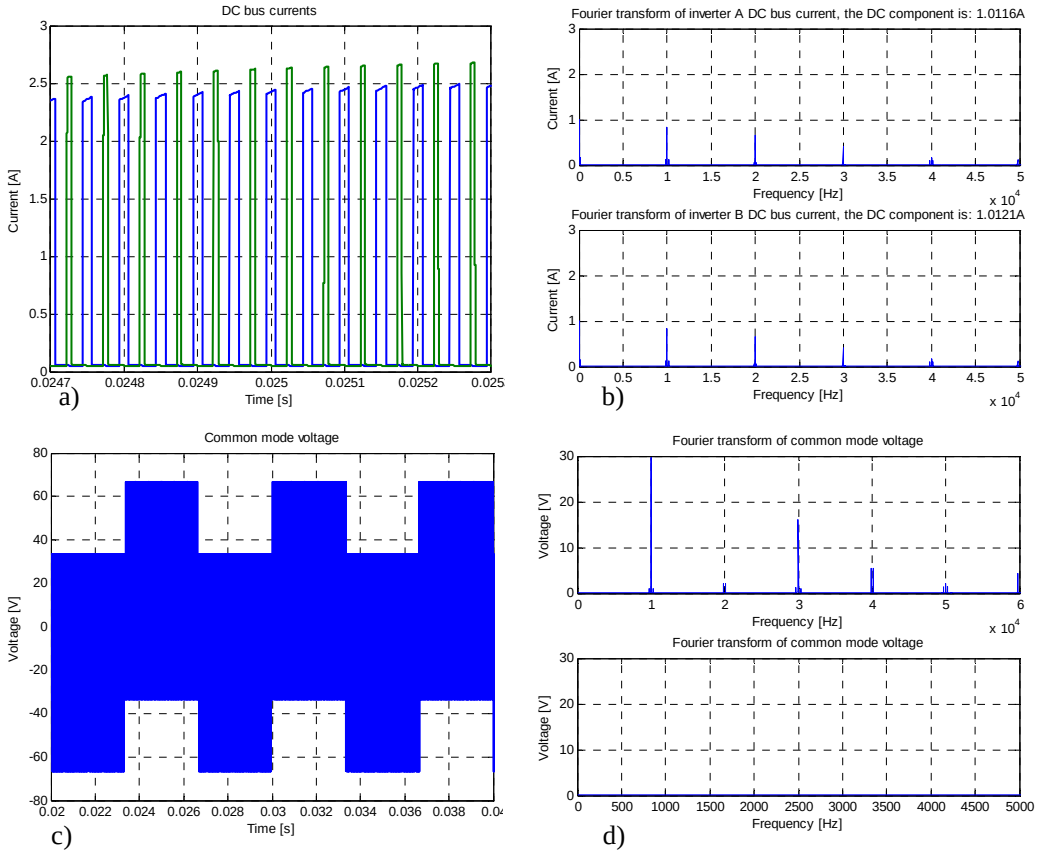


Figure 4.13: Waveforms related to DC busses with a reference equal to 0.25. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

modulation obtained using two carriers.

Regarding DC bus waveforms, it is clear the behaviour of the currents is different depending on the instantaneous value of the reference. As Figure 4.13a) highlights, this mean that there will be time intervals in which the highest average current is flowing through inverter A while in other intervals the highest current will be flowing through inverter B. Anyway considering a whole output fundamental period, the average currents through inverters A and B are the same. Moreover, DC currents have the same spectra as it is possible to see in Figure 4.13b). Common mode voltage, depicted in Figure 4.13c) has fundamental component at 10 kHz even if it may appear to be different. Anyway, Figure 4.13d) shows common mode voltage spectrum and it is evident there are no components at low frequencies. Comparing Figure 4.13d) with Figure 4.5d) it can be easily noted one harmonic at the switching frequency appears in the spectrum of this last kind of modulator common mode voltage while the spectrum of the common mode voltage using two references was deprived of this.

Results of the simulation using a reference equal to 0.5 are presented in Figure 4.14. Figure 4.14a) shows the waveforms of the load phase voltage and current. Figure 4.14b) depicts the voltage vectors applied to the load: only the inner vectors are used as expected in a multilevel modulation. Load phase voltage and current waveforms are even shown in Figure 4.14c) where a magnification of the time scale highlights the commutations of the output showing that only three voltage level are involved in the generation of the maximum voltage. Reference and carriers in Figure 4.14d) and e) reveals the modulation is still in linear zone like previous cases.

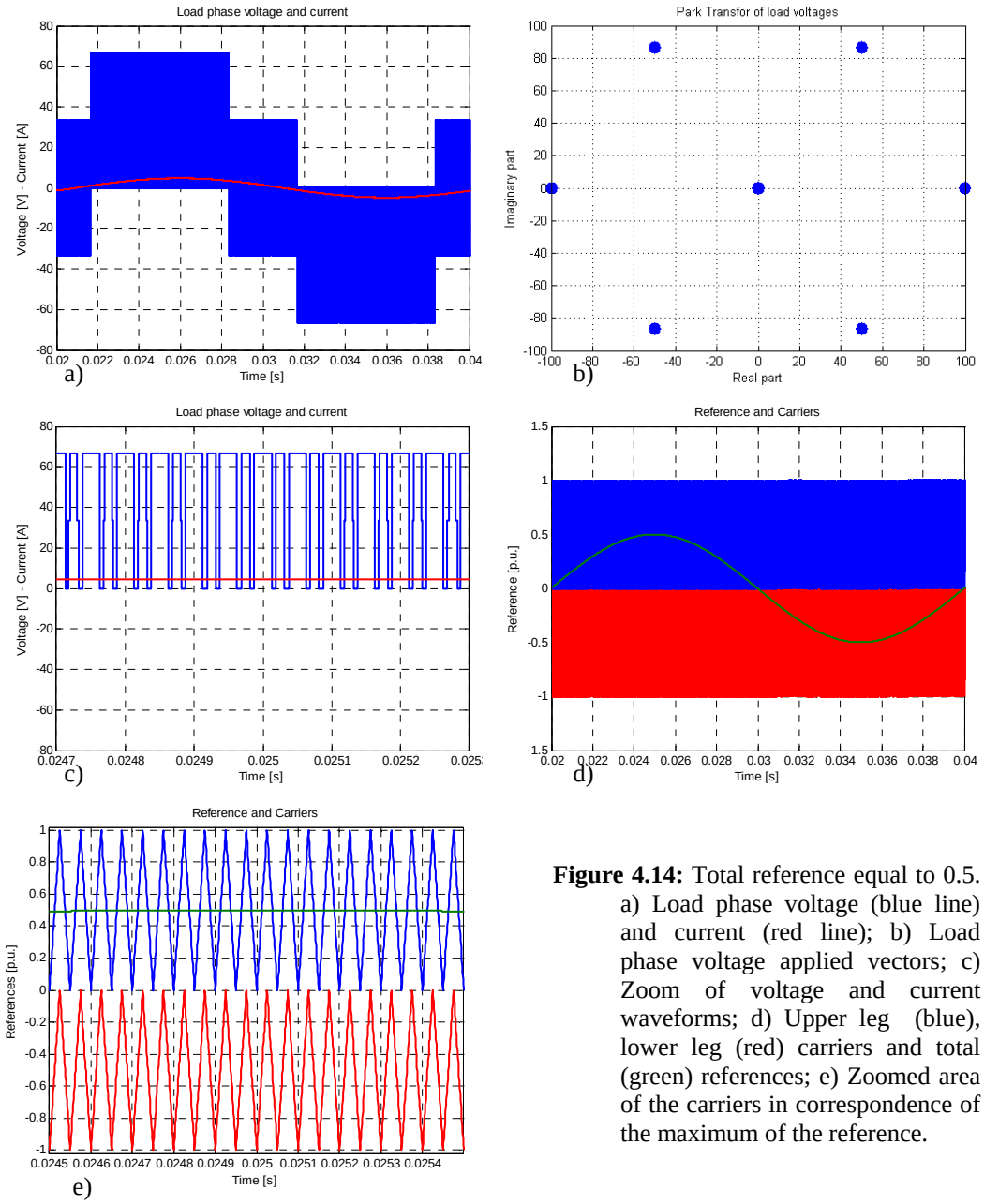


Figure 4.14: Total reference equal to 0.5. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) carriers and total (green) references; e) Zoomed area of the carriers in correspondence of the maximum of the reference.

Table 4.6 reports the RMS and THD of load phase voltage and current. There is an increment of converter performances as expected because the reference is greater and it can be synthesised in a better way exploiting the whole voltage level.

Load phase voltage	
RMS	42.8156 V
THD	0.68694
Load phase current	
RMS	3.3669 A
THD	0.0034495

Table 4.6: Load Phase voltage and current RMS and THD with a reference of 0.5.

As happened in all other cases, it is interesting to get some information about the DC side waveforms. The DC currents are reported in Figure 4.15a). As the previous case, the currents have different shapes, but the harmonic contents are equal as Figure 4.15b) shows. The common mode

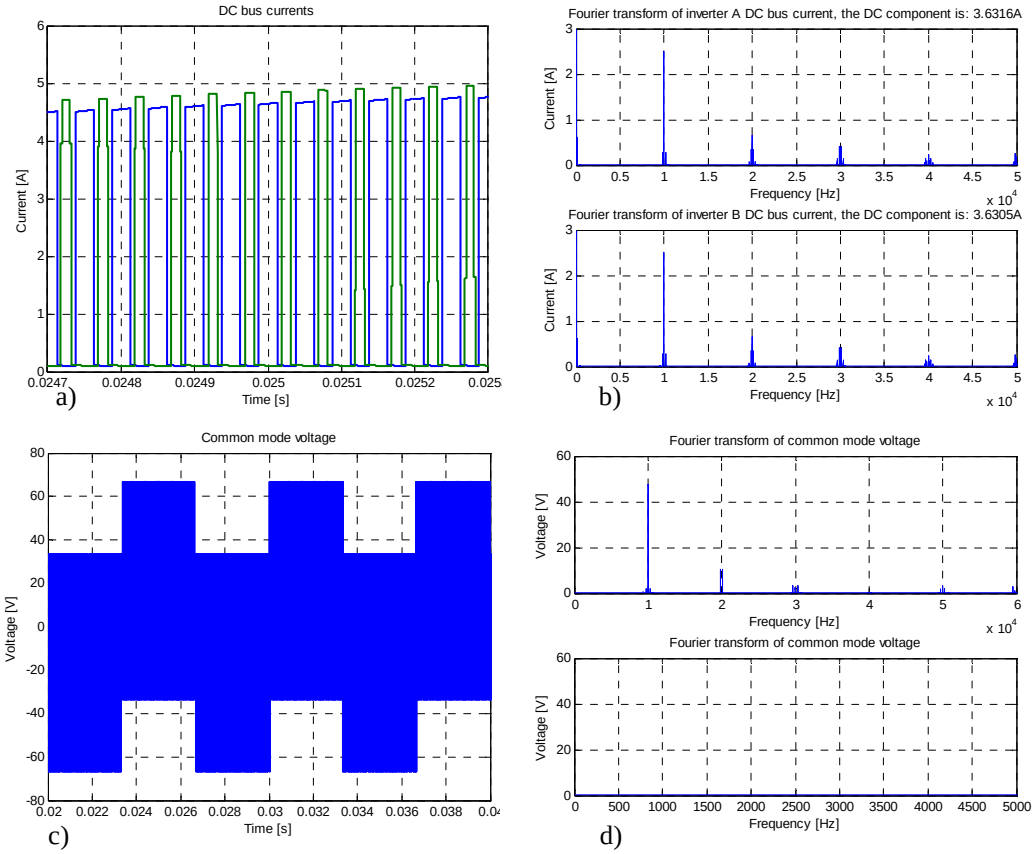


Figure 4.15: Waveforms related to DC busses with a reference equal to 0.5. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

voltage is presented in Figure 4.15c) and its spectrum is shown in Figure 4.15d). The fundamental of the common mode voltage can be found at 10 kHz, so its spectrum is deprived of all low frequency harmonics.

The waveforms of load voltage and current with a reference equal to 1 are depicted in Figure 4.16a). It is interesting to note that the voltage waveform exploits more levels than using lesser references. All the possible levels are now used, but the voltage commutates among three adjacent levels only in each switching cycle. This property of the modulation is extremely good to increase the performances of the converter because the derivative of the voltage with respect to the time is slightly decreased in the comparison with the two references modulation. Obviously this means a lesser stress over the components, which is subject to smaller voltage overshoots and may last longer. Looking at Figure 4.16b) it is possible to note that the null vector is never used, because the reference is always in the outermost part of the hexagon. So, only the nearest vectors are used to synthesise the desired output.

Figure 4.16c) still highlights this concept showing the voltage level used when the reference is near to its maximum. As it is possible to see, the zero voltage level is no more used on the contrary of what is happening using the two references modulation as in Figure 4.8a). Unfortunately the given reference is the limit of the linear zone for a standard SPWM as Figure 4.16d) and e) show clearly.

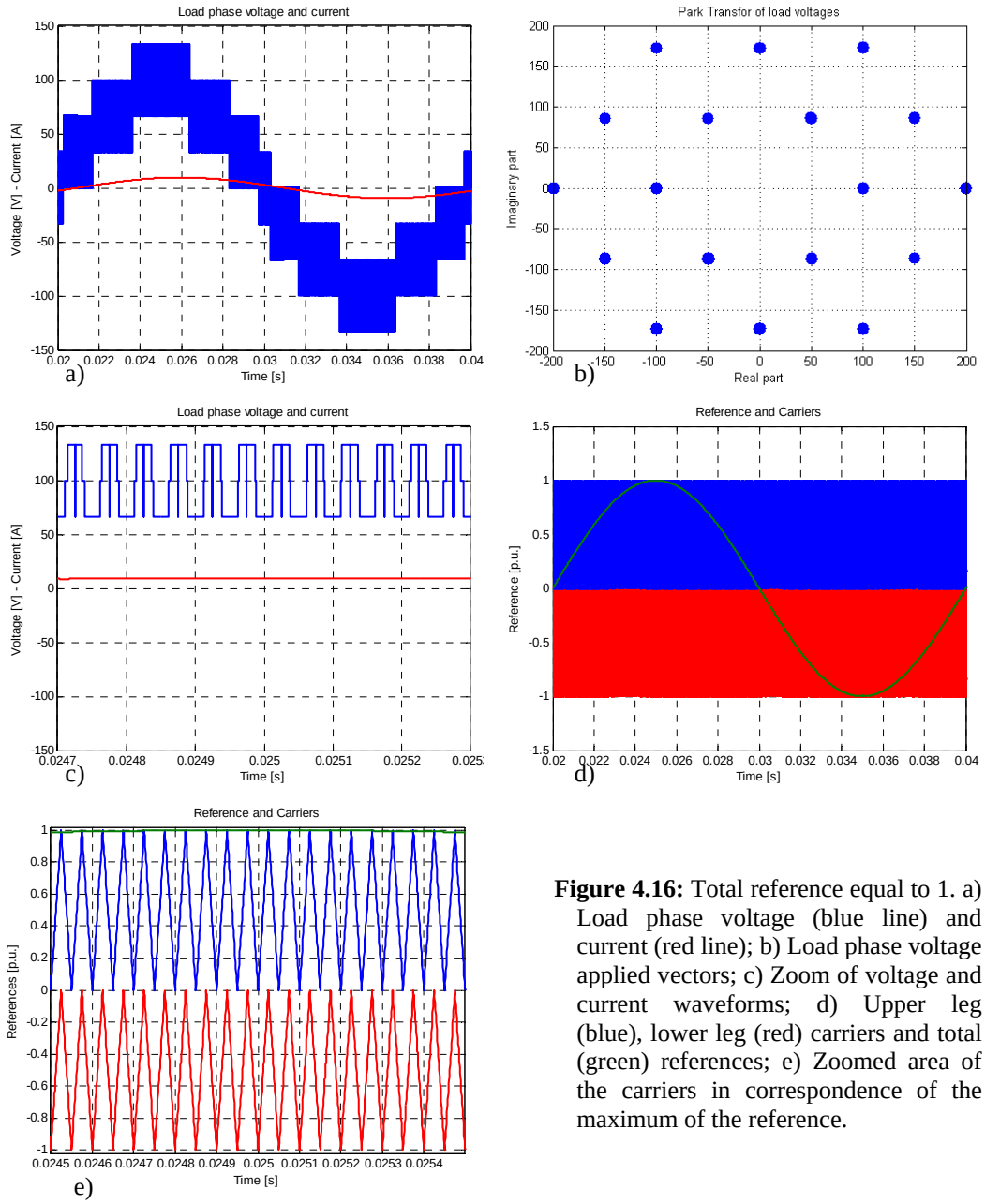


Figure 4.16: Total reference equal to 1. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) carriers and total (green) references; e) Zoomed area of the carriers in correspondence of the maximum of the reference.

As usual, Table 4.7 reports the RMS and THD values of the load phase voltage and current. It is clear the performances of the converter are increased using this particular kind of modulation considering a simple comparison of Table 4.7 and Table 4.3.

Load phase voltage	
RMS	74.866 V
THD	0.35365
Load phase current	
RMS	6.7338 A
THD	0.0019617

Table 4.7: Load Phase voltage and current RMS and THD with a reference of 1.

The THD related to the two carriers modulation is even smaller than the one related to the two references modulation which was a quite good.

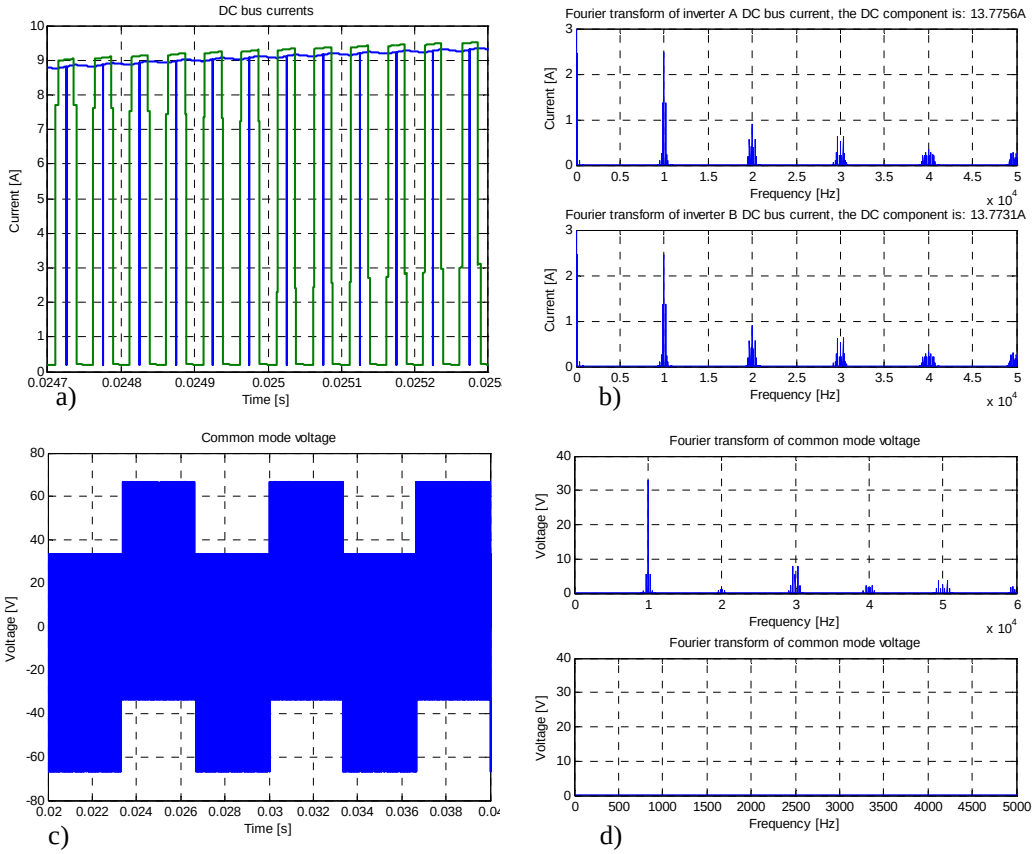


Figure 4.17: Waveforms related to DC busses with a reference equal to 1. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

Figure 4.17a) shows the DC bus currents when the reference is equal to 1 and Figure 4.17b) reports their spectra. Even in this case, the two currents present a DC component and a relatively high harmonic at 10 kHz. Figure 4.17c) shows the waveform of the common mode voltage while in Figure 4.17d) its spectrum is depicted. The low frequency spectrum (lower picture) is not present and the fundamental of the common mode voltage is located at 10 kHz. This last consideration is valid for all the modulations which use the SPWM. In the following, it is possible to see that a GPWM will introduce some low frequency harmonic in the common mode, in particular at 150 Hz.

To conclude this section, a simulation using a GPWM has been done with a reference equal to $\frac{2}{\sqrt{3}}$. First of all, comparing GPWM with SPWM it is possible to notice a difference on the load phase voltage waveform depicted, together to the current in Figure 4.18a). It can be noted there is a sudden change of the voltage levels involved in the modulation when the reference change sign. This did not happen in the previous cases but it is not ascribable to the different modulation (GPWM instead SPWM), but it is due to the reference amplitude. Considering Figure 4.18b), the voltage vectors involved in the modulation are depicted. They define the outer part of the triangular grid specific of this converter. In particular, in each sector there are three visible triangles: two lateral and one central. Because of its amplitude, the reference is tangent to the outer hexagon and does not pass through the central triangle. This is the reason of the sudden passage which is possible to see in the voltage waveform. Figure 4.18c) highlights the commutation of the voltage in correspondence of the maximum of the reference. Figure 4.18d) shows the carriers and the reference in one fundamental period. Figure 4.18e) is a time scale magnification of Figure 4.18d) highlighting the modulation is still in linear zone.

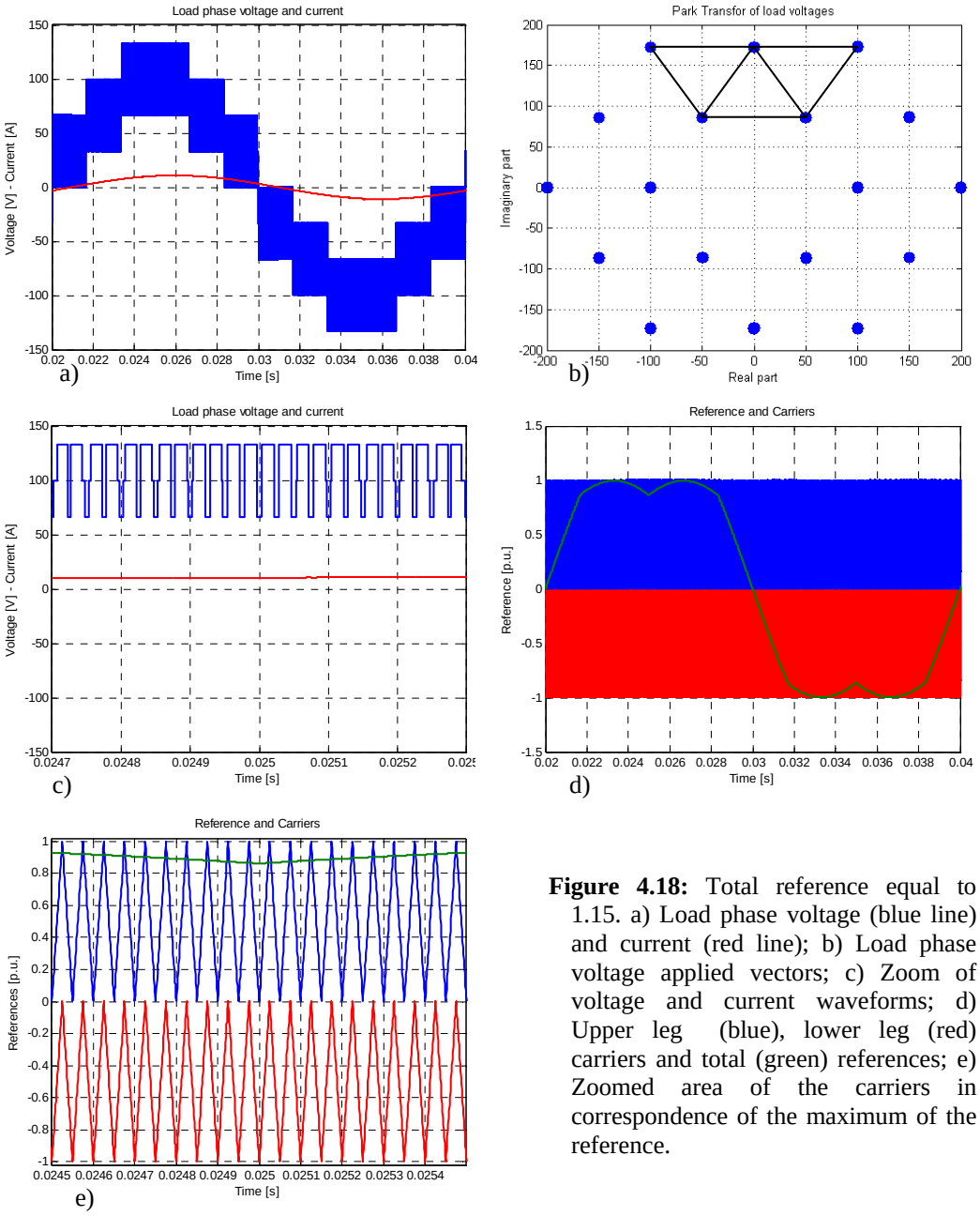


Figure 4.18: Total reference equal to 1.15. a) Load phase voltage (blue line) and current (red line); b) Load phase voltage applied vectors; c) Zoom of voltage and current waveforms; d) Upper leg (blue), lower leg (red) carriers and total (green) references; e) Zoomed area of the carriers in correspondence of the maximum of the reference.

Table 4.8 reports the RMS and THD values of load phase voltage and current. Voltage THD is an extremely good value, but it should be taken into account that there are no dead time which are

Load phase voltage	
RMS	84.14 V
THD	0.27301
Load phase current	
RMS	7.7438 A
THD	0.0014769

Table 4.8: Load Phase voltage and current RMS and THD with a reference of 1.15.

the main cause of THD worsening.

Regarding DC bus situation, Figure 4.19a) depicts the waveforms of the two DC currents while Figure 4.19b) shows their spectra. Now the harmonic content is composed by more frequencies than

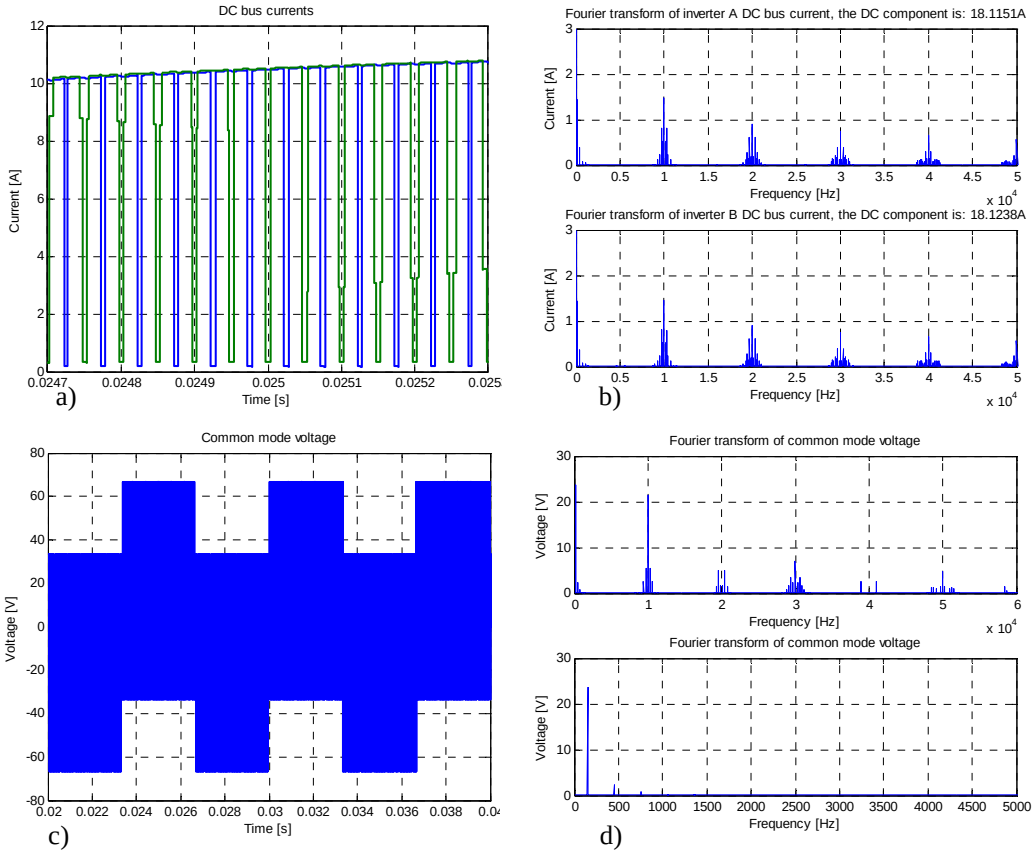


Figure 4.19: Waveforms related to DC busses with a reference equal to 1.15. a) DC bus currents through inverter A (blue line) and B (green line); b) DC bus current spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 20 kHz while the lower one highlights the low frequency spectrum.

in SPWM, but the amplitude are slightly decreased. Figure 4.19c) displays the common mode voltage waveform. It seems to be equal to the one obtained using SPWM , but the harmonic content in Figure 4.19d) highlights the appearance of low frequency harmonics, in particular the one at 150 kHz.

4.3. Special carrier based modulation

4.3.1. Modulation and six-step

To conclude the simulations of analogue modulation strategies, in this section a particular technique is presented. In the landscape of pulse width modulations saw-tooth or triangular carriers have been always used. The saw-tooth carrier is the simplest way to guarantee the proportionality between the area subtended by the reference and the one subtended by the gating signals. Moreover an improvement of the output spectrum is introduced by using triangular shaped carriers. However, both the carriers repeat themselves every switching period and they do not differentiate among the parts composing a multilevel converter. That is the several voltage sources are always exploited in the same way.

Some differences have been introduced in hybrid multilevel converters when the frequencies of the carriers are unequal to adapt to the different characteristics of the devices (Section 2.4.3).

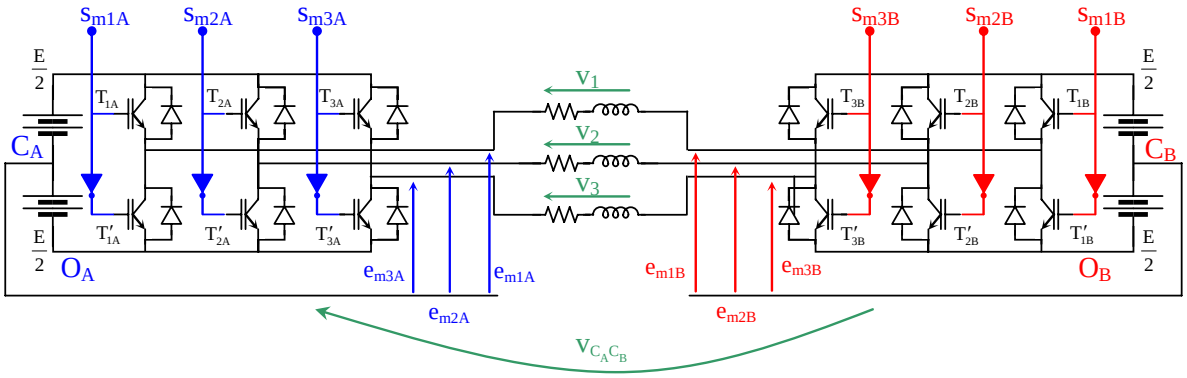


Figure 4.20: Electrical circuit considered in the analogue modulation which synchronises the commutations of the two inverters.

In this section a new approach is presented which aims to distinguish two different roles for the inverters: one of them is modulated using six-step modulation while the other one is modulated at high frequency. Moreover the proposed modulation exchanges inverter roles between them to equalize the delivered powers.

In Figure 4.20 the voltage references used in the following discussion are depicted. In the development of this modulation control scheme is has been found useful to refer the output voltages to the two middle points of DC busses indicated as C_A and C_B in Figure 4.20. So there are two sets of output voltages: e_{m1A}, e_{m2A} and e_{m3A} are associated to inverter A, while e_{m1B}, e_{m2B} and e_{m3B} are associated to inverter B. The load phase voltages are still betoken as v_1, v_2 and v_3, while the common mode voltage between the two middle point is referred as $v_{C_AC_B}$.

Kirchhoff's voltage law can be applied to each phase leading to the following equations which give the relationships among all the voltages.

$$\begin{cases} e_{m1A} = v_1 + e_{m1B} - v_{C_AC_B} \\ e_{m2A} = v_2 + e_{m2B} - v_{C_AC_B} \\ e_{m3A} = v_3 + e_{m3B} - v_{C_AC_B} \end{cases}. \qquad \textbf{(4.4)}$$

The determination of the common mode voltage is quite simple. Considering a close surface wrapping one inverter and the load, it can be observed the sum of the three load currents has to be zero due to Gauss' theorem. In the hypothesis the load is linear, even the sum of the load phase voltages (i.e. the load phase common mode voltage) has to be zero. Summing the three equations in (4.4) leads to:

$$v_{C_AC_B} = -\frac{1}{3}\left(\sum_{j=1}^{3} e_{mjA} - \sum_{j=1}^{3} e_{mjB}\right). \qquad \textbf{(4.5)}$$

It is assumed that a possible modulation solution is given, for the generic phase k, by the following equation in which the quantity x is arbitrary with the bond to keep all the quantities inside their boundaries and v_k^* is the total reference for the generic phase.

$$e_{mkA} - e_{mkB} = v_k^* - x\,. \qquad \textbf{(4.6)}$$

Substituting (4.5) in (4.4) and then (4.6), it leads to:

$$\begin{cases} v_1 = e_{m1A} - e_{m1B} + v_{C_A C_B} = v_1^* - \frac{1}{3}\left(v_1^* + v_2^* + v_3^*\right) \\ v_2 = e_{m2A} - e_{m2B} + v_{C_A C_B} = v_2^* - \frac{1}{3}\left(v_1^* + v_2^* + v_3^*\right). \\ v_3 = e_{m3A} - e_{m3B} + v_{C_A C_B} = v_3^* - \frac{1}{3}\left(v_1^* + v_2^* + v_3^*\right) \end{cases} \quad \textbf{(4.7)}$$

Equations (4.7) are tautologies only if the sum of the load phase voltages is equal to zero. This happens in the considered structure, so the assumed solution is not contradictory. In this way a relationship between the total reference and the single inverter references is obtained. In the actual implementation per unit references were preferred. Accordingly to the choice done about the voltage references, inverters output voltages can continuously vary between $-E/2$ and $+E/2$, while the load phase voltages limits are $-E$ and $+E$. The per unit references are introduced in (4.8) where v_k^*, e_{mkA}^* and e_{mkB}^* are, respectively, the voltage references of the generic phase k for the whole converter, for inverter A and for inverter B.

$$r_k^* = \frac{v_k^*}{E} \qquad r_{kA}^* = \frac{2e_{mkA}^*}{E} \qquad r_{kB}^* = \frac{2e_{mkB}^*}{E}. \quad \textbf{(4.8)}$$

Dividing (4.8) by $E/2$, it can be modified introducing the references just defined. It leads to:

$$r_{kA}^* - r_{kB}^* = 2r_k^* - y. \quad \textbf{(4.9)}$$

To simplify the approach, it is assumed now that inverter B is always controlled using six-step modulation, while inverter A must synthesise the remaining part of the total reference. Given r_k^*, the reference for inverter B is easily determined: if r_k^* is not negative r_{kB}^* is equal to 1 else r_{kB}^* is equal to -1. Moreover, using (4.9) even the reference for inverter A is determined.

$$r_{kA}^* = 2r_k^* + r_{kB}^*. \quad \textbf{(4.10)}$$

In (4.10) the quantity y has been arbitrary assumed as zero to make a simplification. In Figure 4.21a) two carriers are shown: the blue and the red one. The blue carrier is the usual triangular waveform, while red one is constantly equal to zero. This choice has been made because a direct comparison of the opposite of the total reference with zero will give the correct gating signals for the inverter in six-step. Concerning inverter A, its gating signals come from the comparison between the modified reference given by (4.10) and the blue carrier, as Figure 4.21a) highlights.

Using the two carriers just presented it is possible to achieve the first purpose of the modulation: one inverter commutates at low speed following a six-step, while the other one synthesises the difference at higher frequency. Now, a further step has to be done: a way to exchange the roles between the inverters has to be found. This is not complicated because a particular carrier can be created being a triangular wave in half period and zero in the other half. The high frequency commutation is associated to the triangular wave, whereas the six-step role is associated to the other half period. Obviously, the two inverters must always assume complementary roles, so the two carriers must be delayed of half a period as shown in Figure 4.21b) by the blue and the red wave.

Moreover, the two references appear to be quite queer because they are discontinuous due to the role exchange. Indeed each inverter changing the role each half period even change the reference it needs: a compensated reference is needed in half period while in the other half the total reference is directly compared to zero.

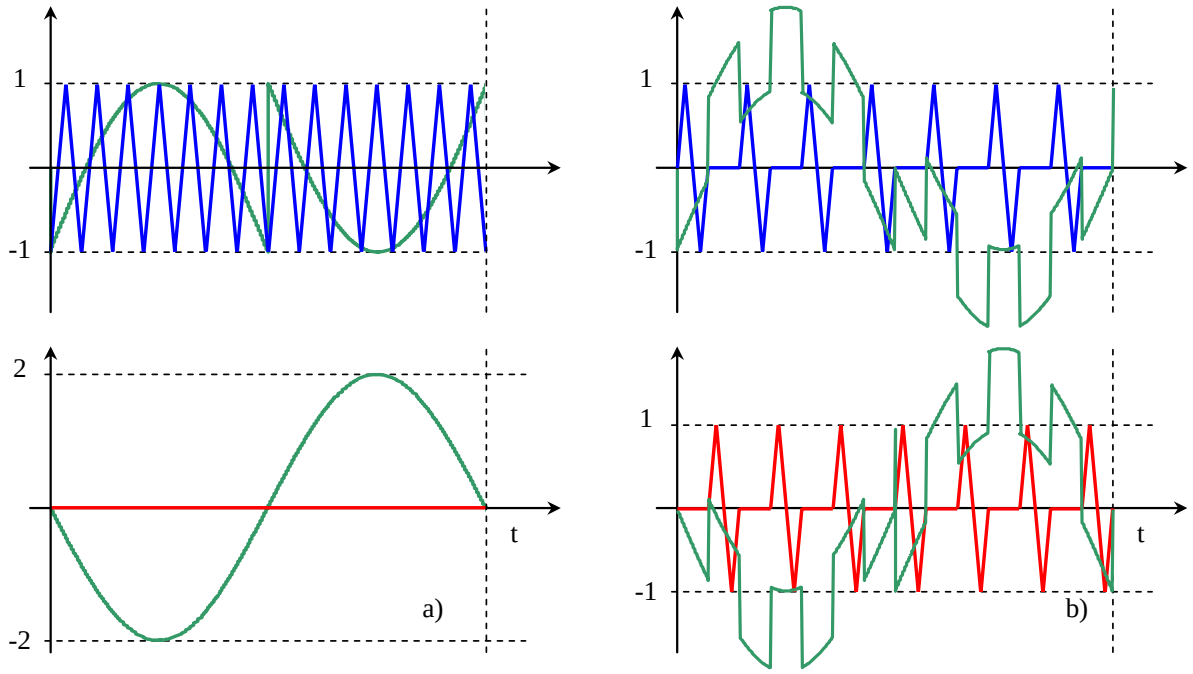


Figure 4.21: Carriers used in the modulation. a) Inverter A is always modulating at high frequency while inverter B is modulated in six step; b) Inverter A and inverter B exchange their role due to the particular shape and complementarity of the carriers.

The control scheme implemented in Simulink is presented in Figure 4.22. Due to the complexity of the algorithm, some explanations about the control may better clarify what was said above.

The total reference is doubled accordingly to (4.10) to get to inverter A reference while the double of the opposite is considered for inverter B. The two switches, driven by the signal “Six-Step Indicator” add zero when the specific inverter has the six-step role or add the compensation of the reference when the inverter has to modulate at high frequency. Inverter carriers are subtracted from

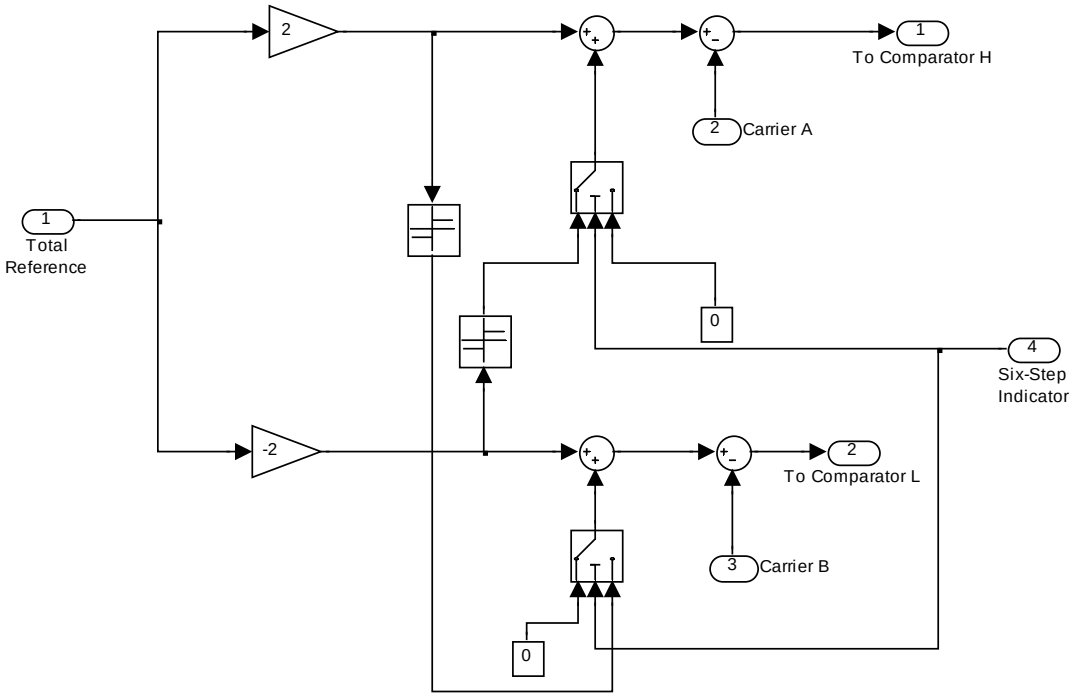


Figure 4.22: Control scheme for one phase implemented in Simulink to achieve the proposed modulation.

the resulting signals to obtain the driving signals for the two comparators which are connected to the gates of the complementary legs.

4.3.2. Simulation results

The modulation strategy presented in the previous section has been simulated using MatLab Simulink with total reference equal to 0.25, 0.5, 1 and 1.15 to make possible a comparison with other results.

Figure 4.23a) depicts the load voltage and current waveform when the total reference is equal to 0.25. As expected, only the smallest voltage level are used to synthesise the desired voltage. This can be better seen in Figure 4.23b), where Park transform of load phase instantaneous voltage is

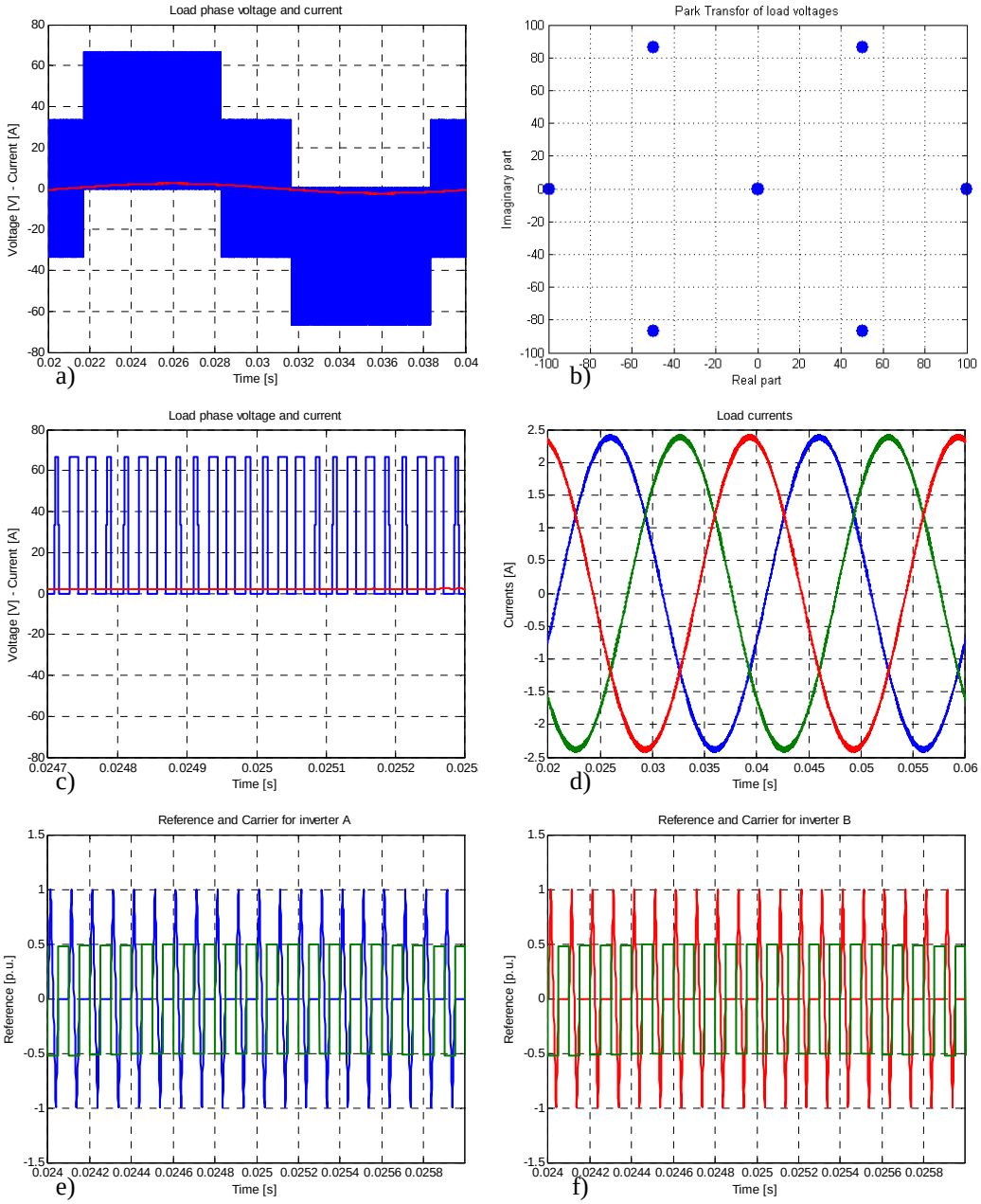


Figure 4.23: Total reference equal to 0.25. a) Load phase voltage (blue line) and current (red line); b) Load phase applied vectors; c) zoom of voltage and current waveforms; d) Load phase currents; e) Inverter A carrier (blue line) and reference (green line); f) Inverter B carrier (red line) and reference (green line).

shown. Figure 4.23c) shows a time magnification of the voltage and the current to better see the commutation involved. To prove the modulation is linear, Figure 4.23d) gives two periods of load currents: they are quite close to sinusoidal waveforms. Eventually, Figure 4.23e) and f) depict the carrier and the reference related to inverter A and inverter B respectively. The most important thing these pictures have to show is that the reference is always contained in the carrier sweep during high frequency modulation, i.e. during the half period in which the carrier is not flat.

As usual, RMS and THD values of the load voltage and current are reported in Table 4.9. The data show this modulation produces outputs pretty close to the one using two carriers.

Load phase voltage	
RMS	30.2935 V
THD	1.3955
Load phase current	
RMS	1.6835 A
THD	0.0085139

Table 4.9: Load Phase voltage and current RMS and THD with a reference of 0.25.

Figure 4.24a) depicts the DC currents waveforms related to the two inverters: it is possible to distinguish clearly when one inverter is switching at high frequency and when is in six-step. Figure 4.24b) shows the spectra of the two currents. Due to the role exchange, the DC component of the currents are the same and the delivered power as well. Figure 4.24c) depicts the common mode

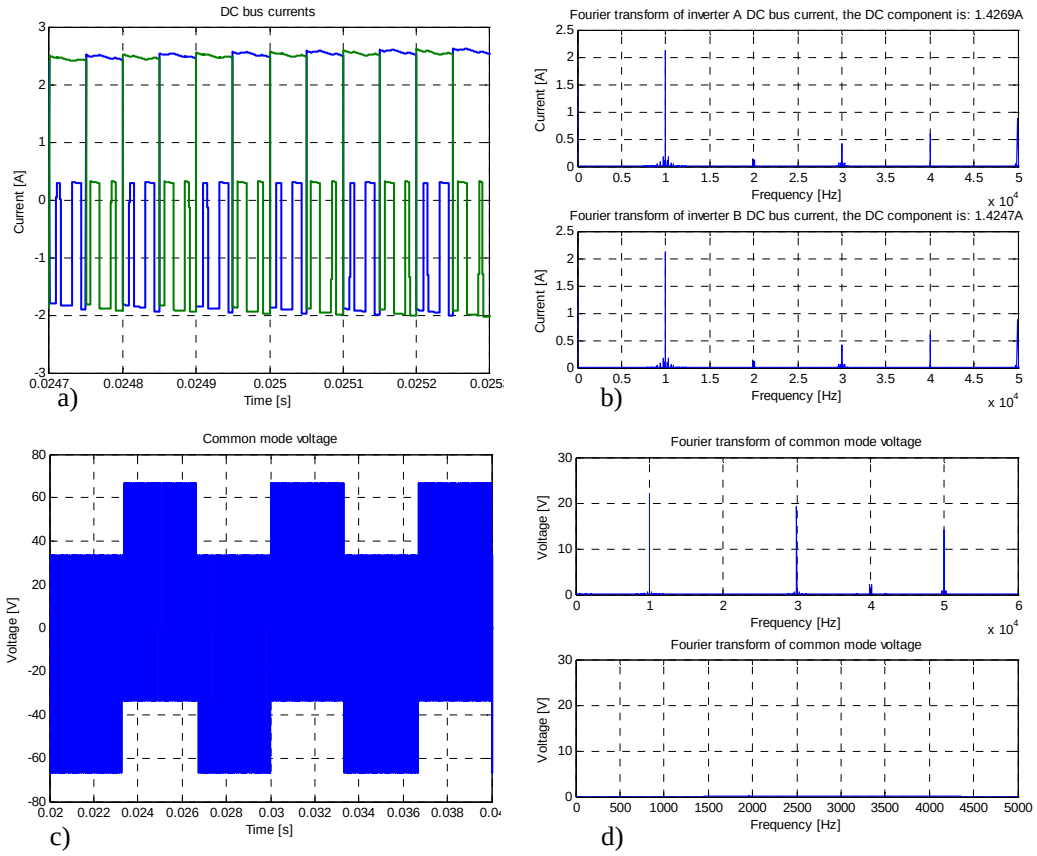


Figure 4.24: Waveforms related to DC busses with a reference equal to 0.25. a) DC bus currents through inverter A (blue line) and through inverter B (green line); b) DC currents spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 60 kHz while the lower one highlights the low frequency spectrum.

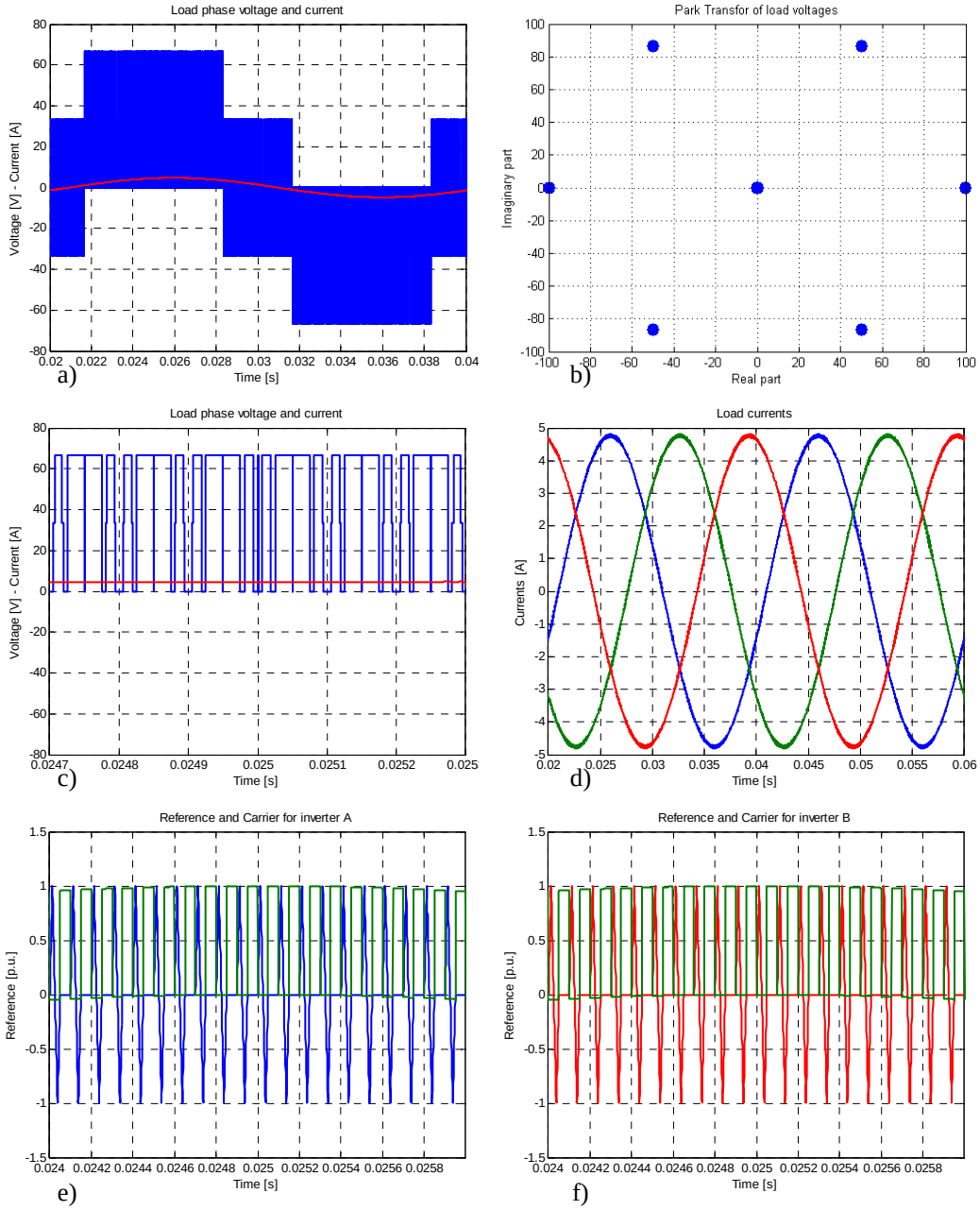


Figure 4.25: Total reference equal to 0.5. a) Load phase voltage (blue line) and current (red line); b) Load phase applied vectors; c) Zoom of voltage and current waveforms; d) Load phase currents; e) Inverter A carrier (blue line) and reference (green line); f) Inverter B carrier (red line) and reference (green line).

voltage waveform and Figure 4.24d) gives its spectrum.

Concerning the simulation with a reference equal to 0.5, Figure 4.25a) shows load phase current and voltage waveforms. From Figure 4.25b) it is possible to understand the modulation still exploits the right voltage vectors because only the inner active vectors and the null one are used to synthesise a reference inside the inner hexagon. Figure 4.25c) shows a time magnification of the load voltage to draw the attention to the voltage levels. Figure 4.25e) shows the control of inverter A whereas Figure 4.25f) is referred to inverter B.

Table 4.10 reports THD and RMS for the load voltage and current. It is possible to see that the voltage waveform produced using this modulation is quite near to the one produced using the modulation with two carriers but in this case the harmonic content is more concentrated in the low

frequencies: indeed the THD of the current is higher then in the previous case, even if RMS values are identical.

Load phase voltage	
RMS	42.8156 V
THD	0.68694
Load phase current	
RMS	3.3669 A
THD	0.0066554

Table 4.10: Load Phase voltage and current RMS and THD with a reference of 0.5.

Regarding DC side, Figure 4.26a) shows the DC currents flowing through the two inverters. Even in this case it is quite easy to distinguish when the inverter operates in six-step mode and is switching. Figure 4.26b) reports the spectra of the two DC currents: the 10 kHz harmonic is the more emphasized while the high frequency harmonics are quite lower than in two carriers modulation. Figure 4.26c) depicts the common mode voltage waveform, showing quite clearly it has a null mean value. This could even be noticed by Figure 4.26d) where its spectrum is shown.

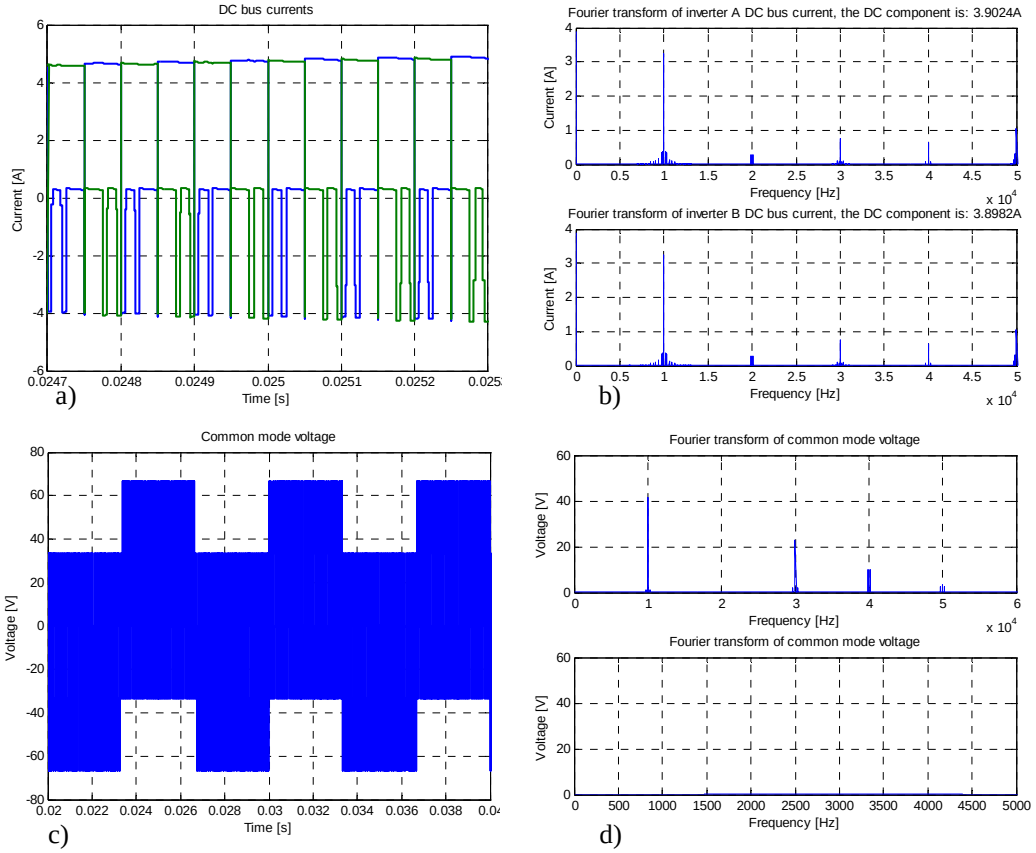


Figure 4.26: Waveforms related to DC busses with a reference equal to 0.5. a) DC bus currents through inverter A (blue line) and through inverter B (green line); b) DC currents spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 60 kHz while the lower one highlights the low frequency spectrum.

The harmonic at 20 kHz is not present, but 10, 30 and 40 kHz harmonics are slightly huge. Even in this case, there are not low frequency harmonics (less than 5 kHz).

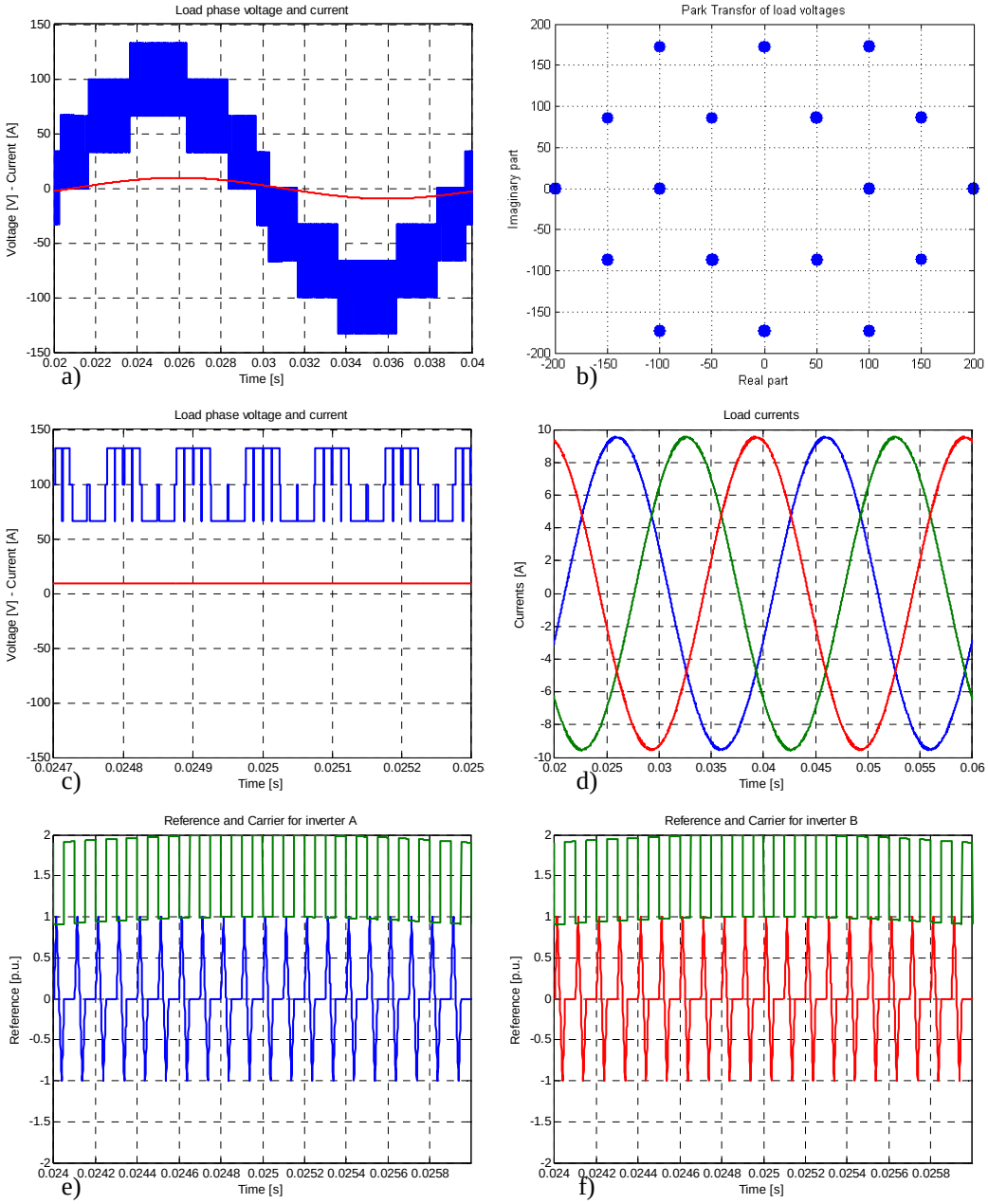


Figure 4.27: Total reference equal to 1. a) Load phase voltage (blue line) and current (red line); b) Load phase applied vectors; c) Zoom of voltage and current waveforms; d) Load phase currents; e) Inverter A carrier (blue line) and reference (green line); f) Inverter B carrier (red line) and reference (green line).

Voltage and current waveforms with a reference equal to 1 are depicted in Figure 4.27a). The reference lays in the outer hexagon, so the outermost vectors are used meaning that all the voltage levels are exploited. Figure 4.27b) emphasizes this concept showing the applied voltage vectors as blue dots. Figure 4.27c) displays a zoomed area of Figure 4.27a) in correspondence of the maximum voltage to highlight the commutations. Figure 4.27d) depicts the load current to prove the modulation is still linear because it can be seen they are quite near to sinusoidal wave. To conclude the part related to AC side, Figure 4.27e) shows the carrier and the reference for inverter A: the reference (green line) is touching the high edge of the carrier meaning the system is operating at the limit of linearity. The same can be seen from Figure 4.27f) which shows carrier and reference for inverter B.

Table 4.11 reports RMS and THD values for the load voltage and current. Increasing the voltage required slightly decrease the THD.

Load phase voltage	
RMS	74.8663 V
THD	0.35366
Load phase current	
RMS	6.7338 A
THD	0.003211

Table 4.11: Load Phase voltage and current RMS and THD with a reference of 1.

Regarding DC side, Figure 4.28a) depicts the currents flowing through the two inverters: the reference is near the limit of the system, so there is not an evident demarcation between the six-step and the switching modes. Figure 4.28b) shows the DC current spectra indicating a greater harmonic content than with lower references. Figure 4.28c) depicts the common mode voltage which has its first harmonic at 10 kHz as Figure 4.28d) shows. Its low frequency spectrum is still empty because the modulation is still sinusoidal and not generalized.

To conclude the overview of the analogue modulation, one simulation has been conducted using a reference equal to 1.15, together to a generalized pulse width modulation to guarantee the linearity. Figure 4.29a) shows the load phase voltage and current highlighting all the voltage levels used in the modulation. Figure 4.29b) shows the voltage vectors instantaneously applied: only the

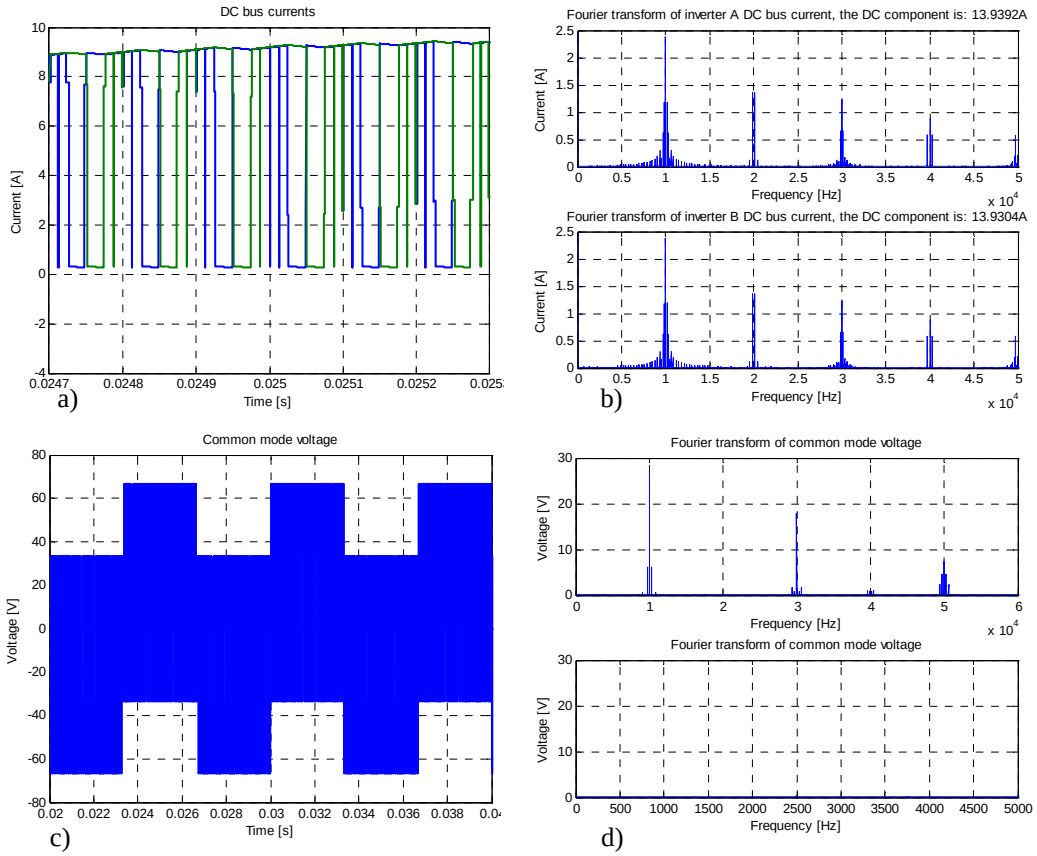


Figure 4.28: Waveforms related to DC busses with a reference equal to 1. a) DC bus currents through inverter A (blue line) and through inverter B (green line); b) DC currents spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 60 kHz while the lower one highlights the low frequency spectrum.

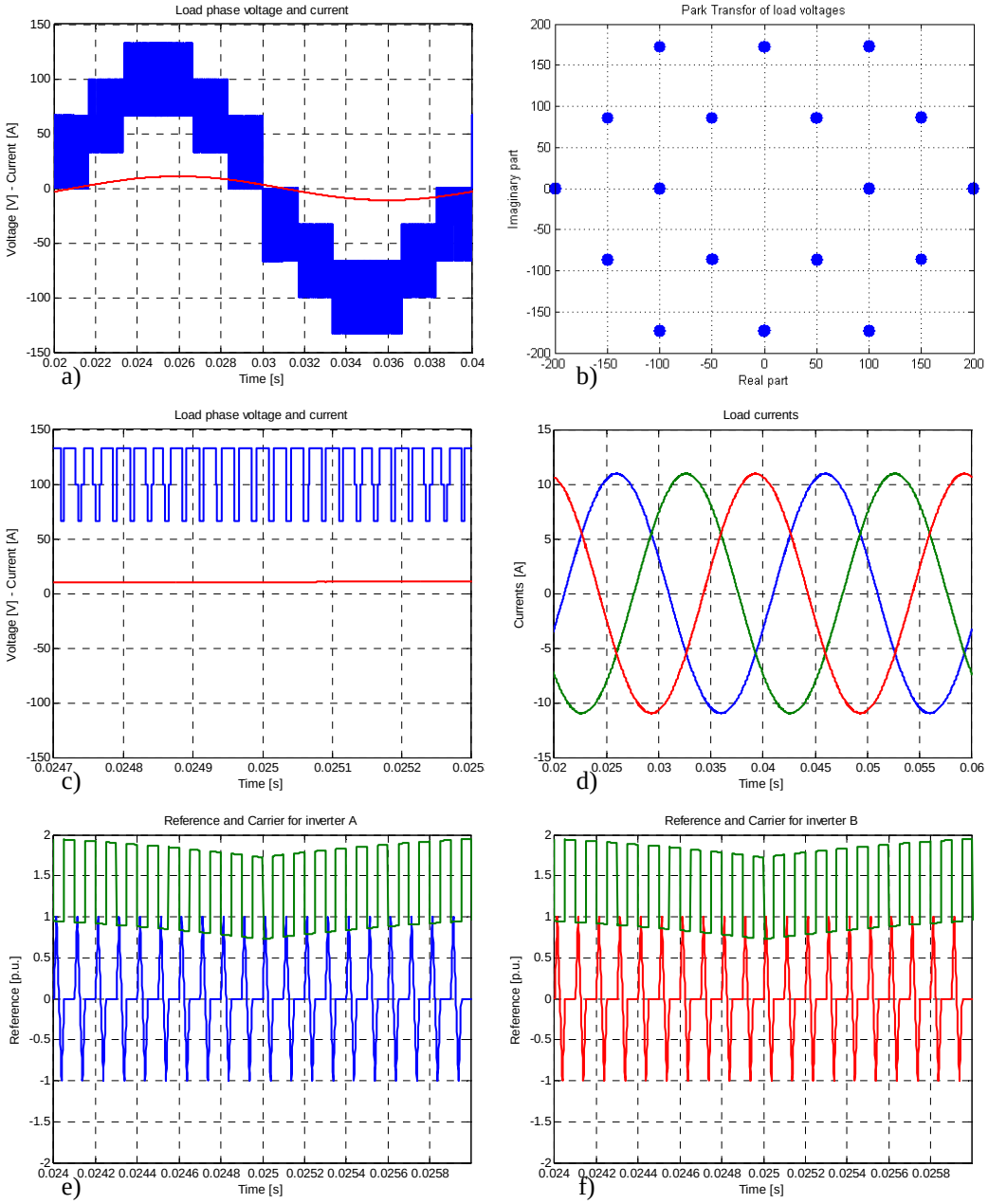


Figure 4.29: Total reference equal to 1.15. a) Load phase voltage (blue line) and current (red line); b) Load phase applied vectors; c) Zoom of voltage and current waveforms; d) Load phase currents; e) Inverter A carrier (blue line) and reference (green line); f) Inverter B carrier (red line) and reference (green line).

outermost are used to synthesise the requested reference. Figure 4.29c) shows a time magnification of Figure 4.29a) which allows to better see system commutations. In Figure 4.29d) the load phase currents are represented to underline the modulation is in linear zone even using a greater reference. Figure 4.29e) shows carrier and reference used in the control of inverter A whereas Figure 4.29f) shows the same waveforms for inverter B control. A part from the discontinuities on the references due to the modulation strategy which modifies the reference when the inverter is in switching mode, the peculiar bilobate shape of GPWM can be still recognized.

Table 4.12 reports THD and RMS values of the load phase voltage and current in one phase. Voltage THD is even improved reaching a quite low value. Anyway, it is important to remember the dead times were not implemented on the simulation and it is expected a huge worsening of THD after their introduction.

Load phase voltage	
RMS	84.1396 V
THD	0.27299
Load phase current	
RMS	7.7438 A
THD	0.0025087

Table 4.12: Load Phase voltage and current RMS and THD with a reference of 1.15.

To conclude, Figure 4.30a) shows the DC current waveforms while Figure 4.30b) depicts their spectra. Unfortunately, the harmonic content of the DC currents is grown using GPWM in the respect of the standard SPWM. The common mode voltage is represented in Figure 4.30c) and its spectrum is given in Figure 4.30d). Even regarding common mode voltage, using a GPWM adds harmonic content quite visible, particularly at low frequencies. From the bottom picture in Figure 4.30d) a harmonic at 150 Hz can be noticed.

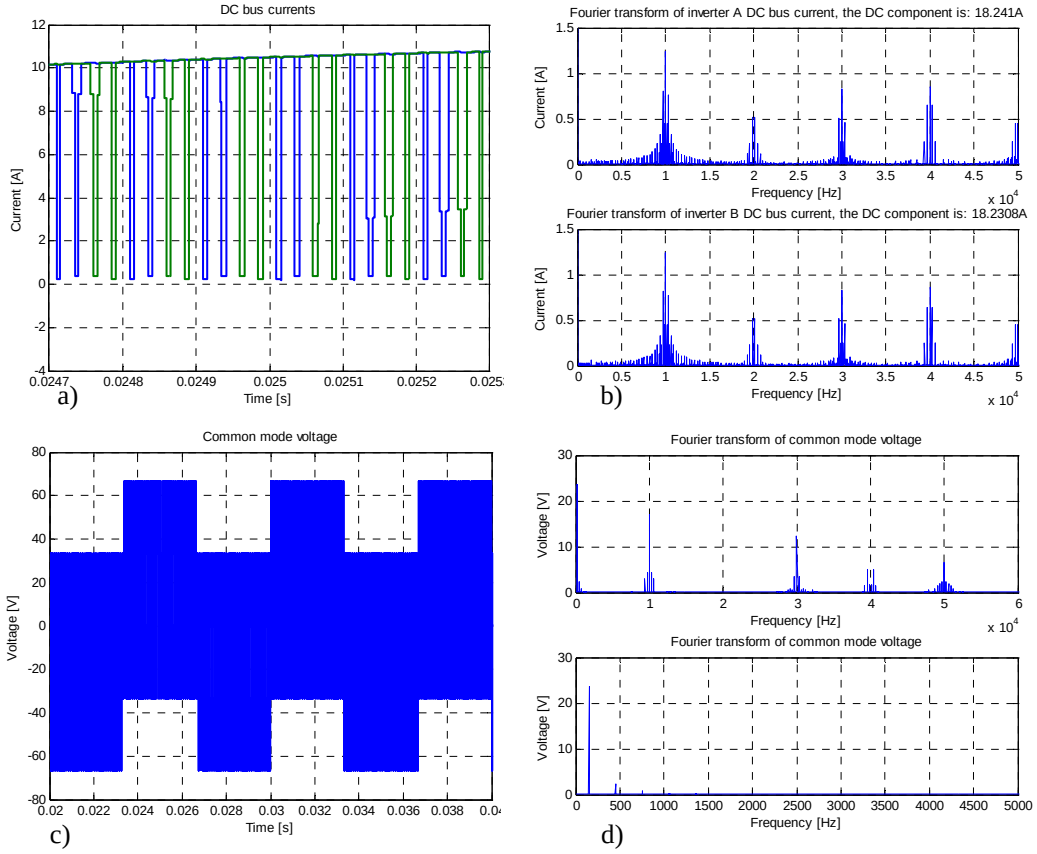


Figure 4.30: Waveforms related to DC busses with a reference equal to 1.15. a) DC bus currents through inverter A (blue line) and through inverter B (green line); b) DC currents spectra; c) Common mode voltage between the negative poles; d) Fourier's transform of the common mode voltage: the upper picture shows frequencies until 60 kHz while the lower one highlights the low frequency spectrum.

Chapter 5

Digital modulation

5.1. Introduction

5.1.1. Power sharing

In the previous chapter some analogue modulation strategies have been presented and discussed. The purpose of this chapter is to analyse the **Space Vector Modulation** (**SVM**) developed for the dual 2-level inverter. The principles of SVM are well known for multilevel converters as seen in Chapter 1, but some new contributions will be given.

Using SVM techniques directly involves a large amount of calculations to be done during switching periods. Usually, these calculations are done using a dedicated microprocessor or a **Digital Signal Processor** (**DSP**). So, introducing additional code to achieve some particular purpose is possible without increasing the cost of the system.

Considering the system proposed in this thesis and schematically represented in Figure 5.1, the history of the two DC sources (usually banks of batteries) can be slightly different as well as the voltages produced. The difference in voltage sources will produce some effects on the load feeding which were not taken into account in the previous chapter.

There are several ways to remedy this problem. For example, the control algorithm can consider the difference between the two voltage sources and operates taking into account the effects this will produce on the load voltage. Otherwise, the control can try to keep constant the DC voltages

Figure 5.1: Dual 2-level inverter scheme.

operating on the power supplied by the sources, for instance. Indeed, if the sources are batteries, the discharge will be dependent on the delivered power: controlling the power flow means the control of their discharge.

This idea can be applied to the dual 2-level inverter because of its particular topology exploiting the redundancy of the generable voltage vectors. Indeed, most of the generable vectors can be applied with two or more configurations which imply different power flows through the 3-phase inverters.

5.1.2. Power sharing aims

The first application found for the dual 2-level inverter was automotive traction. Using this converter gives the possibility to avoid the normative in force about maximum battery voltage on board.

In Italy, the maximum voltage allowed for batteries banks is 96 V. The limit on the voltage, together to the current limit of the switching components, creates some bonds to the maximum power of electrical vehicles. To overcome the limits, different solutions have been found: special dual 3-phase motors can be used, for instance. Unfortunately, this solution has the heavy drawback to require a special wounded asynchronous machine, which can be quite expensive.

The solution presented by the dual 2-level inverter is a little bit more effective because allows to use standard components either for the converter (two 3-phase inverters) or the motor (standard asynchronous motor). The bank of batteries can be split in two parts to feed the two inverters: in this way there is no increment on the cost and the voltage limit is doubled. Furthermore, using the control on power sharing, the voltage of the batteries banks can be kept constant improving the quality of load voltage and current. Moreover, in case of fault, the control algorithm can easily impose a null delivered power at the broken inverter, making the other one still operating at half the total rated power.

Another interesting application of the dual 2-level inverter is ship propulsion, in particular fishing boats. The use of the converter in this application allows the fast change between two cruise modes: trawling and moving. During moving mode, the boats require low mechanical power whereas during trawling mode they require high power and high torque. This is a huge problem in the design of diesel engines because the operating conditions of the two modes are really different and the efficiency of the system can be optimized for a single operating condition. The system proposed to overcome the problem is the dual 2-level inverter fed by two diesel engines. The power sharing technique allows the diesel engines to work at the highest efficiency point, while is up to the control algorithm and the electrical part of the system to deliver the power to the screw.

In the following, power sharing technique will be discussed. After a general dissertation which will introduce the theory above power sharing, two implementation ways will be described: one of them is quite easy to implement on a standard DSP based control board, but presents a worst control upon power sharing than the other one.

5.2. Power sharing

5.2.1. Power sharing coefficient

The electrical scheme of the dual 2-level inverter is represented in Figure 5.2. The voltages and currents directions given in Figure 5.2 will be used in the whole Chapter. To start the discussion about power sharing, (5.1) summarizes the Park transform of voltage and current systems.

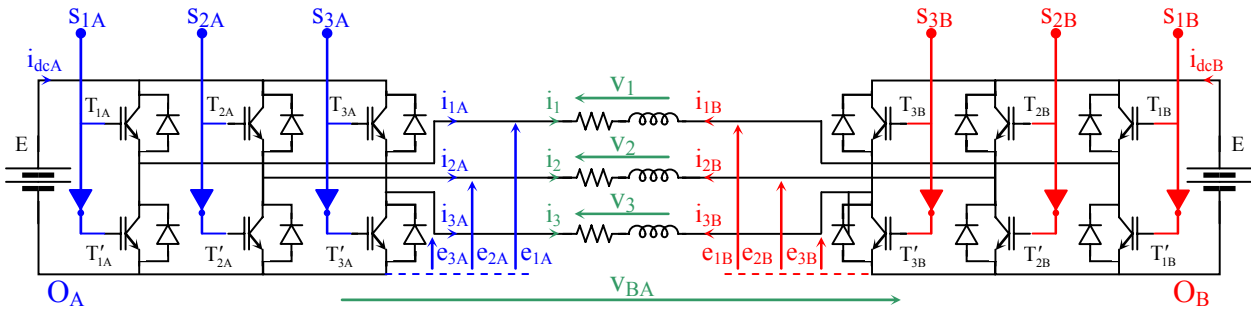


Figure 5.2: Dual 2-level inverter circuit and electrical quantities conventional signs.

$$\begin{cases} \bar{e}_A = \frac{2}{3}\left(e_{1A} + \bar{\alpha} e_{2A} + \bar{\alpha}^2 e_{3A}\right) \\ \bar{e}_B = -\frac{2}{3}\left(e_{1B} + \bar{\alpha} e_{2B} + \bar{\alpha}^2 e_{3B}\right) \\ \bar{v} = \frac{2}{3}\left(v_1 + \bar{\alpha} v_2 + \bar{\alpha}^2 v_3\right) \end{cases} \quad \begin{cases} \bar{i}_A = \frac{2}{3}\left(i_{1A} + \bar{\alpha} i_{2A} + \bar{\alpha}^2 i_{3A}\right) \\ \bar{i}_B = \frac{2}{3}\left(i_{1B} + \bar{\alpha} i_{2B} + \bar{\alpha}^2 i_{3B}\right) \\ \bar{i} = \frac{2}{3}\left(i_1 + \bar{\alpha} i_2 + \bar{\alpha}^2 i_3\right) \end{cases} . \qquad \textbf{(5.1)}$$

In (5.1), $\bar{\alpha}$ is equal to $e^{j\frac{2}{3}\pi}$, whereas $\bar{e}_A$ is the Park transform of inverter A outputs e_{1A}, e_{2A} and e_{3A}. For inverter B outputs e_{1B}, e_{2B} and e_{3B}, the opposite of their Park transform $\bar{e}_B$ is taken into account to simplify the following discussion. Load voltages v_1, v_2 and v_3 are associated to the complex vector $\bar{v}$. The same relationship subsists among the currents: $\bar{i}_A$ is associated to i_{1A}, i_{2A} and i_{3A}, $\bar{i}_B$ to i_{1B}, i_{2B} and i_{3B}, $\bar{i}$ to i_1, i_2 and i_3.

Moreover, (5.2) gives the relationships between converter configurations and inverters outputs or load voltages.

$$\begin{cases} e_{1A} = s_{1A} E \\ e_{2A} = s_{2A} E \\ e_{3A} = s_{3A} E \end{cases} \quad \begin{cases} e_{1B} = s_{1B} E \\ e_{2B} = s_{2B} E \\ e_{3B} = s_{3B} E \end{cases} \quad \begin{cases} v_1 = (s_{1A} - s_{1B})E - v_{BA} \\ v_2 = (s_{2A} - s_{2B})E - v_{BA} \\ v_3 = (s_{3A} - s_{3B})E - v_{BA} \end{cases} . \qquad \textbf{(5.2)}$$

Substituting (5.2) in (5.1) leads to:

$$\begin{cases} \bar{e}_A = E\bar{s}_A \\ \bar{e}_B = E\bar{s}_B \\ \bar{v} = E(\bar{s}_A + \bar{s}_B) \end{cases} . \qquad \textbf{(5.3)}$$

After this short introduction, power sharing can be faced. Considering a converter with efficiency equal to 1, the instantaneous load power and the instantaneous power asked to the sources are the same. If the efficiency of the converter has to be taken into account, the matter is to consider a coefficient in the following equations. So, being $p(t)$ the requested load power, $p_A(t)$ the power flowing through inverter A and $p_B(t)$ the power flowing through inverter B, (5.4) is the relationship existing among them.

$$p(t) = p_A(t) + p_B(t). \qquad \textbf{(5.4)}$$

A **power sharing coefficient** k is introduced: it has been defined as the ratio between the power inverter A must deliver and the required load power. Considering (5.4), even the power delivered by inverter B is defined depending on coefficient k. Equation (5.5) summarises this concept.

$$\begin{cases} p_A(t) = kp(t) \\ p_B(t) = (1-k)p(t) \end{cases}. \tag{5.5}$$

A further step can be done expressing the powers delivered by the two inverters as the dot product between the respective voltage and current vectors, as (5.6) does.

$$\begin{cases} p_A(t) = \frac{3}{2}\bar{e}_A \cdot \bar{i}_A \\ p_B(t) = -\frac{3}{2}\left(\bar{e}_B \cdot \bar{i}_B\right) \end{cases}. \tag{5.6}$$

A similar equation can be written even for the load power, obtaining (5.7).

$$p(t) = \frac{2}{3}\bar{v} \cdot \bar{i}. \tag{5.7}$$

Substituting (5.6) and (5.7) in (5.5), (5.8) is obtained.

$$\begin{cases} \bar{e}_A \cdot \bar{i}_A = k\left(\bar{v} \cdot \bar{i}\right) \\ \bar{e}_B \cdot \bar{i}_B = -(1-k)\left(\bar{v} \cdot \bar{i}\right) \end{cases}. \tag{5.8}$$

Considering Figure 5.2, it can be noticed that inverter A output currents coincide with the load phase currents, whereas inverter B output currents are the opposites of the load phase currents, so (5.9) can be asserted.

$$\begin{cases} \bar{i}_A = \bar{i} \\ \bar{i}_B = -\bar{i} \end{cases}. \tag{5.9}$$

Substituting of (5.9) in (5.8) and considering inverters output voltage vectors ($\bar{e}_A$, $\bar{e}_B$) in phase with the load voltage vector $\bar{v}$ the simplification of the load current vectors in the dot products can be done and leads to (5.10).

$$\begin{cases} \bar{e}_A = k\bar{v} \\ \bar{e}_B = (1-k)\bar{v} \end{cases}. \tag{5.10}$$

Equation (5.10) has an important meaning: it asserts that the power sharing coefficient, which expresses the proportionality between inverters output powers and load power, even gives the proportionality between inverters output voltages and load voltage, under the hypothesis done above. So, to obtain power sharing, the control has to keep inverter output voltages in phase and proportional to the load voltage.

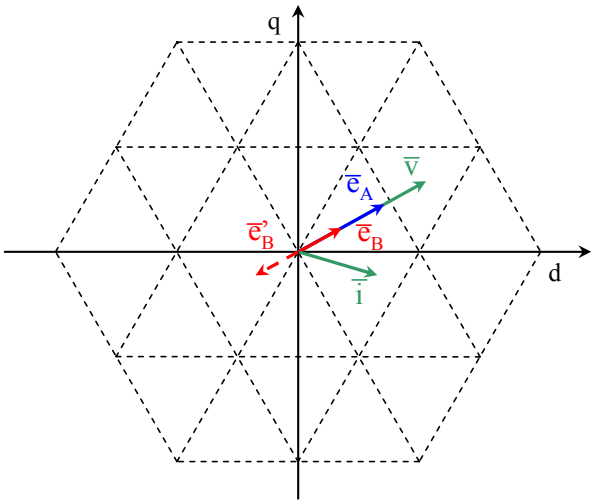


Figure 5.3: Voltage vectors for which the inverters are demanded.

This concept is represented in Figure 5.3 where the output voltage vectors (blue and red) are drawn together to the load voltage and current (green). Regarding inverter B, the vector $\bar{e}'_B$ (dashed) represents the actual Park transform of output voltages e_{1B}, e_{2B} and e_{3B}, whereas $\bar{e}_B$ is the opposite and it is the complex vector which will be taken into account in power sharing technique. As expressed by equation above, the voltage vectors $\bar{e}_A$, $\bar{e}_B$ and $\bar{v}$ must be kept parallel and with the same scale factor existing between the powers: in case of Figure 5.3, k has been chosen equal to $\frac{2}{3}$. Due to the topology of the converter, only the load current is important, because inverters output current can be referred to it. To conclude this Section, it is better to specify that the same relationships existing among $\bar{e}_A$, $\bar{e}_B$ and $\bar{v}$, given by (5.10), can be even considered for the references $\bar{e}^*_A$, $\bar{e}^*_B$ and $\bar{v}^*$. So for any given $\bar{v}^*$ and k (under the boundaries which will be discussed in the following), inverters references $\bar{e}^*_A$ and $\bar{e}^*_B$ are univocally determined.

5.2.2. Duty-cycles determination

Due to the geometrical symmetry existing among the generable vectors three regions can be

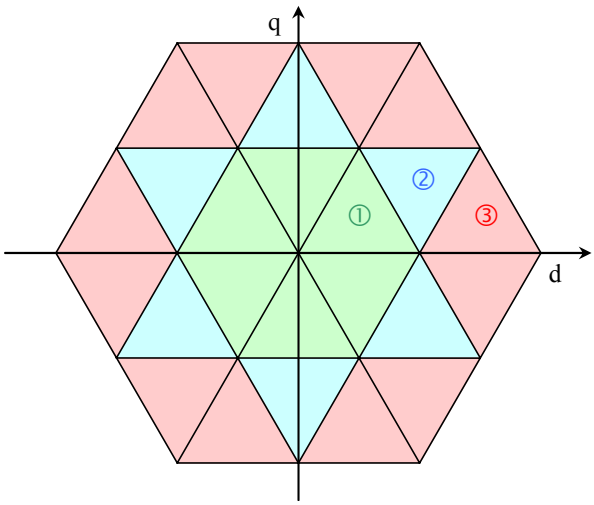


Figure 5.4: Subdivision of d-q plane in three regions due to the symmetry of generable voltage vectors locus. Each colour indicates a different region, in particular Region ① is light green, Region ② is azurine and Region ③ is pink.

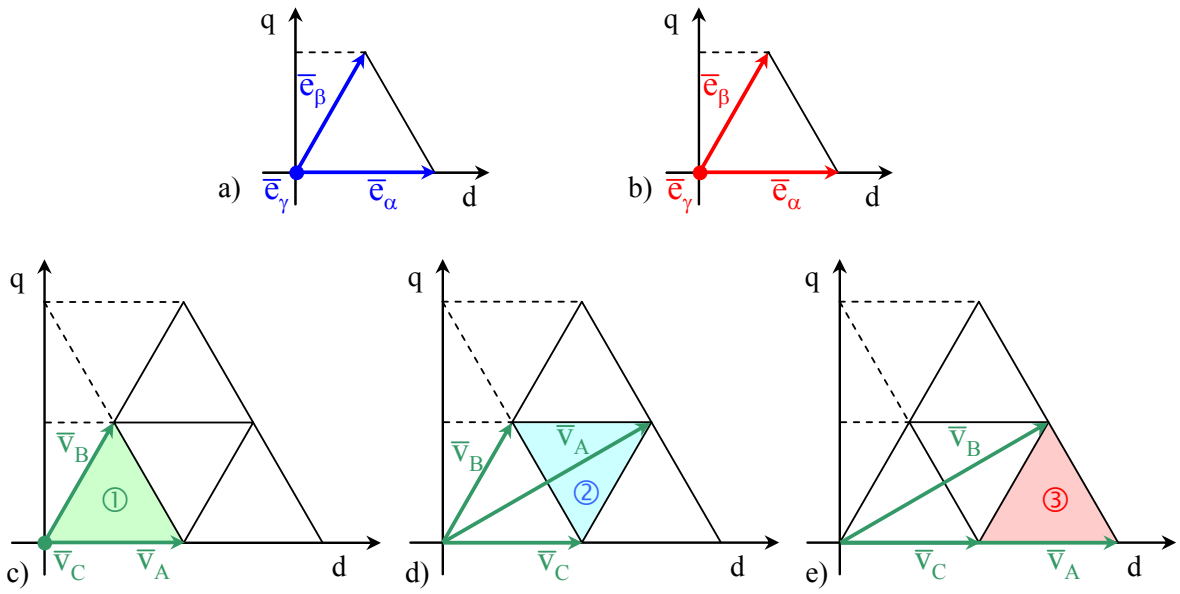


Figure 5.5: Voltage vectors used by the two inverters and by the whole converter to synthesise a reference inside Sector I. a) Inverter A voltage vectors; b) Inverter B voltage vectors; c) Whole converter voltage vectors for Region ①; d) Load voltage vectors in Region ②; e) Load voltage vectors in Region ③.

found called **Region ①**, **Region ②** and **Region ③**, as Figure 5.4 shows. Region ① is composed by the inner triangles highlighted by the light green zone in the picture, azurine middle triangles belong to Region ② and the outermost triangles with pink background constitute Region ③. The three regions just defined are important to simplify the treatment of power sharing because only one triangle for each zone must be analysed. Other triangles analysis is a direct consequence of the geometrical symmetry.

In Figure 5.5 the voltage vectors used in the determination of duty-cycles are shown. It is supposed that the reference lays in Sector I, so even the references for each inverter belong to the same sector. Figure 5.5a) and b) show the vectors each inverter can use to synthesise its own reference: one null vector $\bar{e}_\gamma$ and two active vectors $\bar{e}_\alpha$ and $\bar{e}_\beta$. For both the inverters active vectors are the same because for inverter B is considered the opposite of the representative vector, as previously said. Figure 5.5c), d) and e) depict the vectors used by the dual 2-level inverter to synthesise its reference considering the three different zones. Figure 5.5c) is inherent to Region ①: the total vectors to be used are the null vector $\bar{v}_C$ and the active vectors $\bar{v}_A$ and $\bar{v}_B$. Figure 5.5d) concerns Region ②: the vector used are named in the same way, but represent different active vectors than in Figure 5.5a). Region ③ is represented in Figure 5.5e). This choice to give the same names to different vectors will find the reason why in the following: in this way only one set of equations can describe all the three zones.

To proper control the dual two level inverter it is necessary to determine three sets of duty-cycles: for the whole converter, for inverter A and for inverter B. Given $\bar{v}^*$ and k, the first step in the calculus of duty-cycles is the determination of the references for both inverters: they can be found applying (5.11).

$$\begin{cases} \bar{e}_A^* = k\bar{v}^* \\ \bar{e}_B^* = (1-k)\bar{v}^* \end{cases}. \qquad \textbf{(5.11)}$$

The determination of inverter A and inverter B duty-cycles exploits the same principle used in standard 2-level SVM. Considering that $\bar{e}_\gamma$ is a null vector and being α_A, β_A and γ_A respectively the duty-cycles of vectors $\bar{e}_\alpha$, $\bar{e}_\beta$ and $\bar{e}_\gamma$, (5.12) can be asserted.

$$\bar{e}_A^* = \alpha_A \bar{e}_\alpha + \beta_A \bar{e}_\beta . \qquad \textbf{(5.12)}$$

Before continuing the discussion it is better to specify that the definition of a duty-cycle for null vector, which does not appear in (5.12), is important in the determination of the application times of converter configurations. Hence it is preferred to introduce this parameter here. The way to determine α_A and β_A is well known: a little knowledge about vector algebra suggests to use the method of the reciprocal vector basis.

For any real base vector its reciprocal is univocally determined by two conditions: i) the dot product between the real and the reciprocal vectors must be 1, ii) the reciprocal vector must be perpendicular to all other vectors of the base. The reciprocal vectors of $\bar{e}_\alpha$ and $\bar{e}_\beta$ are given by (5.13).

$$\left\{\bar{e}_\alpha, \bar{e}_\beta\right\} \;\Leftrightarrow\; \left\{\frac{j\bar{e}_\beta}{\bar{e}_\alpha \cdot j\bar{e}_\beta}, -\frac{j\bar{e}_\alpha}{\bar{e}_\alpha \cdot j\bar{e}_\beta}\right\}. \qquad \textbf{(5.13)}$$

Making a dot product between both members of (5.12) and both reciprocal vectors leads to the determination of duty-cycles α_A and β_A. Obviously, even γ_A is determined because the sum of these three parameters is identically equal to 1. The duty-cycles of inverter A are given by (5.14).

$$\begin{cases} \alpha_A = \dfrac{\bar{e}_A^* \cdot j\bar{e}_\beta}{\bar{e}_\alpha \cdot j\bar{e}_\beta} \\ \beta_A = -\dfrac{\bar{e}_A^* \cdot j\bar{e}_\alpha}{\bar{e}_\alpha \cdot j\bar{e}_\beta} \\ \gamma_A = 1 - \alpha_A - \beta_A \end{cases} . \qquad \textbf{(5.14)}$$

The same procedure can be applied to determine inverter B duty-cycles α_B, β_B and γ_B respectively for vectors $\bar{e}_\alpha$, $\bar{e}_\beta$ and $\bar{e}_\gamma$. This leads to (5.15).

$$\begin{cases} \alpha_B = \dfrac{\bar{e}_B^* \cdot j\bar{e}_\beta}{\bar{e}_\alpha \cdot j\bar{e}_\beta} \\ \beta_B = -\dfrac{\bar{e}_B^* \cdot j\bar{e}_\alpha}{\bar{e}_\alpha \cdot j\bar{e}_\beta} \\ \gamma_B = 1 - \alpha_B - \beta_B \end{cases} . \qquad \textbf{(5.15)}$$

Unfortunately, the determination of the duty-cycles of the whole converter is harder than that of a single inverter. Being a, b and c the duty-cycles of the vectors $\bar{v}_A$, $\bar{v}_B$ and $\bar{v}_C$, (5.16) can be considered to make a general treatment.

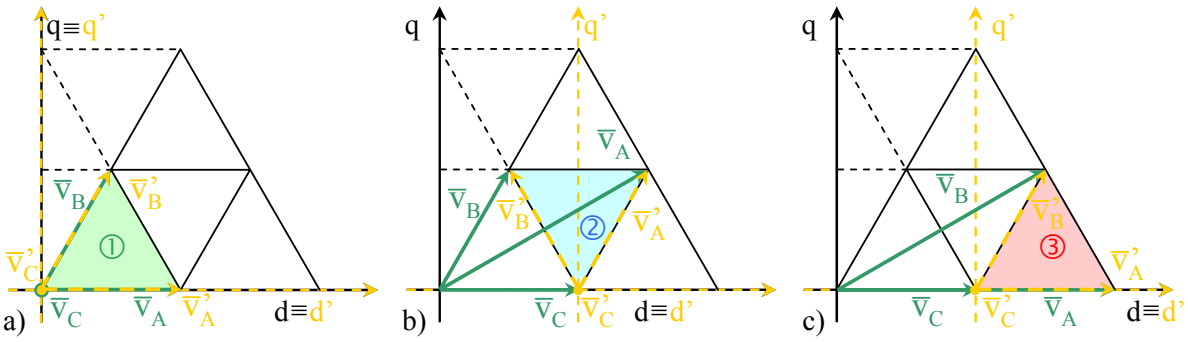


Figure 5.6: Determination of the duty-cycles of the whole converter. a) Region ①; b) Region ②; c) Region ③.

$$\bar{v}^* = a\bar{v}_A + b\bar{v}_B + c\bar{v}_C \,. \qquad \textbf{(5.16)}$$

Even if in Region ①, (5.16) can be simplified because $\bar{v}_C$ coincide with the null vector, in other regions this does not happen. Hence the reciprocal basis of the three vectors must be found, but it depends on the specific regions. Anyway, a general algorithm can be found, considering a translation of the axis as Figure 5.6 suggests. Figure 5.6a), b) and c) depict the situations representative of Region ①, Region ② and Region ③ respectively: the new axes considered are drown in yellow and are characterized by the prime symbol. The same happens for the vector in the new reference. Even if the translations in the three zone are different, the equations which will be written are the same. So, considering (5.16), the vector $\bar{v}_C$ can be subtracted from both members.

$$\bar{v}^* - \bar{v}_C = a\bar{v}_A + b\bar{v}_B + c\bar{v}_C - \bar{v}_C \,. \qquad \textbf{(5.17)}$$

The duty-cycles a, b and c must have their sum identically equal to 1, so the vector added to the second member can be multiplied for this quantity without changing (5.17).

$$\bar{v}^* - \bar{v}_C = a\left(\bar{v}_A - \bar{v}_C\right) + b\left(\bar{v}_B - \bar{v}_C\right) + c\left(\bar{v}_C - \bar{v}_C\right). \qquad \textbf{(5.18)}$$

Moreover, a set of new vectors can be defined:

$$\begin{cases} \bar{v}'^* = \bar{v}^* - \bar{v}_C \\ \bar{v}'_A = \left(\bar{v}_A - \bar{v}_C\right) \\ \bar{v}'_B = \left(\bar{v}_B - \bar{v}_C\right) \\ \bar{v}'_C = \left(\bar{v}_C - \bar{v}_C\right) \end{cases}. \qquad \textbf{(5.19)}$$

The vectors defined in (5.19) are the vectors in the new reference system and, as expected, their mathematical expression is independent of the Region in which the reference lays. Substituting (5.19) in (5.18) leads to one equations formally similar to (5.12).

$$\bar{v}'^* = a\bar{v}'_A + b\bar{v}'_B \,. \qquad \textbf{(5.20)}$$

To determine the two duty-cycles appearing in (5.20), the procedure described above for a single inverter can be used. The reciprocal basis can be defined and parameters a and b can be

found. Even the third duty-cycle is determined. Equation (5.20) gives the final expression for the three duty-cycles, in which the dependency on real vectors $\bar{v}^*$, $\bar{v}_A$, $\bar{v}_B$ and $\bar{v}_C$ is made explicit.

$$\begin{cases} a = \dfrac{(\bar{v}^* - \bar{v}_C)\cdot j(\bar{v}_B - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C)\cdot j(\bar{v}_B - \bar{v}_C)} \\ b = -\dfrac{(\bar{v}^* - \bar{v}_C)\cdot j(\bar{v}_A - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C)\cdot j(\bar{v}_B - \bar{v}_C)} \\ c = 1 - a - b \end{cases} . \qquad \textbf{(5.21)}$$

In this way, three sets of duty-cycles have been found, two of them are related to each single inverter, while the third one is related to the whole converter. The determination of the right application times of the configurations is possible using this parameters.

5.2.3. Limit of power sharing coefficient k

Considering the duty-cycles of both inverters constituting the dual 2-level converter, some boundaries must be provided. For any given couple of independent vectors in a 2-dimensional vector space, their span, using coefficients whose sum is less or equal to 1, is given by the set of vectors laying in the smallest convex region of the plane containing the initial vectors. With reference to Figure 5.7a), the smallest convex region containing vectors $\bar{e}_\alpha$ and $\bar{e}_\beta$ is given by the triangle having $\bar{e}_\alpha$, $\bar{e}_\beta$ and the segment between their tips as sides. In Figure 5.7a) the vector which can be synthesised by the inverter, $\bar{e}^*$, is represented, while in Figure 5.7b) another vector which is not allowed is drawn.

These boundaries on the vectors which can be synthesised can be mathematically formalized imposing that each duty-cycles is included between 0 and 1.

$$\begin{cases} 0 \le \alpha_A \le 1 \\ 0 \le \beta_A \le 1 \\ 0 \le \gamma_A \le 1 \\ 0 \le \alpha_B \le 1 \\ 0 \le \beta_B \le 1 \\ 0 \le \gamma_B \le 1 \end{cases} . \qquad \textbf{(5.22)}$$

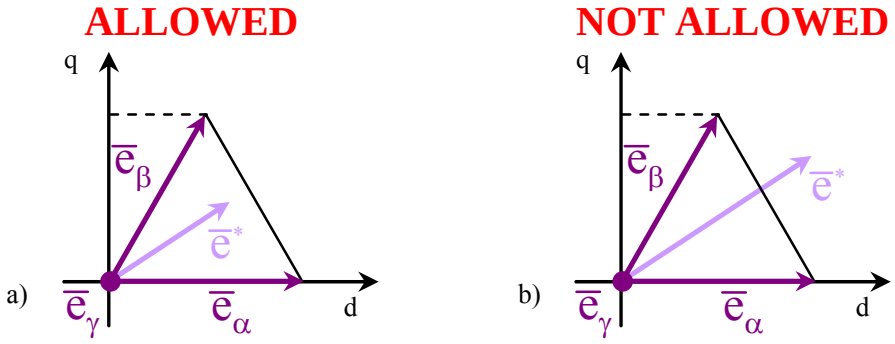


Figure 5.7: Limits of the vectors generable by a single inverter. a) Allowed output; b) Not allowed output.

The definition of duty-cycles given in (5.15) and (5.14), together to (5.11), can be substituted in the twelve inequalities presented in (5.22). Assuming $\bar{v}^* = v^* e^{j\theta^*}$ and considering that for each of the six Sectors the dot product $\bar{e}_\alpha \cdot j\bar{e}_\beta$ is equal to the constant $-\frac{\sqrt{3}}{2}u^2$, where u is the amplitude of the phasors, (5.23) can be asserted.

$$\begin{cases} k \le \frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\cos\left(\frac{5}{6}\pi-\theta^*\right)\right|} \\ k \le \frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\sin\left(\theta^*\right)\right|} \\ k \le \frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\cos\left(\frac{7}{6}\pi-\theta^*\right)\right|} \\ k \ge 1-\frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\cos\left(\frac{5}{6}\pi-\theta^*\right)\right|} \\ k \ge 1-\frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\sin\left(\theta^*\right)\right|} \\ k \ge 1-\frac{\sqrt{3}}{2}\frac{u}{v^*}\frac{1}{\left|\cos\left(\frac{7}{6}\pi-\theta^*\right)\right|} \end{cases} \quad \textbf{(5.23)}$$

In (5.23) there are only six inequalities because the others are less restrictive that the ones considered. The six inequalities depend on two parameters related to the reference, v^* and θ^*, whereas the amplitude u is only depending on the coefficient chosen for Park transform. The first three inequalities are related to the upper limit of power sharing coefficient k, while the last three are related to the lower limit. For any given reference $\bar{v}^*$, the limits of variation of parameter k are given by the most strict among the first three inequalities and the most strict among the last three.

In Figure 5.8a) all the six boundaries appearing in (5.23) are depicted for three different values of the **modulation index** m defined in (5.24).

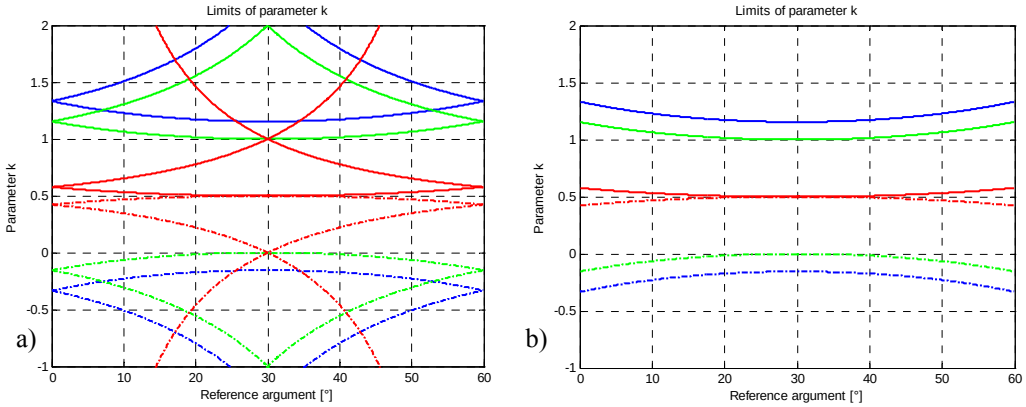


Figure 5.8: Limits of parameter k depending on the argument of the reference. a) All the six limits are drawn for three values of the modulation index: blue m=0.43, green m=0.5, red m=1. The solid line is referred to the upper limits, whereas the dash-dotted line is referred to lower limits; b) Most constraining upper and lower limits of k: blue m=0.43, green m=0.5, red m=1.

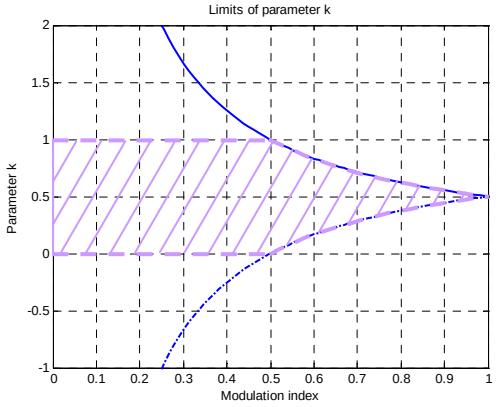


Figure 5.9: Limits of parameter k varying the modulation index.

$$m = \frac{\sqrt{3}\bar{v}^*}{2E}. \qquad \textbf{(5.24)}$$

In particular, the blue lines are calculated for a modulation index equal to 0.43, the green lines concerns the limits when $m = 0.5$, while the red lines are referred to $m = 1$. The solid lines represent the upper limits of k, whereas the lower limits are drawn in dash-dotted stile.

Among the upper and lower limits there are two that are the most constraining for any given value of θ^* and v^*: they are given by the third and the sixth of (5.23). These two limits are drawn in Figure 5.8b), for the values of the modulation index given above. Unfortunately, the most constraining upper and lower limits vary depending on reference argument, as Figure 5.8b) shows.

The calculus of the constrains of k can be a very hard duty for the controller, in particular if it is a fixed-point architecture, so it can be preferred to implement a limit which depends only by the modulation index. These limits are represented in Figure 5.9 with the blue lines.

Figure 5.9 shows that the range of variation of parameter k changes a lot depending on the modulation index: at low indices the allowed interval is quite large and it decreases to a single value when the modulation index is 1. in particular, when the modulation index m is less than 0.5, the power sharing coefficient k can assume values greater than 1 or negative. This means that inverter A can deliver a power greater than the load one or can absorb power. The same will happen for inverter B because of (5.4): when inverter A produces more power than the necessary, inverter B absorbs the superfluous and vice versa. This peculiarity of the dual 2-level inverter allows to use the power stored in one battery bank to recharge the other one and can find some application even for diesel engines balancing.

Actually, it has not been treated and simulated, assuming the violet lines of Figure 5.9 as boundary for power sharing coefficient k: the chosen limits avoid a transfer of power even at low modulation indices.

With reference to Figure 5.8b), the most constraining limit corresponds to an argument equal to 30°. In fact, among the maximum vectors generable by a single inverter, the one with argument 30° has the smallest modules as it could be inferred by Figure 5.7. So, (5.25) can be asserted assuming $u = \frac{2}{3}E$.

$$\begin{cases} k \le \dfrac{1}{2m} \\ k \ge 1 - \dfrac{1}{2m} \end{cases}. \qquad \textbf{(5.25)}$$

Equation (5.25) refers to the blue limits of Figure 5.9, a further limitation must be considered for m lesser than 0.5 to obtain the violet boundaries.

5.3. Multilevel operation

5.3.1. Determination of subduty-cycles

The definition of inverters references and duty-cycles is not enough to achieve a proper multilevel operation of the converter. A synchronisation between inverters commutation must be done. For instance, the two references $\bar{e}_A^*$ and $\bar{e}_B^*$ can be synthesised by the two inverters separately, using a standard 2-level SVM technique, but this will lead to a phase voltage waveform

	Region ①					Region ②						Region ③				
$\bar{v}$	$\bar{v}_A$		$\bar{v}_B$		$\bar{v}_C$	$\bar{v}_A$		$\bar{v}_B$		$\bar{v}_C$		$\bar{v}_A$	$\bar{v}_B$		$\bar{v}_C$	
$\bar{e}_A$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$
$\bar{e}_B$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\alpha$

Table 5.1: Redundant vectors generation used in power sharing modulation.

similar to the one achieved by the two references modulation seen in the previous Chapter: the converter will always use all the possible voltage levels and not only the necessaries.

A proper multilevel operation can be achieved exploiting the redundancies on the vectors generation peculiar of this converter. With reference to Figure 5.10, Table 5.1 reports the relationship between inverter A and B outputs and the vectors generated by the whole converter.

For instance, in Figure 5.10a), the vectors used to synthesise the load voltage vector are $\bar{v}_A$, $\bar{v}_B$ and $\bar{v}_C$ in Region ①; in this particular case they coincide with the vectors generable by a single inverter $\bar{e}_\alpha$, $\bar{e}_\beta$ and $\bar{e}_\gamma$. When one inverter generates an active vector, the other one must generate the null one as the first part of Table 5.1 shows. When the whole converter is demanded for a null vector, both inverters must generate their own null vector $\bar{e}_\gamma$ which can be obtained using two different configurations.

A similar consideration can be done for Region ③: in this case the inverters must generate the vector $\bar{e}_\alpha$ simultaneously, when the whole converter is demanded for vector $\bar{v}_A$ (with reference to Figure 5.10c)). Both in Region ① and ③, five different configurations of the whole converter can

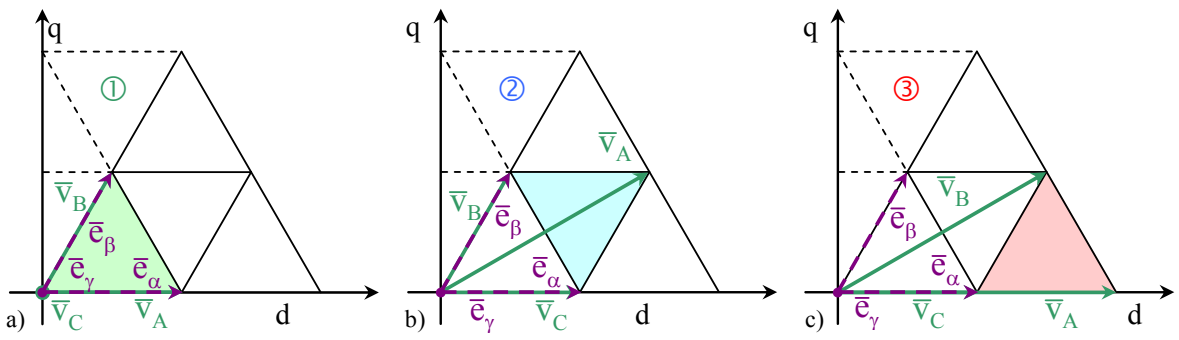


Figure 5.10: Redundant vectors generation used in power sharing, the vectors of the whole converter are drawn in green, whereas the vectors generated by each inverter are violet. a) Voltage vectors in Region ①; b) Voltage vectors in Region ②; c) Voltage vectors in Region ③.

be used.

Nevertheless, Region ② wander from the other two because there are two configurations for each vectors the whole converter can be demanded. So, there are six configurations to manage in Region ②: it will lead to an indefiniteness of the system of equations related to this region.

A further step can be done defining the switching sequences used for the SVM. To do this task, two principles have been taken into account: i) equally subdivide the commutation among all the legs composing the converter, ii) minimize the numbers of commutations the whole inverter has to do in the transition between two adjacent configurations.

In Table 5.2, the configurations presented in Table 5.1 are rearranged trying to have a single leg commutating at each step.

	Region ①					Region ②						Region ③				
$\bar{e}_A$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\gamma$			$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\beta$				$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$		
δ_A	α_A	β_A	γ_A			α_A	γ_A	β_A				γ_A	β_A	α_A		
δ_B	γ_B			β_B	α_B	γ_B	β_B		α_B	γ_B		α_B			β_B	γ_B
$\bar{e}_B$	$\bar{e}_\gamma$			$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\beta$		$\bar{e}_\alpha$	$\bar{e}_\gamma$		$\bar{e}_\alpha$			$\bar{e}_\beta$	$\bar{e}_\gamma$
$\bar{v}$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$
δ	a'	b'	c	b''	a''	c'	a'	b'	c''	a''	b''	c'	b'	a'	b''	c''

Table 5.2: Switching sequence base for the three Regions.

Unfortunately, this is achieved for Region ① and Region ③, but not for Region ②: the second step of inverter A, is applying the null vector $\bar{e}_\gamma$ which can be linked to one of the two active vectors. In this point avoiding a double commutation is impossible and will be discussed in the following. By now, it is necessary to determine the application time of each configuration. This operation can easily be done considering Table 5.2 and express their dependency on inverters duty-cycles.

Equation (5.26) gives the **subduty-cycles** a', a'', b', b'' and c proper of Region ①: parameters a', a'', b' and b'' are found as function of inverter duty-cycles, whereas c is directly one duty-cycle of the whole converter.

$$\begin{cases} a' = \alpha_A \\ a'' = \alpha_B \\ b' = \beta_A \\ b'' = \beta_B \\ c \text{ is known} \end{cases} . \qquad \textbf{(5.26)}$$

Considering Region ②, the system of equation given in (5.27) can be obtained which characterize the relationship among a', a'', b', b'', c', c'' and the duty-cycles found in the previous Section for the two inverters.

$$\begin{cases} a'+c' = \alpha_A \\ a''+b'' = \beta_A \\ b'+c'' = \gamma_A \\ a''+c'' = \alpha_B \\ a'+b' = \beta_B \\ b''+c' = \gamma_B \end{cases} . \qquad \textbf{(5.27)}$$

In the same way as Region ① , subduty-cycles a , b′ , b″ , c′ and c″ characterizing Region ③ are given by (5.28). Even in this case, one parameter coincides with a duty-cycle of the whole converter.

$$\begin{cases} a \text{ is known} \\ b' = \beta_A \\ b'' = \beta_B \\ c' = \gamma_A \\ c'' = \gamma_B \end{cases} . \qquad \textbf{(5.28)}$$

To obtain the desired application times, the calculated subduty-cycles must be multiplied for the SVM period.

5.3.2. Indefiniteness of region 2

Considering Region ②, (5.27) must to be solved to obtain the values of the subduty-cycles. Unfortunately, this system of equations is indefinite: adding all the six equations and considering the properties of the duty-cycles an identity is obtained. Hence, (5.27)can be parameterized using one of the six subduty-cycles, for instance c' . This leads to (5.29).

$$\begin{cases} a' = \alpha_A - c' \\ a'' = \beta_A - \gamma_B + c' \\ b' = \beta_A - \alpha_A + c' \\ b'' = \gamma_B - c' \\ c'' = \alpha_B - \beta_A + \gamma_B - c' \end{cases} . \qquad \textbf{(5.29)}$$

Obviously, even the range of variation of parameter c' can not sweep all the real values, but are limited by the condition that all the six subduty-cycled must be included between 0 and 1, as any other duty-cycle. Imposing these conditions leads to a system of twelve inequalities which depend on $\bar{v}^*$ and k. Anyway, only six among the twelve inequalities are the most constraining for each values of $\bar{v}^*$ and k.

$$\begin{cases} c' \geq 0 \\ c' \geq \gamma_B - \beta_A \\ c' \geq \alpha_A - \beta_B \end{cases} \qquad \begin{cases} c' \leq \alpha_A \\ c' \leq \gamma_B \\ c' \leq \alpha_B + \gamma_B - \beta_A \end{cases} . \qquad \textbf{(5.30)}$$

Dependently on the actual values of $\bar{v}^*$ and k, the most constraining inequalities among the first and the second group of (5.30) must be found to catch the boundaries. This is a hard task, especially before the substitution of (5.24), (5.14) and (5.21). In the final implementation, it was preferred to calculate the duty-cycles and then find the boundaries of parameter c' in each period.

Some examples of boundaries over parameter c' are depict in Figure 5.11. Figure 5.11a) shows the limits given by (5.30) varying reference angle θ^* with power sharing coefficient equal to 0.5 and a reference amplitude of $\frac{\sqrt{3}}{2}E$. The inequalities of the first group are represented by solid lines, whereas the ones of the second group are associated to dash-dot lines. For any given θ^*, the most

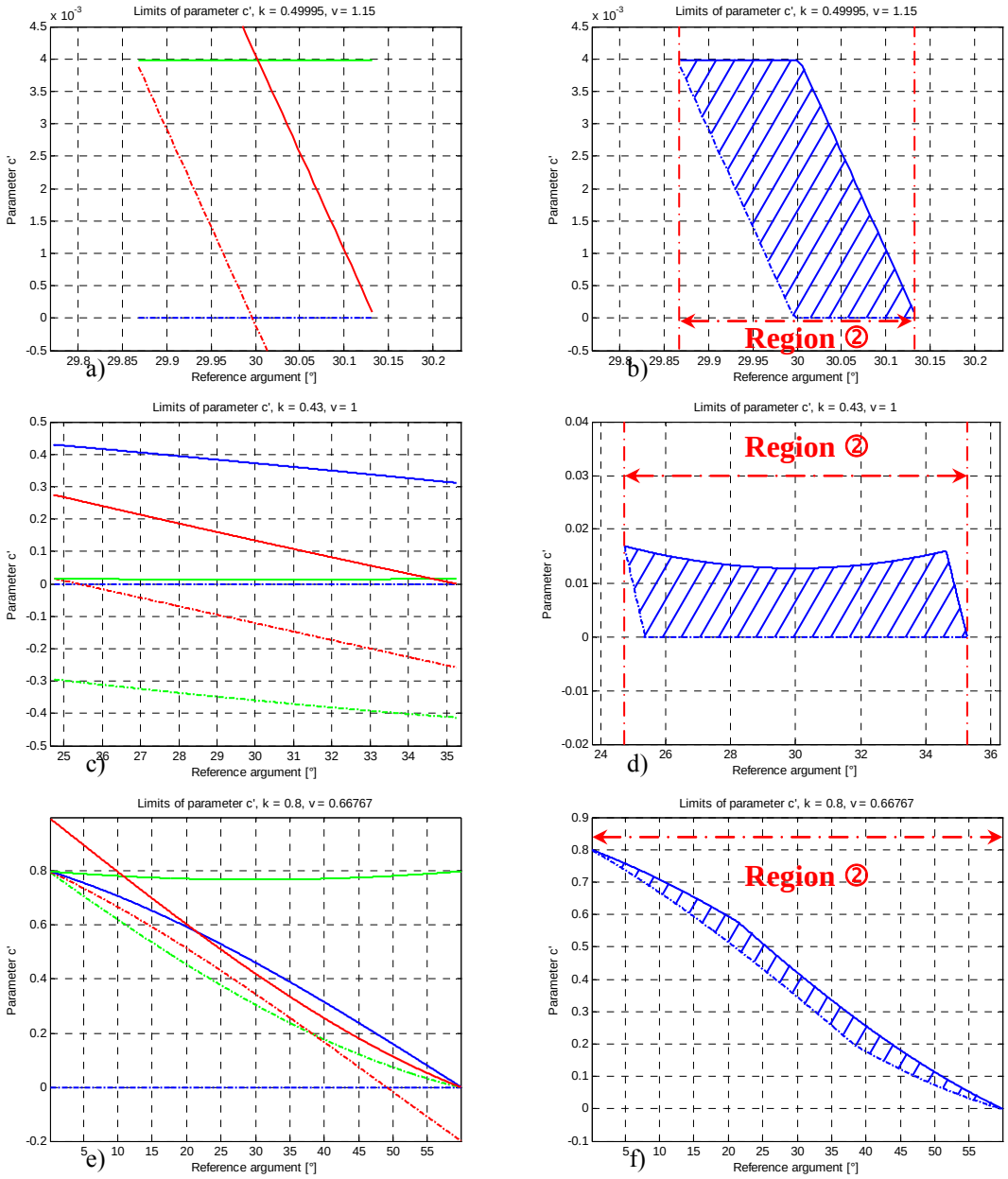


Figure 5.11: Limit of parameter c' as function of reference angle q. a) Fundamental limits with k=0.5 and v=1.15E; b) Most constraining limits with k=0.5 and v=1.15E; c) Fundamental limits with k=0.43 and v=E; d) Most constraining limits with k=0.43 and v=E; e) Fundamental limits with k=0.8 and v=0.667E; f) Most constraining limits with k=0.8 and v=0.667E.

constraining limits define two curves drawn in Figure 5.11b). The dashed area represents the set of admissible values for the parameter c'. Figure 5.11c) represents the six limits in a different situation: now k is equal to 0.43 and the reference amplitude is E. Among these six lines, only the two represented in Figure 5.11d) are the limits of variation for parameter c'. Even in this case the dashed area is the set of allowed value for the parameter. Figure 5.11e) and f) are related to $k = 0.5$ and $v^* = \frac{2}{3}$. In this case Region ② is 60° wide. Figure 5.11e) depicts all the six limits, whereas the most constraining boundaries are shown Figure 5.11f).

Considering Figure 5.11b), d) and f), it is possible to understand how narrow and different are the boundaries over parameter c' varying θ^*: this lead to a difficult implementation, in particular with a fixed point architecture because a little error in the calculation can lead to a value of c' outside the limits.

The limits over parameter c' come from the inequalities which impose that each subduty-cycles must be greater or equal to 0. This means that for any given k and $\bar{v}^*$, one subdyty-cycle is zeroed when c' coincides with one of its limits, reducing the switching sequence presented in Table 5.2 to five steps like in other Regions.

5.3.3. Switching tables construction

$\bar{v}$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\gamma$		$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\gamma$				$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	
s_{1A}	0	0	1	1	1	1	1	1	1	1	0	0
s_{2A}	0	0	0	1	1	1	1	1	1	0	0	0
s_{3A}	0	0	0	0	1	1	1	1	0	0	0	0
s_{1B}	0	0	0	0	0	0	0	1	1	1	1	0
s_{2B}	0	0	0	0	0	0	1	1	1	1	1	1
s_{3B}	1	0	0	0	0	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\beta$	$\bar{e}_\gamma$				$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$				$\bar{e}_\alpha$

Table 5.3: Switching table for Region ①.

Before having determined the subduty-cycles for the configurations presented in Table 5.2, more complex switching tables can be constructed to give more continuity to the adjacent configurations as well as the passage from 5-step to 7-step in standard 3-phase SVM.

Considering Region ①, Table 5.3 reports the switching table used when the reference lays on this zone. Each leg of the six composing the dual 2-level inverter commutates at the same mean frequency: in a cycle each leg changes state twice.

$\bar{v}$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$
$\bar{e}_A$	$\bar{e}_\alpha$		$\bar{e}_\gamma$		$\bar{e}_\beta$				$\bar{e}_\gamma$		$\bar{e}_\alpha$	
s_{1A}	1	1	0	0	1	1	1	1	1	1	1	1
s_{2A}	0	0	0	0	1	1	1	1	1	1	0	0
s_{3A}	0	0	0	0	0	0	0	0	1	1	0	0
s_{1B}	0	0	0	0	0	1	1	0	0	0	0	0
s_{2B}	0	0	0	1	1	1	1	1	1	0	0	0
s_{3B}	0	1	1	1	1	1	1	1	1	1	1	0
$\bar{e}_B$	$\bar{e}_\gamma$	$\bar{e}_\beta$		$\bar{e}_\alpha$	$\bar{e}_\gamma$		$\bar{e}_\alpha$		$\bar{e}_\beta$			$\bar{e}_\gamma$

Table 5.4: Switching table for Region ②.

Moreover, it is possible to see that all the commutations take place involving a single leg. This means that, during dead times, the output coincide with the previous or the next vector, but both of them are allowed for a proper multilevel modulation.

In Table 5.4 the switching table chosen for Region ② is shown. Even the switching table for this Region the mean switching frequencies of each leg are the same, but there are some problem concerning the number of legs involved in the commutations.

Indeed, considering the configurations highlighted with red states in Table 5.4, it is clear that the commutations take place changing the states of two legs at the same time. This has repercussions on the output voltage during dead times, which can be a vector outside the set of the admissible ones as discussed on the next section. It is possible to change this switching table, exploiting the possibility

$\bar{v}$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\gamma$	$\bar{e}_\alpha$					$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$		
s_{1A}	0	1	1	1	1	1	1	1	1	1	1	1
s_{2A}	0	0	0	0	0	0	1	1	1	0	0	0
s_{3A}	0	0	0	0	0	0	0	1	0	0	0	0
s_{1B}	0	0	0	0	0	0	0	0	0	0	1	0
s_{2B}	1	1	0	0	0	1	1	1	1	1	1	1
s_{3B}	1	1	1	0	1	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\alpha$		$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$					$\bar{e}_\gamma$	$\bar{e}_\alpha$

Table 5.5: Switching table for Region ③.

to zero the application time of one configuration, but this method is not yet implemented in a real set-up neither in simulation.

Table 5.5 concerns Region ③. The switching table for this Region is very close to the one found for Region ①, but obviously, the applied vectors are different.

As Region ①, Table 5.5 keeps the same switching frequency for all the six legs and requires a single leg commutating at each step.

To conclude this Section, a general specification must be done: the switching tables which have been presented are composed by twelve steps, but only six subduty-cycles are available. A careful analysis of Table 5.3, Table 5.4 and Table 5.5 will show that each configuration appears two times, so the six subduty-cycles can be split in two equal parts to achieve the application times. For the proposed switching tables.

5.4. Dead-times effects

5.4.1. Double commutation effects

In real systems, dead-times have to be used to avoid DC bus short-cuts due to the different turn-on and turn-off delays of IGBTs. The introduction of dead times adds to the ideal sequence a short time interval in which the output voltage is not imposed by the converter state, but by load currents.

In Table 5.4, it has been seen there are two commutations which involve two legs. In the ideal case, there is no problem in this kind of switching tables because the commutations are considered instantaneous, so the converter passes from a defined state to another defined state.

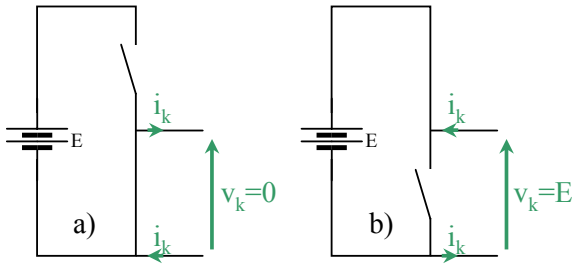


Figure 5.12: Leg output during dead times. a) When the current is being drawn from the leg the output is 0; b) When the current is entering in the leg the output is E.

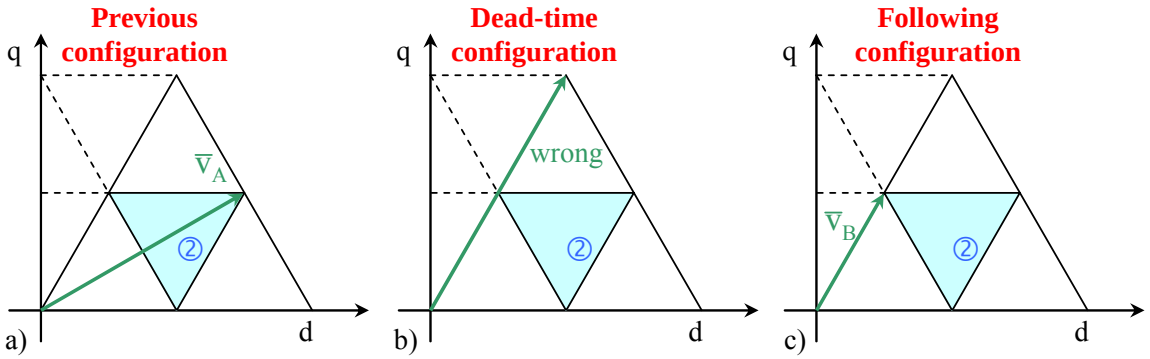


Figure 5.13: Example of dead-time effect on the output. a) Output before dead-time; b) Output during dead-time; c) Output after dead-time.

Figure 5.12 shows the effect of dead times on leg output. In Figure 5.12a) is depicted the electrical circuit existing when the current is being drawn from the leg which will be considered positive in follow discussion. In this case the current passes through the lower diode and the output is zero. In Figure 5.12b) the opposite case is shown. Here the current is entering the leg and it will be considered negative. The current passes through the upper diode and the DC sources, so the leg output is equal to E.

When only one leg is involved in the commutation, dead-times delays or anticipates output changes. Dependently on the current direction, the output will be the one before or after dead-time: both of them belong to the set of allowed voltage vectors and this situation will not give any problem but a different mean value of the output itself.

When two legs are involved in commutation, the indefiniteness of the output during dead-times may lead to apply wrong voltage vectors to the load, meaning the load voltages will be affected by spikes. Figure 5.13 gives an example of what may happen using vector representation. Figure 5.13a) shows the state of the converter before the dead-time: the voltage vector $\bar{v}_A$, which belongs to the set of correct vectors, is applied. Figure 5.13b) depicts the situation during dead-time in which a vector outside the correct ones is output. This creates voltage spikes in two phases at least. After dead-time, when the output is imposed by the switch state again, the correct output $\bar{v}_B$ is given as Figure 5.13c) shows.

5.4.2. Analysis of different configurations

The double commutations in Table 5.4 can be deeply analysed to understand which kind of effects dead-times have. The first double commutation in the switching table involves two legs

	$\bar{v}_C$	Unknown	$\bar{v}_A$
States	$\bar{e}_\gamma$	Unknown	$\bar{e}_\beta$
s_{1A}	0	x_1	1
s_{2A}	0	x_2	1
s_{3A}	0	0	0
s_{1B}	0	0	0
s_{2B}	1	1	1
s_{3B}	1	1	1
States	$\bar{e}_\alpha$	$\bar{e}_\alpha$	$\bar{e}_\alpha$

Table 5.6: First kind of double commutation.

belonging to the same inverter but in different phases. The output of inverter A passes from the null vector, related to $\bar{e}_\alpha$, to the active vector $\bar{e}_\beta$ making phase 1 and phase 2 commutate at the same time. The configurations before and after the dead-time are shown in Table 5.6. The column in the between represents the configuration the inverter assumes during dead-time: the indefiniteness of inverter state is highlighted using the two variable x_1 and x_2 which may assume the values 0 or 1 dependently on current directions.

Because the directions of two independent currents have to be taken into consideration, four cases must be analysed. The conditions which lead to these four cases are given by (5.31).

$$\begin{array}{llll} i) & \begin{array}{l} i_1 > 0 \Rightarrow x_1 = 0 \\ i_2 > 0 \Rightarrow x_2 = 0 \end{array} & ii) & \begin{array}{l} i_1 > 0 \Rightarrow x_1 = 0 \\ i_2 < 0 \Rightarrow x_2 = 1 \end{array} \\ iii) & \begin{array}{l} i_1 < 0 \Rightarrow x_1 = 1 \\ i_2 > 0 \Rightarrow x_2 = 0 \end{array} & iv) & \begin{array}{l} i_1 < 0 \Rightarrow x_1 = 1 \\ i_2 < 0 \Rightarrow x_2 = 1 \end{array} \end{array} . \qquad \textbf{(5.31)}$$

During dead-time, a different output vector is obtained for each one of the four cases just shown. To find out the output voltage vector, the values assumed by x_1 and x_2 can be substituted in the undetermined configuration. Table 5.7 reports all the four possible states the dual 2-level inverter can assume.

	i)	*ii*)	*iii*)	*iv*)
	$\bar{v}_C$	$\bar{v}_B$	$2\bar{e}_\alpha$	$\bar{v}_A$
$\bar{v}_A$	$\bar{e}_\gamma$	$ue^{j\frac{2}{3}\pi}$	$\bar{e}_\alpha$	$\bar{e}_\beta$
s_{1A}	0	0	1	1
s_{2A}	0	1	0	1
s_{3A}	0	0	0	0
s_{1B}	0	0	0	0
s_{2B}	1	1	1	1
s_{3B}	1	1	1	1
$\bar{v}_B$	$\bar{e}_\alpha$	$\bar{e}_\alpha$	$\bar{e}_\alpha$	$\bar{e}_\alpha$
Allowed	**OK**	**OK**	**NO**	**OK**

Table 5.7: The four possible configurations during dead-time in the first kind of double commutation.

In particular, the whole converter outputs are shown in the second row. Three configurations produce an admissible output vector. The first and the fourth configurations give the same outputs as before or after the dead-time. The second configuration generates another admissible vector, but some spikes can be present on the load voltages. Anyway, these spikes are limited in amplitude and can be accepted. The configuration that is completely wrong is the third one which produces an output vector outside the set of the correct ones.

The conditions on the currents of phase 1 and phase 2 which lead to the wrong configurations are summarized in (5.32).

$$(i_1 < 0) \wedge (i_2 > 0). \qquad \textbf{(5.32)}$$

In Figure 5.14 a vector representation of the current conditions expressed by the previous equation is given. In this picture phase 1 and phase 2 axes are drawn in light-blue and in orange

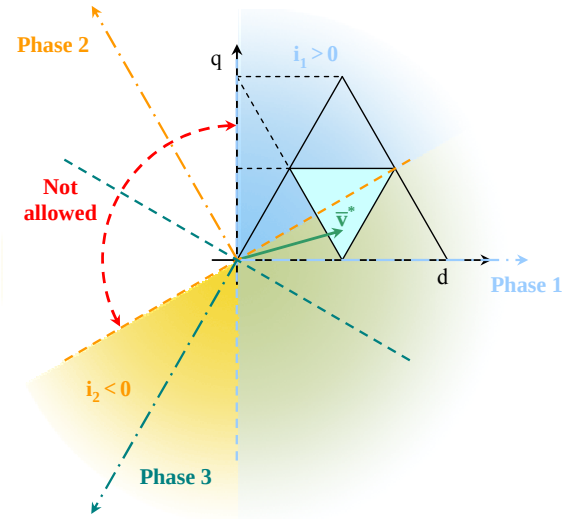


Figure 5.14: First kind of double commutation. Vector representation of load current conditions highlighting the slice of plane in which the current vector must lay to generate admissible voltage vectors during dead time.

respectively. For any given value of the load current vector $\bar{i}$, its component on each phase can be found projecting it on phase axes. Hence, it is possible to identify the region of plane where a particular condition on the phase currents must exist.

The half-plane in which i_1 is greater that 0 is filled in light-blue and the half-plane where i_2 is negative is filled in orange. Their intersection is filled with the fusion of both colours. Hence, the slice of plane in which (5.32) can be asserted is not filled at all. If the current vector lays in this slice, during dead-time in the commutation analysed, a wrong voltage vector will be certainly applied.

	$\bar{v}_B$	Unknown	$\bar{v}_A$
States	$\bar{e}_\gamma$	Unknown	$\bar{e}_\alpha$
s_{1A}	1	1	1
s_{2A}	1	x_2	0
s_{3A}	1	x_3	0
s_{1B}	0	0	0
s_{2B}	0	0	0
s_{3B}	1	1	1
States	$\bar{e}_\beta$	$\bar{e}_\beta$	$\bar{e}_\beta$

Table 5.8: Second kind of double commutation.

A similar analysis can be done for the second double commutation of Table 5.4. This commutation involves phase 2 and phase 3 legs of inverter A which must commutate simultaneously. Table 5.8 shows the configurations of the dual 2-level inverter just before and just after the commutation takes place. The middle column depicts the configuration during dead-time.

Even in this case two phases have an undefined state which depends on the direction of the currents through phase 2 and phase 3. All the four possible cases are given by (5.33).

$$
\begin{array}{llll}
i) & \begin{array}{l} i_2 > 0 \Rightarrow x_2 = 0 \\ i_3 > 0 \Rightarrow x_3 = 0 \end{array} & ii) & \begin{array}{l} i_2 > 0 \Rightarrow x_2 = 0 \\ i_3 < 0 \Rightarrow x_3 = 1 \end{array} \\
iii) & \begin{array}{l} i_2 < 0 \Rightarrow x_2 = 1 \\ i_3 > 0 \Rightarrow x_3 = 0 \end{array} & iv) & \begin{array}{l} i_2 < 0 \Rightarrow x_2 = 1 \\ i_3 < 0 \Rightarrow x_3 = 1 \end{array}
\end{array} \quad . \qquad \textbf{(5.33)}
$$

Table 5.9 reports in detail all the possible configurations the dual 2-level inverter can assume in front of the different states of the legs.

	i)	*ii)*	*iii)*	*iv)*
	$\bar{v}_A$	$\bar{v}_B$	$2\bar{e}_\beta$	$\bar{v}_C$
$\bar{v}_A$	$\bar{e}_\alpha$	$ue^{j\frac{2}{3}\pi}$	$\bar{e}_\beta$	$\bar{e}_\gamma$
s_{1A}	1	1	1	1
s_{2A}	0	0	1	1
s_{3A}	0	1	0	1
s_{1B}	0	0	0	0
s_{2B}	0	0	0	0
s_{3B}	1	1	1	1
$\bar{v}_B$	$\bar{e}_\beta$	$\bar{e}_\beta$	$\bar{e}_\beta$	$\bar{e}_\beta$
Allowed	**OK**	**OK**	**NO**	**OK**

Table 5.9: The four possible configurations during dead-times in the second kind of double commutation.

Even in this case there are three configurations which generate an output vector belonging to the set of the correct ones. In particular the first and the fourth configurations produce output voltages which are respectively the one before and the one after dead-time. As in the previous case, the second configuration generates an admissible output voltage, even if it can produce some spikes. On the contrary, the third is not admissible at all.

In Figure 5.15 the slices of d-q plane in which the current vector can lay without giving problems are filled in orange and green. Respectively, in the orange region i_2 is positive and in the

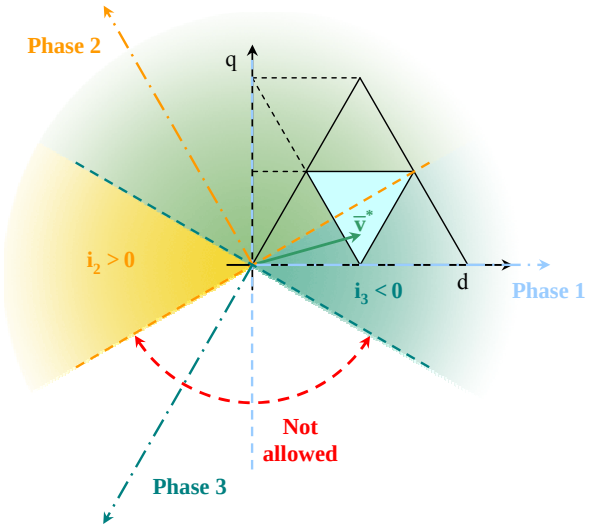


Figure 5.15: Second kind of double commutation. Vector representation of load current conditions highlighting the slice of plane in which the current vector must lay to generate admissible voltage vectors during dead time.

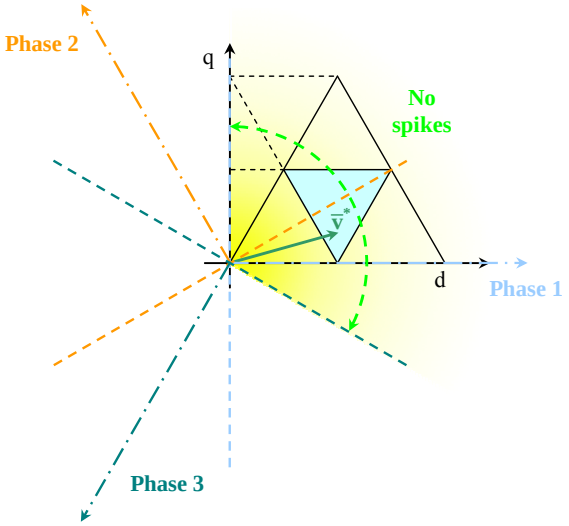


Figure 5.16: Slice of d-q plane in which the current vector can lay without producing not allowed voltage output during dead-times.

green one i_3 is negative. If the current vector lays in the slice not filled, then there will be spikes during dead-times.

In Figure 5.14 and Figure 5.15 the limits of current vector admissibility have been found. To avoid wrong configurations in the whole switching table presented in Table 5.4, the current vector must lay in the intersection of the two slices.

This region is filled with yellow in Figure 5.16. It is important to underline that the line of argument just described is related to Sector I, so the reference voltage vector must lay in the azurine triangle. Considering the worst cases, the current may lead or lack the voltage reference of no more than 30° without producing not allowed vectors.

Certainly, the analysis of all the other odd Sectors can be retraced to the one of Sector I due to symmetry reasons. Some doubts can be allowed for the even Sectors, but proceeding with the same line of argument will lead to similar conclusions. After having built the switching table for Sector II with the same vector sequence as Table 5.4 and having found out the two double commutations there will be, it is possible to catch the conditions on the current to generate an allowed vectors

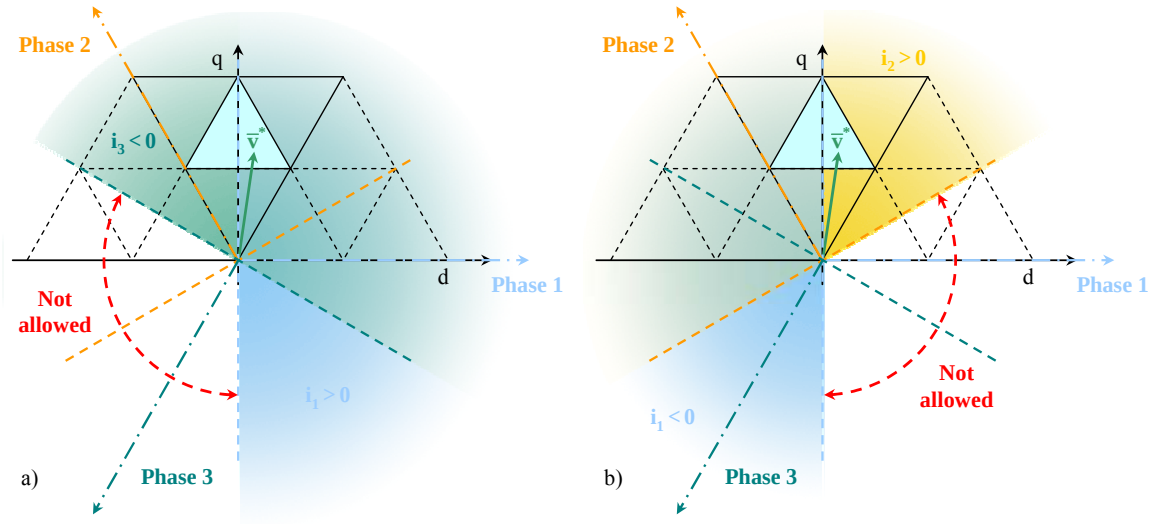


Figure 5.17: Vector representation of load current conditions highlighting the slice of plane in which the current vector must lay to generate admissible voltage vectors during dead time for Sector II. a) First double commutation; b) Second double commutation.

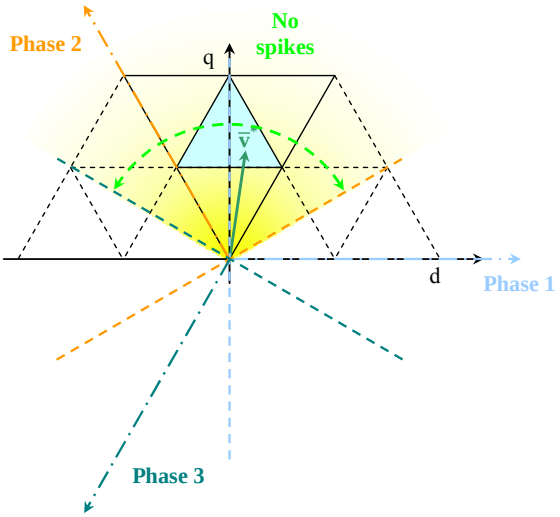


Figure 5.18: : Slice of d-q plane in which the current vector can lay without producing not allowed voltage output during dead-times for Sector II.

during dead-times in both the double commutations. These conditions are depicted by Figure 5.17a) and b), respectively for the first and the second double commutation.

The intersection of the slices found for both commutations is the region of d-q plane in which the current vector may lay without producing not allowed outputs during dead-times. This region is filled with yellow in Figure 5.18. Even in this case the current vector can lead or lack the voltage reference of no more than 30° without producing any wrong voltage vectors during dead-times.

5.4.3. Other possibilities

Table 5.4 can be rearranged, but two double commutations are intrinsically present. It is possible to build a switching table with the same kinds of double commutations as Table 5.4 in inverter B. The analysis of this switching table does not add anything new to the previous discussion.

Anyway there is the possibility to separate the double commutation between the two inverters, as shown in Table 5.10.

$\bar{v}$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$
$\bar{e}_A$	$\bar{e}_\beta$	$\bar{e}_\alpha$		$\bar{e}_\beta$	$\bar{e}_\gamma$				$\bar{e}_\beta$	$\bar{e}_\alpha$		$\bar{e}_\beta$
s_{1A}	1	1	1	1	1	1	1	1	1	1	1	1
s_{2A}	1	0	0	1	1	1	1	1	1	0	0	1
s_{3A}	0	0	0	0	1	1	1	1	0	0	0	0
s_{1B}	0	0	0	0	0	0	0	0	0	0	0	0
s_{2B}	0	0	0	1	1	0	0	1	1	0	0	0
s_{3B}	0	0	1	1	1	1	1	1	1	1	0	0
$\bar{e}_B$	$\bar{e}_\gamma$		$\bar{e}_\beta$	$\bar{e}_\alpha$		$\bar{e}_\beta$		$\bar{e}_\alpha$		$\bar{e}_\beta$	$\bar{e}_\gamma$	

Table 5.10: Alternative switching table for Region ②.

Unfortunately, a fast glance at this switching table shows that the switching frequencies of the six legs are not the same, and this could have an important consequence on converter performances. Moreover, the analysis of double commutations reveals some regrettable aspects. Indeed, the legs involved in the first double commutation belong to the different inverters, but to the same phase. This means that the state assumed by the two leg are mutually dependent, in particular if the current

enters in one inverter will be drawn from the other. Hence, the state of the two legs must be opposite: only two cases are possible. The two possible configurations can be assumed are summarized in Table 5.11.

	$\bar{v}_A$	Unknown	$\bar{v}_A$
States	$\bar{e}_\alpha$	Unknown	$\bar{e}_\beta$
s_{1A}	1	1	1
s_{2A}	0	x_{2A}	1
s_{3A}	0	0	0
s_{1B}	0	0	0
s_{2B}	0	x_{2B}	1
s_{3B}	1	1	1
States	$\bar{e}_\beta$	Unknown	$\bar{e}_\alpha$

Table 5.11: Third kind of double commutation. One commutation in each inverter.

Assuming that the phase current i_2 is positive when it is drawn from inverter A, (5.34) expresses its relationship with the leg states.

$$i)\quad i_2 > 0 \Rightarrow \begin{matrix} x_{2A} = 0 \\ x_{2B} = 1 \end{matrix} \qquad ii)\quad i_2 < 0 \Rightarrow \begin{matrix} x_{2A} = 1 \\ x_{2B} = 0 \end{matrix}. \qquad \textbf{(5.34)}$$

Unfortunately, during dead-times, the dual 2-level inverter produces an output vector not allowed in both conditions, $i_2 > 0$ and $i_2 < 0$. The output is $2\bar{e}_\alpha$, when the current is positive, whereas it is equal to $2\bar{e}_\beta$, when the current is negative. Both vectors clearly do not belong to the set of correct one for Region ②.

The same line of reasoning can be conducted for the other double commutation. Even in this commutation the legs involved belong to the same phase and their states during dead-time will be opposite. In Table 5.12 the transition constituting the second double commutation is shown.

	$\bar{v}_A$	Unknown	$\bar{v}_A$
States	$\bar{e}_\beta$	Unknown	$\bar{e}_\alpha$
s_{1A}	1	1	1
s_{2A}	1	x_{2A}	0
s_{3A}	0	0	0
s_{1B}	0	0	0
s_{2B}	1	x_{2B}	0
s_{3B}	1	1	1
States	$\bar{e}_\alpha$	Unknown	$\bar{e}_\beta$

Table 5.12: Fourth kind of double commutation. One commutation in each inverter.

It can be seen that this transition happens in the opposite direction of the previous one. It can be demonstrated that the conditions deriving from a particular commutation are the same deriving from the opposite transition. Hence, even in this commutation the current imposes a wrong output vector during dead-times.

To conclude, the switching table presented in Table 5.4 is the best solution has been found, however it is possible that better solution could exist. Indeed , this switching table imposes the same switching frequency to all the legs and allow to generate acceptable voltage vectors during dead-times if the load current is no more that 30° out of phase in the respect of the synthesised voltage. In other cases some spikes will be present.

5.5. Six-step implementation

5.5.1. Power sharing achievement

Another way to implement power sharing is exploiting the last modulation seen in the previous Chapter. A six-step operation is imposed to one inverter, whereas the other one is made commutate at high frequency to synthesise the different between the reference and the output of the first inverter. This modulation can even be implemented in a digital way: one switching table can be built for each region.

In the discussion of this modulation all the four triangles belonging to a Sector will be analysed separately to quantify the powers delivered by the inverters, but a general analysis can be done to determine how the inverter share the power. For this purpose, Table 5.13 can be considered.

$\bar{e}_A$	$\bar{v}^* - \bar{v}_C$	$\bar{v}_C$
$\bar{e}_B$	$\bar{v}_C$	$\bar{v}^* - \bar{v}_C$
Application time	ξT_S	$(1-\xi)T_S$

Table 5.13: Application times of mean vectors.

The first row represent inverter A operations: in the first part of the period T_S it synthesises the vector corresponding to the difference between reference $\bar{v}^*$ and the vector $\bar{v}_C$, in the second part it constantly produces the vector $\bar{v}_C$. Inverter B operates in the same way, but in reverse order. To

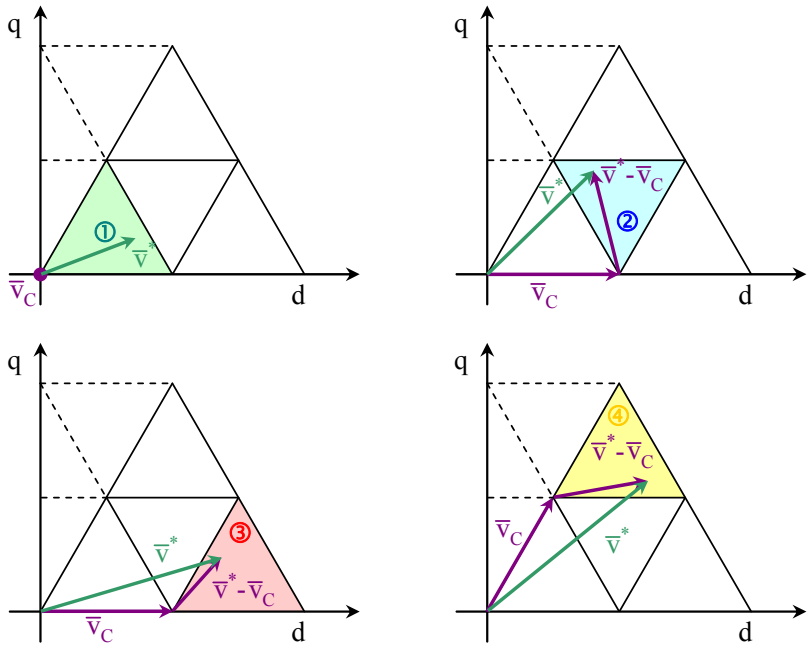


Figure 5.19: Characterisation of the voltage vectors dependently on the Region.

share the power, the parameter ξ has been introduced as the ratio between the period T_S and the first part. Varying parameter ξ implies changing the duration of the two parts in which the period has been decomposed. This means varying the mean vectors the two inverter synthesise and the powers they deliver. The characterisation of the voltage vectors presented in Table 5.13 for the four Regions is given in Figure 5.19.

The mathematical expressions of the mean vectors produced in a period by the two inverters are given by (5.35).

$$\begin{cases} \bar{e}_A = \xi\left(\bar{v}^* - \bar{v}_C\right) + \left(1-\xi\right)\bar{v}_C \\ \bar{e}_B = \xi\bar{v}_C + \left(1-\xi\right)\left(\bar{v}^* - \bar{v}_C\right) \end{cases}. \qquad \textbf{(5.35)}$$

As expected, the outputs produced by the inverters depend on the parameter ξ. Managing (5.35), (5.36) can be obtained.

$$\begin{cases} \bar{e}_A = \xi\bar{v}^* + \left(1-2\xi\right)\bar{v}_C \\ \bar{e}_B = \left(1-\xi\right)\bar{v}^* + \left(2\xi-1\right)\bar{v}_C \end{cases}. \qquad \textbf{(5.36)}$$

The power delivered by the two inverters can be found as the dot product of the current vector $\bar{i}$, which is the same for both the inverters, and the voltage vectors they produce which can be out of phase. Being p_A and p_B respectively the power delivered by inverter A and inverter B, (5.37) can be asserted.

$$\begin{cases} p_A = \frac{3}{2}\left(\bar{e}_A \cdot \bar{i}\right) = \frac{3}{2}\left[\xi\left(\bar{v}^* \cdot \bar{i}\right) + \left(1-2\xi\right)\left(\bar{v}_C \cdot \bar{i}\right)\right] \\ p_B = \frac{3}{2}\left(\bar{e}_B \cdot \bar{i}\right) = \frac{3}{2}\left[\left(1-\xi\right)\left(\bar{v}^* \cdot \bar{i}\right) - \left(1-2\xi\right)\left(\bar{v}_C \cdot \bar{i}\right)\right] \end{cases}. \qquad \textbf{(5.37)}$$

The powers delivered by the two inverters are composed by two quantities: the first one is a fraction of the total power and the second is the same for both inverters (in one case it is added and in the other case it is subtracted). In (5.38) the total power p and the mutual power are defined.

$$\begin{cases} p = \frac{3}{2}\left(\bar{v}^* \cdot \bar{i}\right) \\ p_m = \frac{3}{2}\left(\bar{v}_C \cdot \bar{i}\right) \end{cases}. \qquad \textbf{(5.38)}$$

Substituting (5.38) in (5.37), a compact relationship can be found.

$$\begin{cases} p_A = \xi p + \left(1-2\xi\right)p_m \\ p_B = \left(1-\xi\right)p - \left(1-2\xi\right)p_m \end{cases}. \qquad \textbf{(5.39)}$$

Equation (5.39) clearly shows how controlling parameter ξ allows the sharing of the powers delivered by the two inverters. In this case, the range of variation is well defined: parameter ξ can assume any value between 0 and 1. Unfortunately, the functions expressing the relationships between ξ and the power delivered by the two inverters are quite complicated.

5.5.2. Analysis of delivered powers

The analysis of delivered powers must be conducted referring to a particular triangle. Before starting the characterisation of delivered power, some definitions will be given. The reference vector $\bar{v}^*$ can be expressed using the polar form, as well as the current vector.

$$\bar{v}^* = v^* e^{j\theta^*} \qquad \bar{i} = i e^{j\psi} . \tag{5.40}$$

The vector $\bar{v}_C$, which depends on the triangle in which the reference vector lays, can be defined using the following equation, where the amplitude u can assume the values 0 or 1 and the argument θ_C can assume the values 0° and 60°.

$$\bar{v}_C = \frac{2u}{3} E e^{j\theta_C} . \tag{5.41}$$

Moreover, the modulation index can be used to define the amplitude of the reference and to simplify the equations. Using the modulation index, (5.40) becomes:

$$\bar{v}^* = \frac{2E}{\sqrt{3}} m e^{j\theta^*} . \tag{5.42}$$

Introducing (5.42), (5.41) and (5.40) in (5.38) a new expression of the total and mutual power can be found.

$$\begin{cases} p = \sqrt{3} m\, i\, E \cos(\theta^* - \psi) \\ p_m = u\, i\, E \cos(\theta_C - \psi) \end{cases} . \tag{5.43}$$

Substituting (5.43) in (5.39) leads to the equation which will be characterized for the four regions.

$$\begin{cases} p_A = iE\left[\sqrt{3} m \xi \cos(\theta^* - \psi) + u(1-2\xi)\cos(\theta_C - \psi)\right] \\ p_B = iE\left[\sqrt{3} m (1-\xi)\cos(\theta^* - \psi) - u(1-2\xi)\cos(\theta_C - \psi)\right] \end{cases} . \tag{5.44}$$

Considering Region ①, the vector $\bar{v}_C$ coincides with the null vector, so $u = 0$. Substituting this in (5.44) leads to the equations characteristics of this Region.

$$\begin{cases} p_A = iE\sqrt{3} m \xi \cos(\theta^* - \psi) \\ p_B = iE\sqrt{3} m (1-\xi)\cos(\theta^* - \psi) \end{cases} . \tag{5.45}$$

Region ② and ③ have the same conditions on the vector $\bar{v}_C$. For both Regions u is equal to 1 and the angle θ_C is zero.

$$\begin{cases} p_A = iE\left[\sqrt{3} m \xi \cos(\theta^* - \psi) + (1-2\xi)\cos(\psi)\right] \\ p_B = iE\left[\sqrt{3} m (1-\xi)\cos(\theta^* - \psi) - (1-2\xi)\cos(\psi)\right] \end{cases} . \tag{5.46}$$

Finally, in Region ④ the vector $\bar{v}_C$ is defined by an amplitude u equal to 1 and an argument θ_C equal to $\pi/3$ radians. This leads to (5.47).

$$\begin{cases} p_A = iE\left[\sqrt{3}m\xi\cos\left(\theta^* - \psi\right) + \left(1-2\xi\right)\cos\left(\frac{\pi}{3} - \psi\right)\right] \\ p_B = iE\left[\sqrt{3}m\left(1-\xi\right)\cos\left(\theta^* - \psi\right) - \left(1-2\xi\right)\cos\left(\frac{\pi}{3} - \psi\right)\right] \end{cases}. \quad \textbf{(5.47)}$$

Table 5.14 summarizes all the equations found for the power delivered by the inverters in the different Regions.

	u	θ_C	Powers
①	0	NA	$p_A = iE\sqrt{3}m\xi\cos\left(\theta^* - \psi\right)$
			$p_B = iE\sqrt{3}m\left(1-\xi\right)\cos\left(\theta^* - \psi\right)$
②	1	0	$p_A = iE\left[\sqrt{3}m\xi\cos\left(\theta^* - \psi\right) + \left(1-2\xi\right)\cos\left(\psi\right)\right]$
			$p_B = iE\left[\sqrt{3}m\left(1-\xi\right)\cos\left(\theta^* - \psi\right) - \left(1-2\xi\right)\cos\left(\psi\right)\right]$
③	1	0	$p_A = iE\left[\sqrt{3}m\xi\cos\left(\theta^* - \psi\right) + \left(1-2\xi\right)\cos\left(\psi\right)\right]$
			$p_B = iE\left[\sqrt{3}m\left(1-\xi\right)\cos\left(\theta^* - \psi\right) - \left(1-2\xi\right)\cos\left(\psi\right)\right]$
④	1	$\frac{\pi}{3}$	$p_A = iE\left[\sqrt{3}m\xi\cos\left(\theta^* - \psi\right) + \left(1-2\xi\right)\cos\left(\frac{\pi}{3} - \psi\right)\right]$
			$p_B = iE\left[\sqrt{3}m\left(1-\xi\right)\cos\left(\theta^* - \psi\right) - \left(1-2\xi\right)\cos\left(\frac{\pi}{3} - \psi\right)\right]$

Table 5.14: Delivered powers in the four Regions.

5.5.3. Limits of delivered power

Using Matlab, some graphics have been drawn to make clear how this power sharing methodology works. When the modulation index is less than 0.5, only Region ① is crossed by the reference. Hence, only (5.45) is used meaning the power is shared proportionally to the coefficient ξ. For all the following figures the DC sources give 100 V and the current has an amplitude of 10 A lagging the voltage of 30°. Figure 5.20a) shows the powers delivered by the two inverters with a

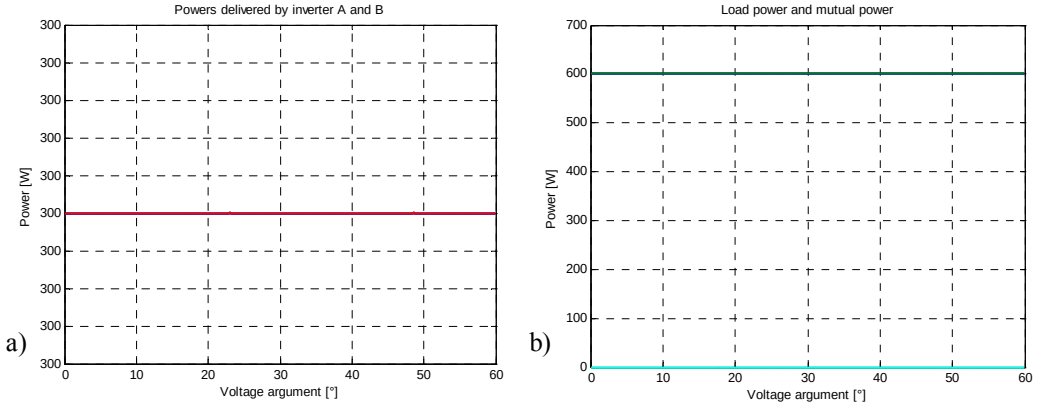


Figure 5.20: Power sharing with a modulation index of 0.4 and coefficient ξ equal to 0.5. The current is lagging the voltage of 30°. a) Powers delivered by the two inverters, blue line is inverter A power, red line is inverter B power; b) Load power (green line) and mutual power (cyan line).

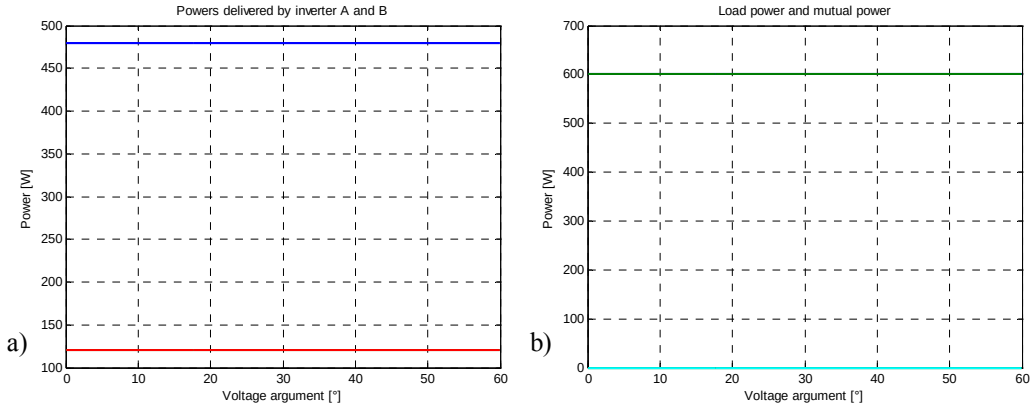


Figure 5.21: Power sharing with a modulation index of 0.4 and coefficient ξ equal to 0.8. The current is lagging the voltage of 30°. a) Powers delivered by the two inverters, blue line is inverter A power, red line is inverter B power; b) Load power (green line) and mutual power (cyan line).

modulation index equal to 0.4 and a coefficient $\xi = 0.5$. The red and the blue lines coincide and both inverters deliver 300 W which correspond to half the load power. Figure 5.20b) shows the load power (green line) and the mutual power (cyan line). Because the reference is in Region ① the mutual power is zero.

Figure 5.21a) depicts the delivered powers in the same conditions as the precious case, but with a coefficient ξ equal to 0.8. Now the power delivered by inverter A is higher than the power

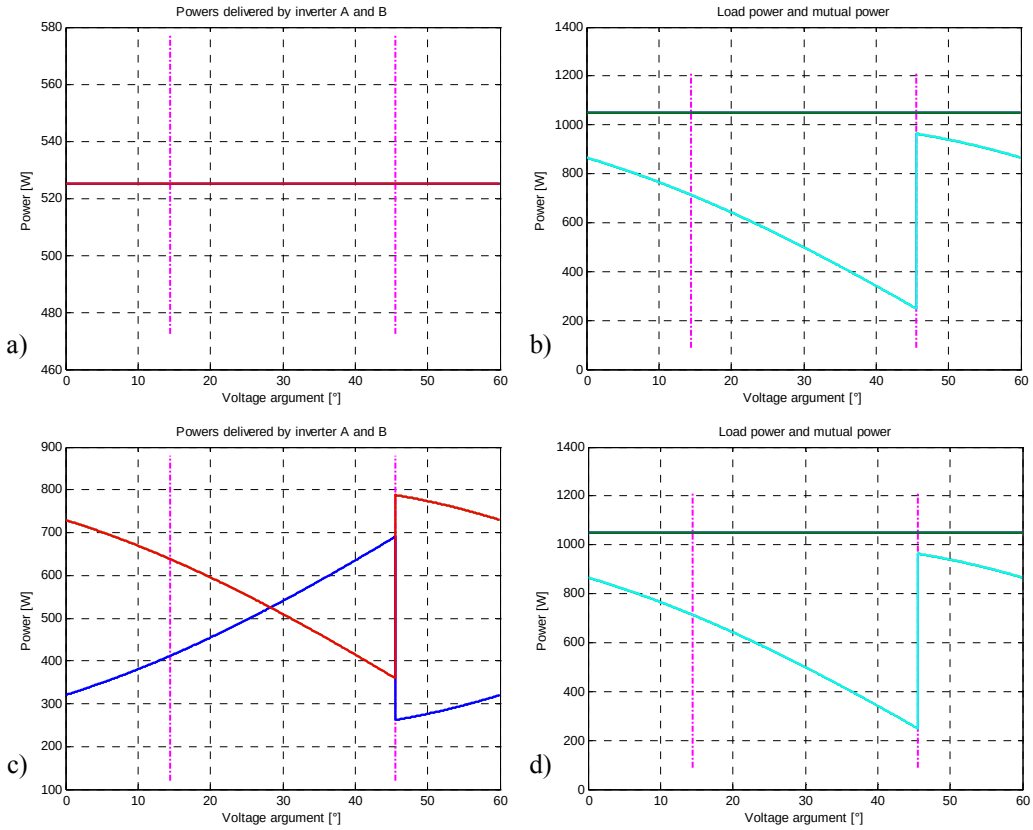


Figure 5.22: Power sharing with the modulation index equal to 0.7. a) Power delivered by inverter A (blue) and inverter B (red) with a coefficient ξ equal to 0.5; b) Load power (green) and mutual power (cyan) with a coefficient ξ equal to 0.5; c) Power delivered by inverter A (blue) and inverter B (red) with a coefficient ξ equal to 0.8; d) Load power (green) and mutual power (cyan) with a coefficient ξ equal to 0.8.

delivered by inverter B. In particular, inverter A supplies 480 W, whereas inverter B supplies 120 W. The load power and the mutual are not affected by the different value of coefficient, as Figure 5.21b) shows.

Figure 5.22 is related to a modulation index equal to 0.7, so the reference crosses the three outermost Regions (②, ③ and ④). The magenta dash-dotted lines outline the three Regions. Figure 5.22a) represents the delivered powers when $\xi = 0.5$, so the two inverters equally share the load power and the coefficient which multiply the mutual power in (5.44) is zero. Anyway, when the reference is not in the inner region, the mutual power is different from zero, as Figure 5.22b) shows. A discontinuity can be noticed in the mutual power. To understand the reason of this, it has to be considered that the reference crosses Regions ③, ② and ④ passing from the left to the right. The vector $\overline{v}_C$ is the same for both Regions ② and ③, but is changes for Region ④ inducing the discontinuity. The same happens on the delivered power when the coefficient ξ is equal to 0.8 as shown in Figure 5.22c). In this case the delivered power are composed by either a part of load power and a part of mutual power creating the blue and the red lines in Figure 5.22c). Unfortunately, the delivered power are no more proportional to coefficient ξ. Moreover, in this case, augmenting ξ means decreasing inverter A power in opposition to the two cases with modulation index equal to 0.4. The average powers delivered by inverter A and inverter B are respectively 439 W and 610 W. As expected by (5.43), the load power and the mutual power do not change in front of a modification of coefficient ξ: Figure 5.22d) and b) represent the same quantities.

Figure 5.23 shows the powers delivered by the two inverters when the modulation index is equal

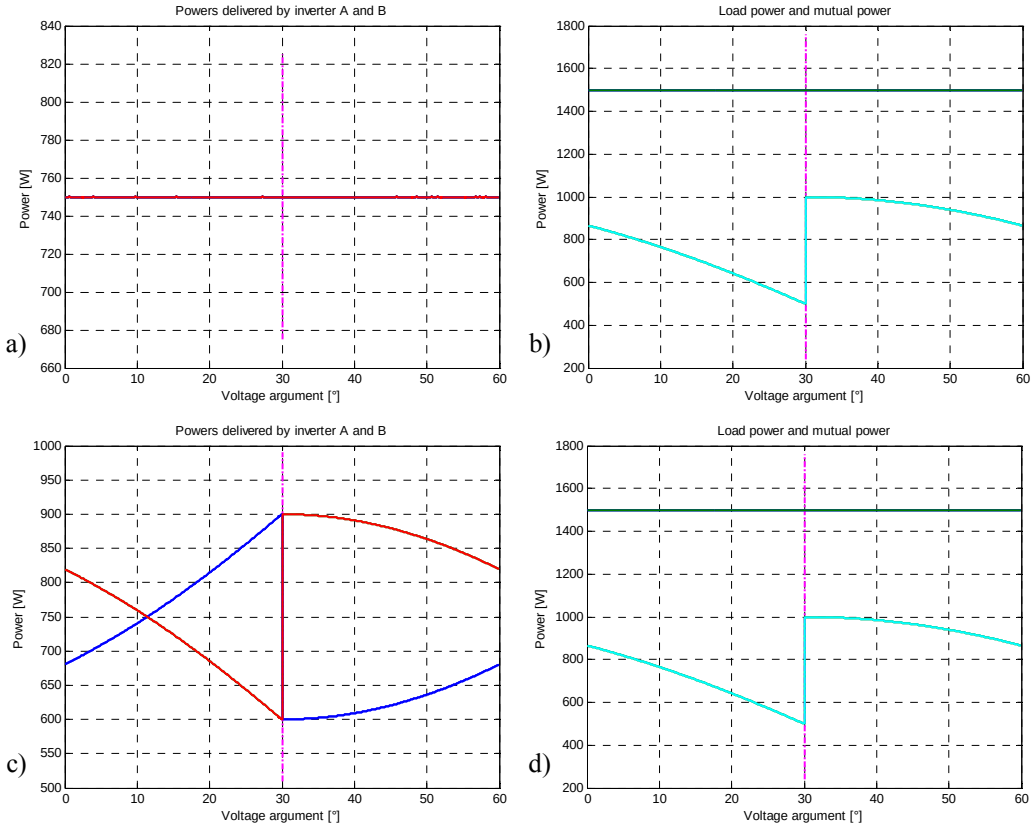


Figure 5.23: Power sharing with the modulation index equal to 1. a) Power delivered by inverter A (blue) and inverter B (red) with a coefficient ξ equal to 0.5; b) Load power (green) and mutual power (cyan) with a coefficient ξ equal to 0.5; c) Power delivered by inverter A (blue) and inverter B (red) with a coefficient ξ equal to 0.8; d) Load power (green) and mutual power (cyan) with a coefficient ξ equal to 0.8.

to 1, meaning that the maximum rotating vector is synthesised. In the pictures there is a magenta line which divides Region ③ by Region ④. Figure 5.23a) shows the delivered power when the converter is demanded for ξ equal to 0.5. Both inverters deliver the same power which is not affected by the discontinuity on the mutual power. Figure 5.23b) shows the load power and the mutual power in the same conditions as Figure 5.23a). Figure 5.23c) depicts the delivered powers when the coefficient ξ is equal to 0.8. The mutual power gives a contribution to the delivered powers which now present the discontinuity. Even in this case Figure 5.23d) and b) show the same quantities because the load power and the mutual power are not affected by parameter ξ.

Chapter 6

Power sharing simulations

6.1. Introduction

6.1.1. Simulation environment

The power sharing technique described in the previous Chapter has been implemented in Matlab Simulink. The choice of this environment was made due to its simplicity because the aim of simulations were to prove the effectiveness of the power sharing algorithm rather than to examine the effects of switching tables on voltage and current throughout the switches during commutations.

Simulink offers an embedded set of tools (**SimPowerSystems**) for the simulation of electrical systems which was used to build converter circuits. Even if SimPowerSystems tool is not so accurate as pSpice can be, it offers an easy way to simulate both system and control circuits. Indeed, Simulink standard blocks can be used to implement the control algorithm and they can be easily connected to SimPowerSystems blocks (Figure 6.1).

In this way, the control algorithm is easy to implement and well integrated with the circuit it has to gate. On the contrary, making the control circuit in pSpice could be very difficult because it is an environment devoted only to circuit simulation. Certainly pSpice makes a more precise estimation of currents and voltages in the circuit, but it requires a lot of time spent in planning how to control the system. Moreover, pSpice is a quite time expensive environment because it uses a lot of disk space to store all the signals in the netlilst.

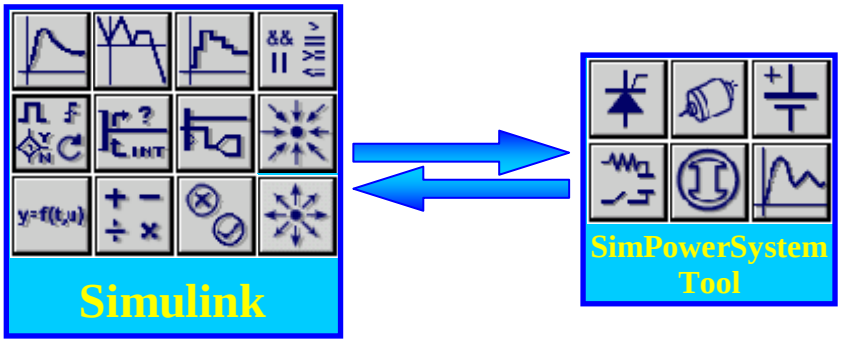


Figure 6.1: Graphical example of the interconnection between Simulink and SimPowerSystem tool used in the simulation of the dual 2-level inverter.

For these reasons, Matlab-Simulink was preferred to other simulation software.

6.1.2. Simulink S-Function

An interesting block of Simulink environment is **S-Function** (Figure 6.2): this block was born specifically to implement continuous and discrete systems in the input-state-output form. Hence, Matlab user can employ S-Functions to describe systems which are not present in Simulink library writing them in M-code. The simplicity of M-code and S-Function structure allows the user to make up the simulation easily and quickly.

Unfortunately, in the simulation of the dual 2-level inverter the S-Function block must simulate something that has no input-state-output form. In the present simulation, S-Function block has to simulate what a DSP (or any other kind of controller) does in the real system. Using a code quite close to the algorithm implemented on DSP, the S-Function block must control the dual 2-level inverter in the same way as a DSP does. This means, the S-Function must change its outputs every time a commutation is necessary and must read its inputs once a period.

To do this task, S-Function has been configured as variable discrete time block and called every time its outputs, the gating signals, change. Moreover, S-Function reads inputs and calculates application times at every beginning of the period. In this way, S-Function block and DSP have the same behaviour for an external observer if they are considered as two impenetrable black boxes.

Furthermore, M-code is high-level programming language, quite near to the C-code used to program **Texas Instruments** (**TI**) DSP. Hence passing from C/C++ to M-code or vice versa is very easy and can be done without altering the algorithm implemented.

A further step has been done connecting the DSP directly to Simulink environment using the **CCSDSP** built-in function. This function can be called inside an S-Function to open a channel to a DSP using **Code Composer Studio** (**CCS**) environment. Simulink talks with CCS which is controlling the DSP: in this way information can be exchanged between Simulink and DSP. Obviously, this kind of connection requires a lot of time and simulations of few seconds may last a

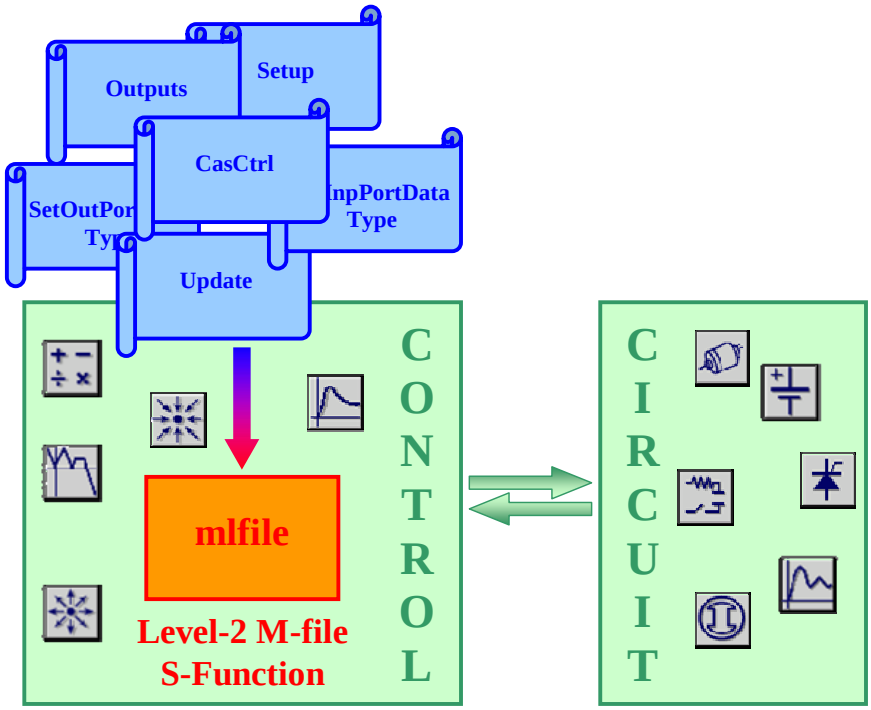


Figure 6.2: S-Function allows to use m-file to describe systems. Using some shrewdness it is possible to use the S-Function code to generate a control algorithm quite close to the one implemented on DSP.

day long, but allows a fast analysis and debugging of the code implemented on the DSP even if the hardware is not yet built.

6.2. Algorithm implementation

6.2.1. System overview

The dual 2-level inverter was born to be controlled by a digital controller; in particular it is a TMS320C2812 digital signal processor. Hence, DSP must be given sufficient time to make all the calculations choosing a proper interval of time, in the following called **cycle**. This concept of cycle is taken into account even in the simulation using the S-Function properties.

The whole control algorithm is based on the Park transform of the quantities involved in the dual 2-level inverter. Hence, the voltage reference the control generates by itself is a rotating vector. The first task the control has to do is to determine the position of the reference in each cycle. To do this, a particular map of the d-q plane has been done as shown in the next Section.

Knowing the reference position the calculation of duty cycles and the determination of the switching tables to be used are possible. Hence the control can generate the six gating signals which are directed to the two inverters.

The two inverters are made using SimPowerSystems toolbox. In this toolbox several components can be found like diodes, IGBTs, SCRs, and so on. Ideal switch was used to build the dual 2-level inverter in order to minimize the effects related to commutations. Anyway, the snubber circuit which is inside every switch model of SimPowerSystems can create some side effects affecting current waveforms.

Two of this power circuits compose each leg and both inverters are composed by three legs. The middle point of each leg is connected to the load which is built using SimPowerSystems inborn blocks. The 3-phase load is symmetric and composed by an R-L series to emulate the most common passive loads which can be found.

Some measurements are done over the voltages and the currents involved in the dual 2-level inverter. In particular DC bus voltages and currents are fed-back to the control algorithm for further implementation of the closed loop regulation of the DC bus voltages themselves.

All the main points discussed in this section are schematically represented in Figure 6.3, which gives a fast idea of how the system has been implemented in Matlab-Simulink environment.

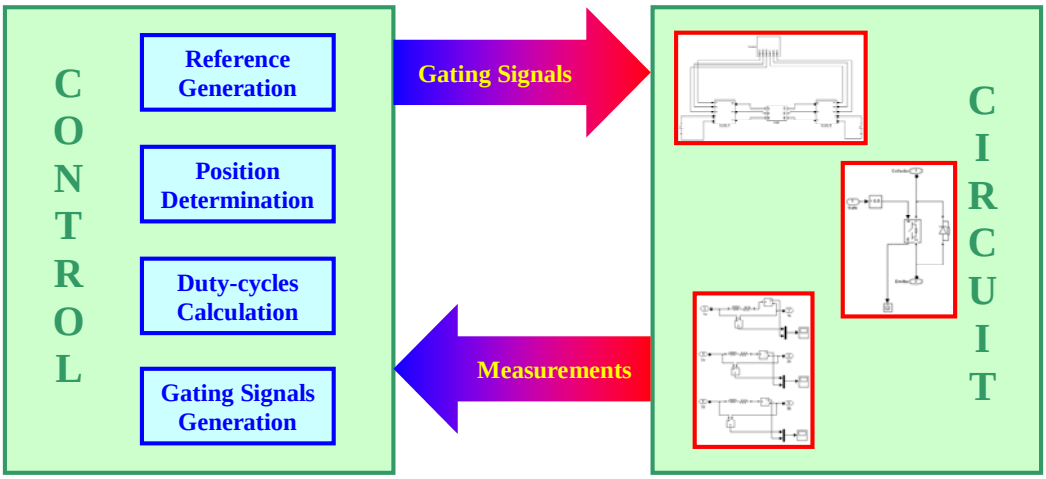


Figure 6.3: General description of the system implemented in simulation.

6.2.2. Determination of reference position

The first task the control algorithm has to do is to determine the position of the voltage reference on the d-q plane. In the simulation of dual 2-level inverter, the control algorithm itself generates the reference, but in a more complex system the reference can be given by a close loop feed-back and its position may be unknown.

The information associated to the position are critical to choose the switching table to be used in the synthesis of the output voltage. Moreover, the calculations involved in its determination must be as fast as possible to occupy the shortest time.

The proposed algorithm for position determination is based on two steps, graphically represented in Figure 6.4. The first step consists in comparing the whole reference with the six Sectors shown in Figure 6.4a). As it is possible to see in the picture, each fundamental active vector, drawn in orange, is bisector of one Sector. For instance, considering the green vector $\bar{v}^*$ as a possible reference, it is laying in the Sector number 1 associated to active vector $\bar{v}_1$.

The second step is to determine the position of the vector which is the difference between the reference and the active vector associated to the Sector just determined. This vector has to be compared with the Sectors depicted in Figure 6.4b) which are rotated 30° anticlockwise in the respect of the Sectors considered in the first step. Continuing the example, the difference between the reference $\bar{v}^*$ and the active vector $\bar{v}_1$ is given by the small green vector in Figure 6.4b) which lays in Sector number 5.

In this case, it is possible to conclude that the position of the reference in the d-q plane is univocally determined by the couple of numbers (1, 5). To simplify the notation, in the following will be used only a dot between the first and the second number, so the position given by (1, 5) will be written as 1.5.

Considering all the possible cases, a hexagonal grid can be filled as shown in Figure 6.5. The different colours used to represent the labels can be useful to quickly distinguish the different Regions.

As can be observed there are some triangles with two labels associated, like 1.2/2.6. If this redundancy can give problems, relationship of equivalence can be found. For instance can be used some table to store the equivalence of position 1.2 with position 2.6 and so on.

Otherwise, there are sets equations which express this equality. In this case it is necessary to distinguish between the innermost triangles and the outer ones because the relationships are

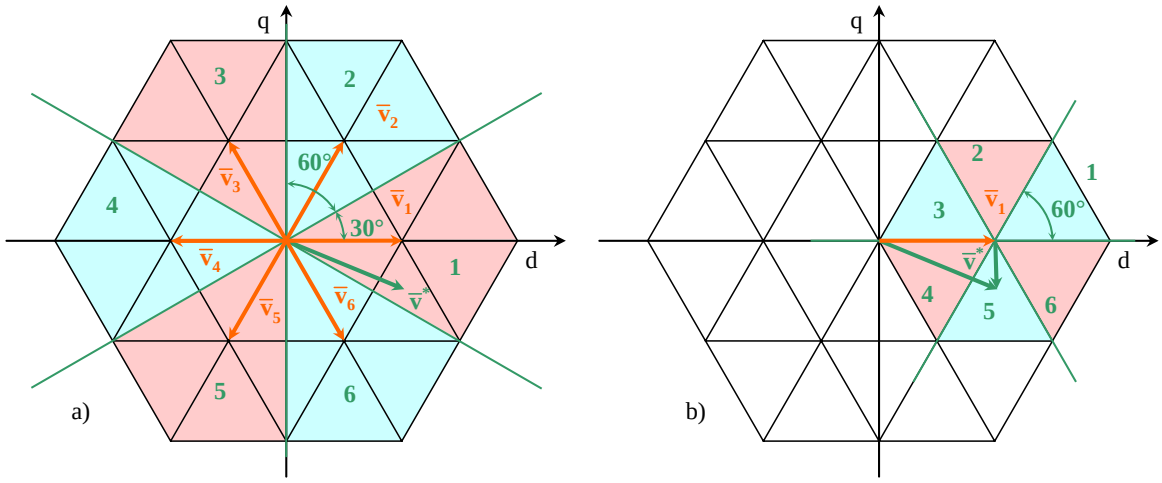


Figure 6.4: Algorithm used to determine the position of voltage reference. a) First identification step using Sectors centred on the six inner vectors; b) Second identification step using Sectors which have active vectors as sides.

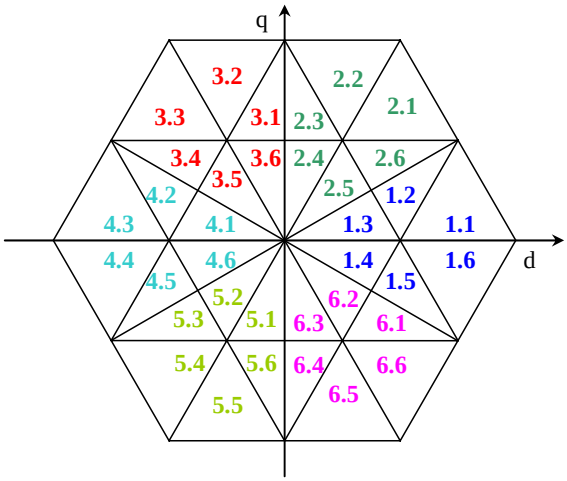


Figure 6.5: Denomination of the zones using the proposed algorithm. Unfortunately there are several triangular regions which have more than one label.

different. For instance, with reference to the triangle defined by the two labels 1.2 and 2.6, it can be noticed that the first number is increased by 1 and the second by 4 when rotating anticlockwise.

This relationship can be extended to any given couple of equivalent labels in the outer triangles if the calculus are done in modulus 6, i.e. considering that the sum of 4 and 3 is 1 instead of 7.

Innermost triangles have similar relationship between two equivalent labels: in this case the first number is increased by 1 and the second by 2 when rotating anticlockwise.

6.2.3. Schematic description of the system

The model of the dual 2-level inverter implemented in Matlab-Simulink is shown in Figure 6.6. The green block is the 3-phase symmetric load connected to the two blocks representing the two inverters. All the grey blocks belong to the control circuit. There is a block which generates the voltage reference passed to the S-Function as a complex number split in real and imaginary parts.

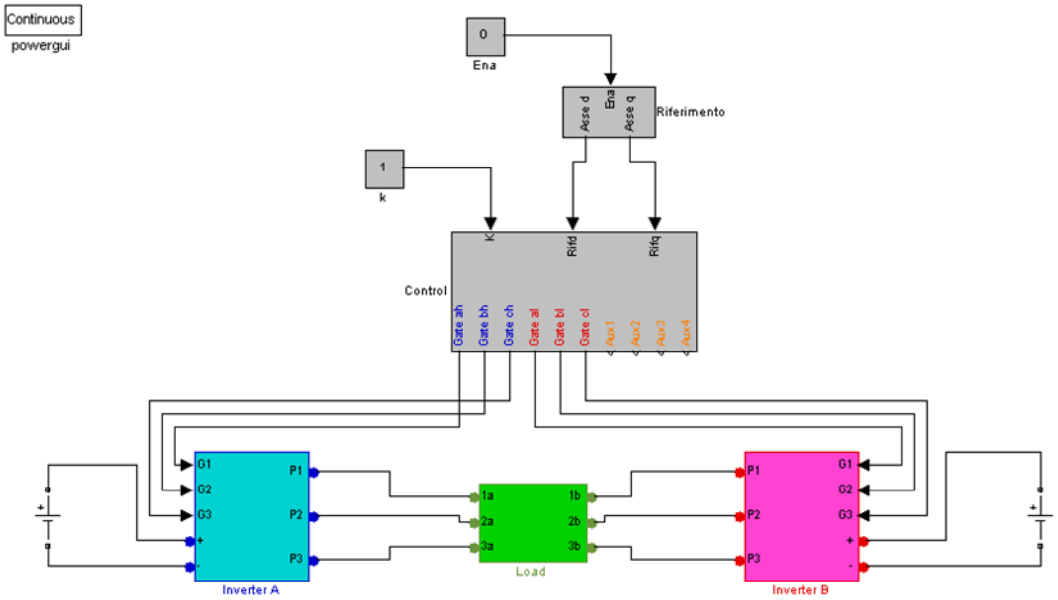


Figure 6.6: Simulink model for the dual 2-level inverter.

The two inverters are composed by several masked subsystems. The smallest block in this chain represents a single switch, composed by an ideal switch and its anti-parallel diode. Both these components have parasitic snubber capacitances and resistances which can not be zeroed without creating problems to the solver. Anyway, the components are well suited for a behavioural analysis of the system.

The S-Function contained in the model acquires the references and the power sharing ratio, elaborates all these inputs and generates the six gating signals and four auxiliary signals useful for debugging. The S-Function block is masked and it requires a single parameter which is the cycle time length.

6.2.4. Algorithm analysis

The S-Function is the core of the control made over the dual 2-level inverter. The choice to employ S-Function instead a tradition block based control came from the necessity to simulate something closest as possible to a digital control system based on a DSP platform. Moreover, the code written for the S-Function has been exported to the DSP without difficulties because both C/C++ and M code are high level programming languages quite close themselves.

Obviously, the functions written for simulations can exploit more resources than the ones implemented on DSP. Anyway, the main structure of the algorithms implemented on Simulink and on the DSP are the same.

Concerning the usage of S-Functions some information can be found in Matlab help, but they refer to the Level-1 M-File S-Functions or to C written S-Functions. In this case, Level-2 M-File S-Function has been used. It is something in between the two S-Function kinds cited above. To have an idea about how this block works it is necessary read the two pages help concerning it after having understood how C written S-Function works.

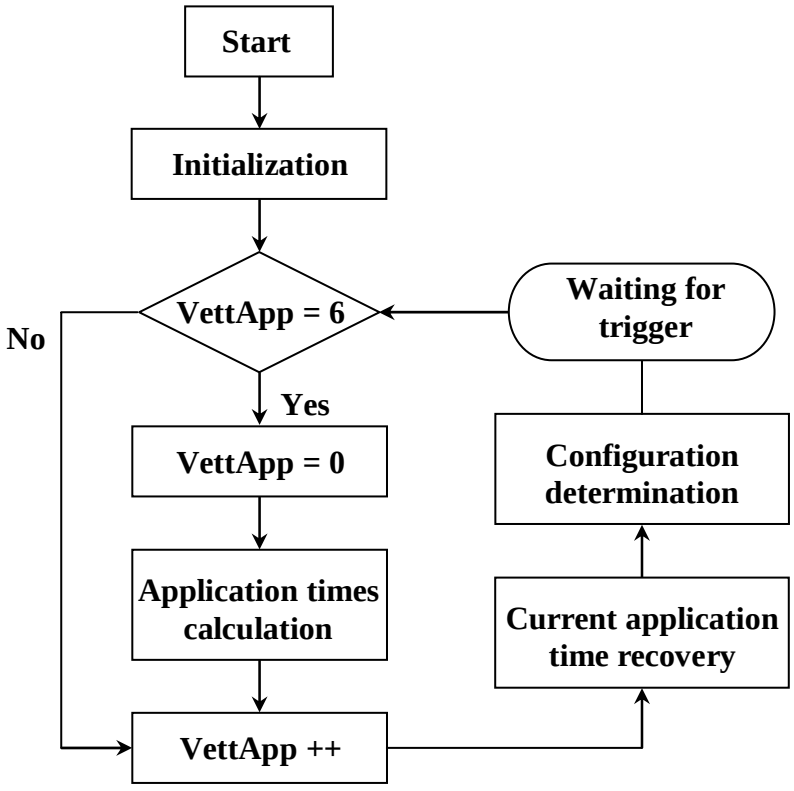


Figure 6.7: Algorithm implemented to control the dual 2-level inverter.

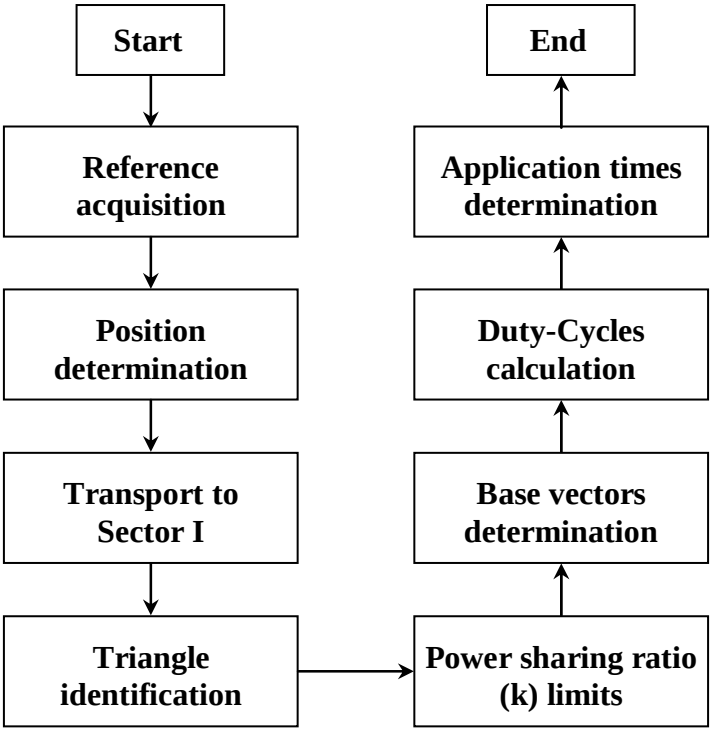


Figure 6.8: Flow diagram of the algorithm for the determination of application times.

After having configured S-Function with a proper number of inputs, outputs and states, the main code for the control of the system is contained in the callback function **update**. The flux diagram of the code implemented is shown in Figure 6.7.

After the initialization of S-Function block which is automatically called by Simulink, there is a choice based on the value of the variable VettApp which represent the number of the configuration applied in the previous application time. When this number is equal to 6 it means that the switching table is completed and it is time to calculate the duty-cycles and determine the switching sequence again. Two specifications are now necessary: *i*) during initialization the variable VettApp is set to 6; *ii*) in this case are used the basic switching table composed by six steps, without considering the problem coming from the dead times.

Then, when VettApp is equal to 6 the inner part of the code is executed and VettApp is set to 0. All the routines for the calculation of application times are executed. Figure 6.8 shows the flow diagram concerning the algorithm for the determination of application times.

As first operation, the reference is acquired as real and imaginary parts. Then the function **pos** determines the position of the reference. It has one complex argument which is the reference itself normalized in the respect of the battery voltage. Function **pos** calls the function **which_ex** twice to determine the first and the second number accordingly with the position algorithm presented in the previous Section. This position is necessary to determine the proper vectors to be applied in order to synthesize the desired output.

Knowing the Sector to which the total reference belong is important to transport the reference in Sector I subtracting from its argument the right multiple of 60°. Due to the symmetry the Sectors have among them, the calculation of duty-cycles can be always done using a virtual reference belonging to Sector I minimizing, in this way, the number of cases which must to be taken into account.

Hence, only four cases have to be considered, one for each triangle composing Sector I. To determine the right triangle, the function pos is called passing the virtual reference to it. The new position is used to determine the triangle using a nested switch-case structure.

At this point, the limits of power sharing ratio k and the vectors $\overline{v}_A$, $\overline{v}_B$ and $\overline{v}_C$ can be determined. In the case the demanded power sharing ratio is outside the boundaries, it is set to the nearest allowed value.

Knowing all the vectors and the virtual reference it is possible to determine the duty-cycles of the whole converter, inverter A and inverter B. Using these duty-cycles, the application times are easily determined solving the equations system shown in the pervious Chapter. Finally, a configurations table is built containing all the configuration the inverter has to assume for the next cycle. This conclude the inner part of the code.

Coming back to Figure 6.7, after the execution of the inner code, the variable VettApp is incremented by 1 and the current application time and configurations are extracted from tables to set S-Function outputs and time of next time call.

At this point, the algorithm waits until Simulink clock is equal to the time stored in the variable related to next call and the loop starts again.

6.3. Simulation results

6.3.1. Effectiveness of the control

The first thing the simulation has to prove is the effectiveness of the proposed control algorithm. With this purpose, the first simulation has been conducted with a voltage reference equal to 1 (modulation index 0.866), to have a general case. The power sharing ratio is put at 0.5, so both

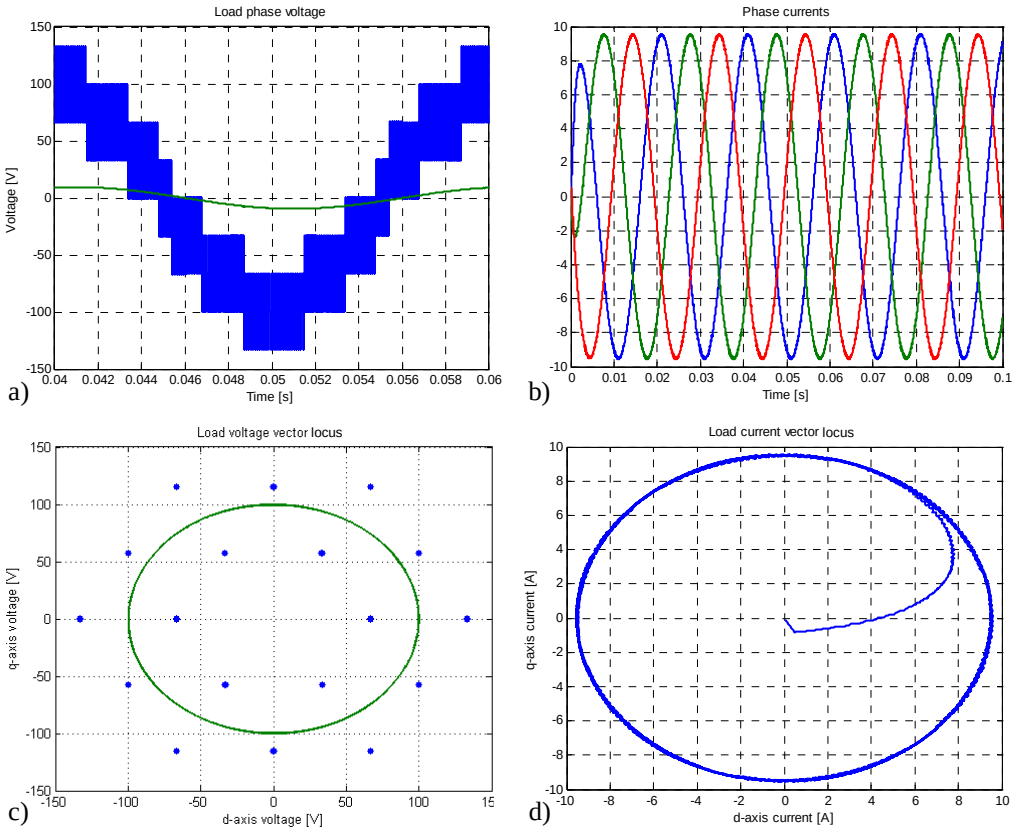


Figure 6.9: Load phase voltage and currents with a reference equal to 1 and k equal to 0.5. a) Load voltage (blue line) and current (green line) in phase 1; b) All the three load phase currents; c) Load voltage vector locus (blue dots) and reference (green line); d) load current vector locus.

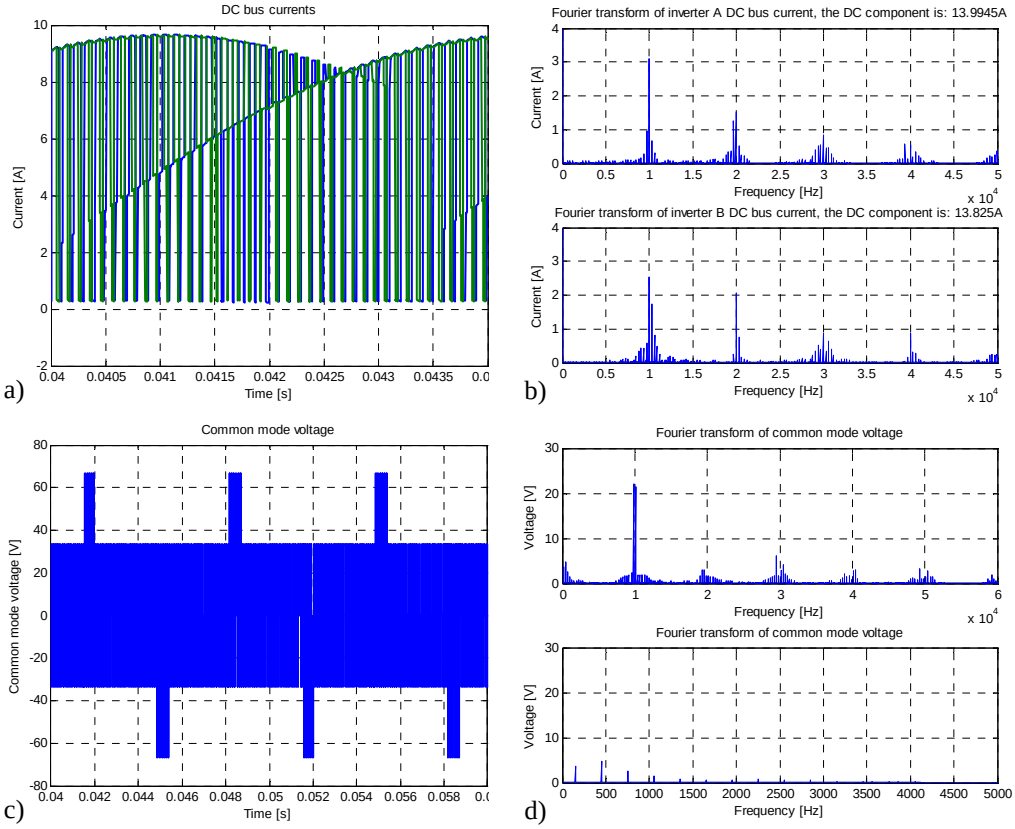


Figure 6.10: DC bus currents and common mode voltage with a reference equal to 1 and k equal to 0.5. a) Waveforms of DC bus currents on inverter A (blue line) and inverter B (green line); b) DC bus currents spectra; c) Common mode voltage between DC buses negative poles; d) High frequency and low frequency spectrum of common mode voltage.

inverters work in the same way.

Figure 6.9a) depicts the voltage and current on one load phase. All the nine voltage levels are used in the synthesis of the output. Moreover, Figure 6.9b) clearly shows that the three load currents are sinusoidal and displaced of 120° as expected by a balanced load. Obviously, the inductive load establishes a transient which lasts in less than a half fundamental period.

Figure 6.9c) depicts the load voltage vector locus. The blue dots represent the instantaneous voltage over the load, whereas the green line is the reference for which the converter is demanded. As expected, the null vector is never used to synthesize a reference always laying in the outer part of the hexagon. Similarly, Figure 6.9d) shows the locus of the load currents vector, which is quite near a perfect circle.

Figure 6.10a) shows the waveforms of DC bus currents whose spectra are represented in Figure 6.10b). Because the modulation is not symmetric, there are some differences between the spectrum of inverter A current (upper one) and the one of inverter B current (lower one). Anyway, for both of them the first important harmonic is at 10 kHz corresponding to switching frequency. Figure 6.10c) shows the waveform of the common mode voltage, that is the voltage between the negative poles of the two DC busses. As it is possible to see in Figure 6.10d), this quantity does not have low frequency harmonics.

Changing the power sharing ratio k changes the load voltage waveform because the redundant configurations can be managed in a different way and applied for different times, but its mean value is not affected. Figure 6.11a) shows the load voltage waveform when the power sharing ratio is equal to 0 and the reference is 1: the voltage level applied are still unchanged. Moreover, Figure 6.11b) depicts the currents waveforms. They are the same as the previous case being the low frequency components of the applied voltage over the respective phase.

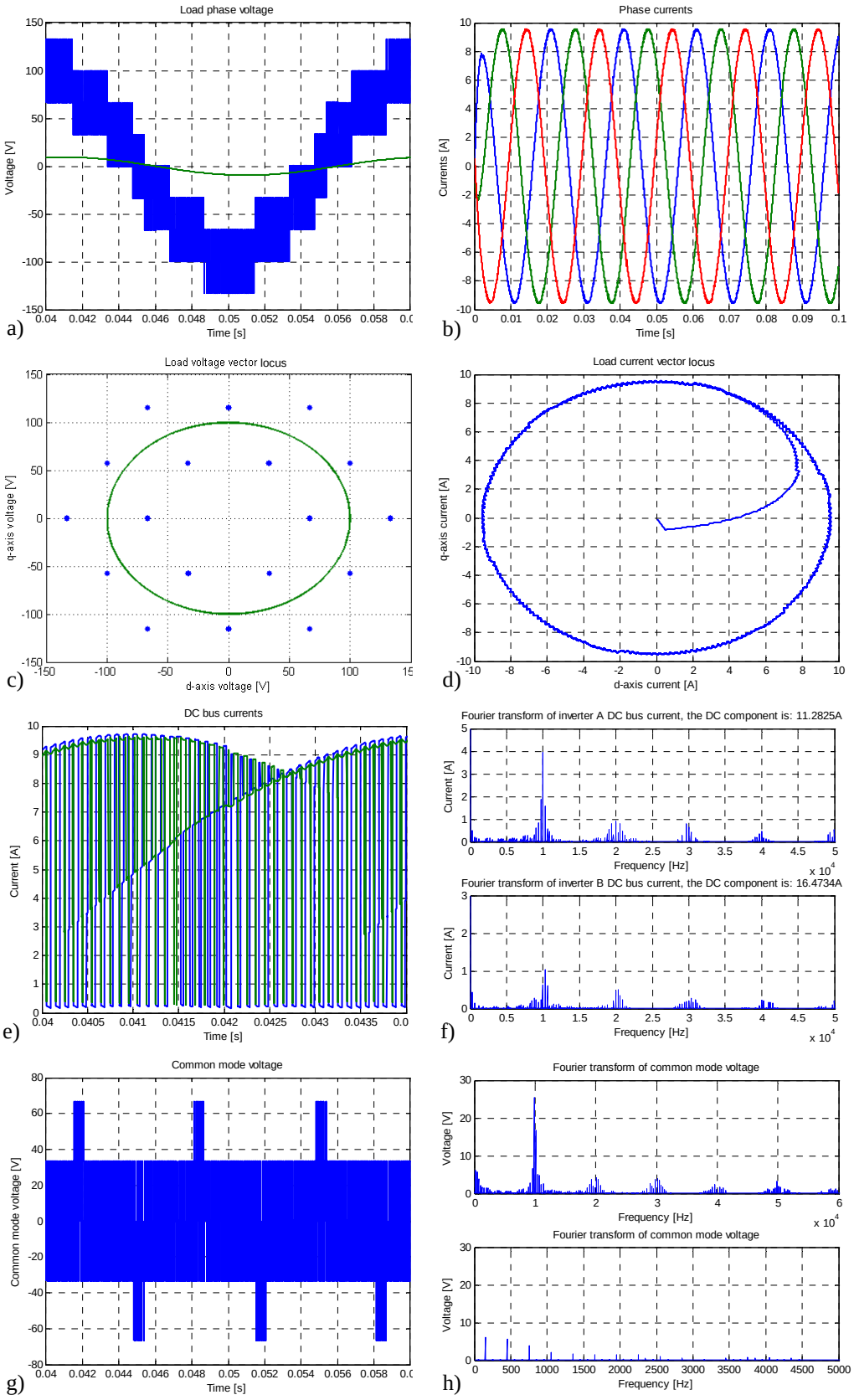


Figure 6.11: Reference equal to 1 and power sharing ratio equal to 0. a) Load voltage (blue line) and current (green line) in phase 1; b) All the three load phase currents; c) Load voltage vector locus (blue dots) and reference (green line); d) load current vector locus; e) Waveforms of DC bus currents on inverter A (blue line) and inverter B (green line); f) DC bus currents spectra; g) Common mode voltage between DC buses negative poles; h) High frequency and low frequency spectrum of common mode voltage.

Figure 6.11c) shows the load voltage locus which is composed only by the outer vectors. In

Figure 6.11d) current vector locus is drawn; it is quite a perfect circle even in this case.

An essential change happens on DC side quantities. Figure 6.11e) shows the DC bus currents on inverter A and inverter B. It is possible to see that they are slightly different. Their spectra, shown in Figure 6.11f), better highlight this difference: inverter B has a zero frequency component a bit greater than inverter A. With a power sharing ratio equal to 0 inverter A is expected to deliver no power, but the power can not be supplied by a single inverter because the modulation index is greater than 0.5, so, cycle after cycle, the nearest allowed value for this parameter is used. In this way even inverter A delivers power and its DC current is different from zero. Figure 6.11g) shows the common mode voltage whose spectra are represented in Figure 6.11h).

To conclude, a case in which a single inverter can supply all the requested power is examined. A reference equal to 0.5 (modulation index 0.433) allows to have a power sharing coefficient equal to 0 for any reference argument. Figure 6.12a) shows load voltage and current waveforms of single load phase. In this case, the voltage waveform has five levels only instead of nine. Figure 6.12b) depicts the load phase currents which have half the amplitude than the previous case, as expected. Anyway, they are quite close to sinusoidal waveforms. Figure 6.12c) shows the load voltage vector locus: only inner vectors are used to synthesize the desired output: this agrees with theory because the reference crosses only the inner zone of the hexagon. Figure 6.12d) shows the load current vector locus. The ripple is more relevant now because the average current amplitude is smaller.

Regarding DC bus quantities, some changes happened clearly shown by Figure 6.13. In particular Figure 6.13a) shows DC bus currents. Inverter B current has the standard waveform expected in SVM, whereas inverter A current is almost zero because the power sharing coefficient equal to 0 imposes to deliver no power. Figure 6.13b) shows the current spectra; as expected inverter A DC current spectrum is zero everywhere, but a small DC component. On the other hands, inverter B current spectrum has DC and 10kHz harmonics. Common mode voltage, shown in

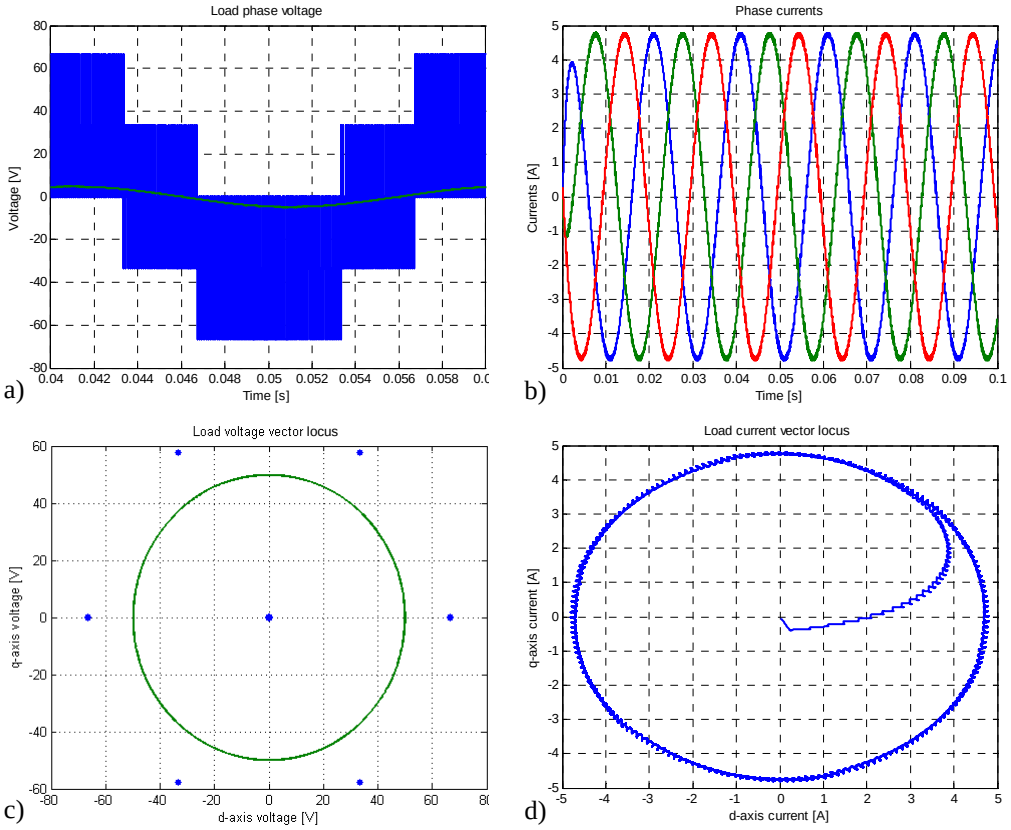


Figure 6.12: Load phase voltage and currents with a reference equal to 0.5 and k equal to 0. a) Load voltage (blue line) and current (green line) in phase 1; b) All the three load phase currents; c) Load voltage vector locus (blue dots) and reference (green line); d) load current vector locus.

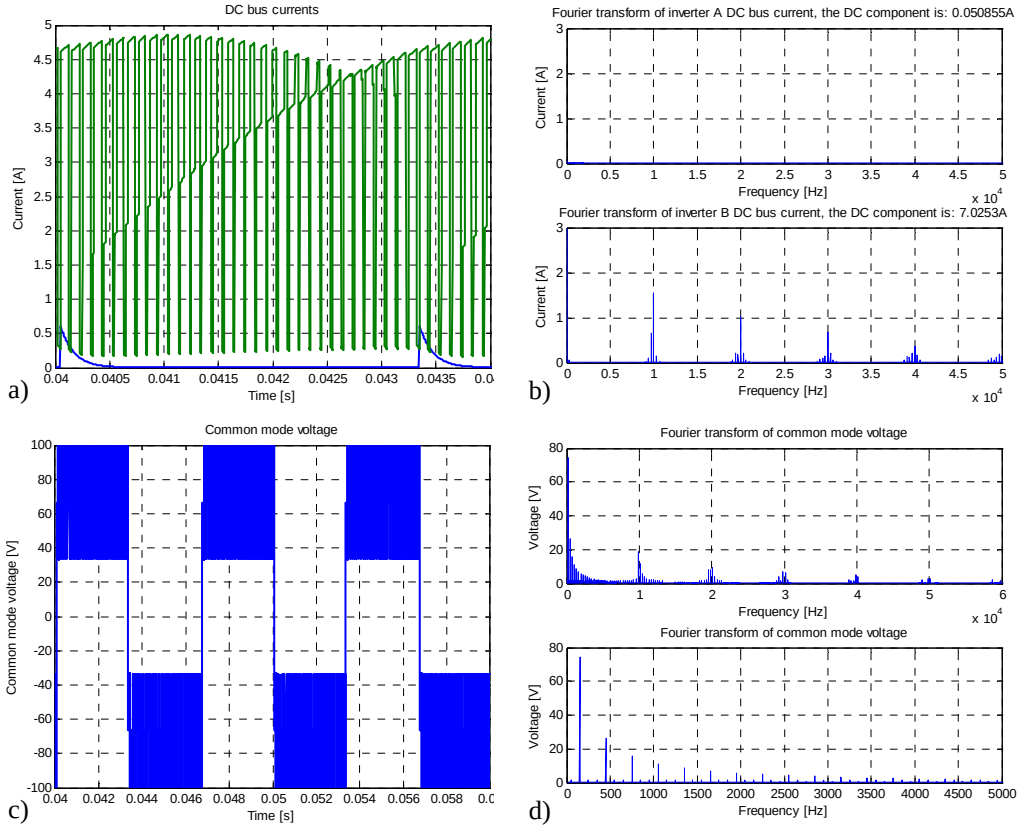


Figure 6.13: DC bus currents and common mode voltage with a reference equal to 0.5 and k equal to 0. a) Waveforms of DC bus currents on inverter A (blue line) and inverter B (green line); b) DC bus currents spectra; c) Common mode voltage between DC buses negative poles; d) High frequency and low frequency spectrum of common mode voltage.

Figure 6.13c), has a waveform essentially different with respect to previous cases. This is due to the change on the reference amplitude. As Figure 6.13d) shows, low frequencies harmonics are clearly present in its spectrum.

6.3.2. Power sharing effectiveness

In the last Section, the effectiveness of the control algorithm was proved. Three main situations were analysed showing that the control can successfully synthesize the desired output voltage with different values of power sharing coefficient.

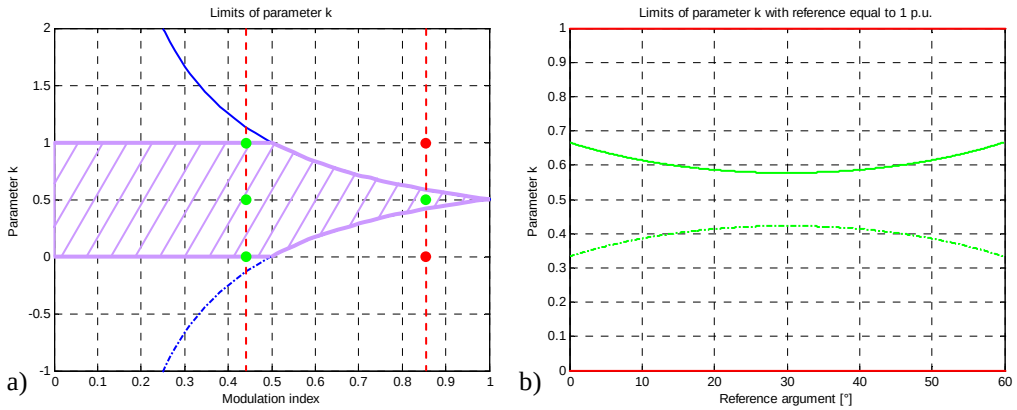


Figure 6.14: References and power sharing coefficients imposed in the simulations. a) Specifications asked to the converter; b) Actions undertaken by the control.

Nevertheless the proposed algorithm must correctly share the power between the two inverters, besides the synthesis of the desired output voltage. Figure 6.14 is useful to better understand what is demanded to the converter and how the control manages situations not allowed. Figure 6.14a) shows the limits of the power sharing coefficient in the respect of the modulation index. The dots represent the specifications for which the converter is demanded. The four green dots do not create any problem. Concerning the red dots, they are outside the allowed region, as can be seen in the picture. The converter can not deliver power keeping unchanged the power sharing coefficient for all the values of the reference argument, so it undertakes the action shown in Figure 6.14b): it uses the nearest allowed value cycle after cycle. This means that the green solid line is followed when the power sharing coefficient is 1 and the green dash-dotted line is followed when the power sharing coefficient is 0.

All the pictures in Figure 6.15 shows the power absorbed by the two inverters. In particular the blue line and the green line refer to inverter A and inverter B respectively. Figure 6.15a), c) and e)

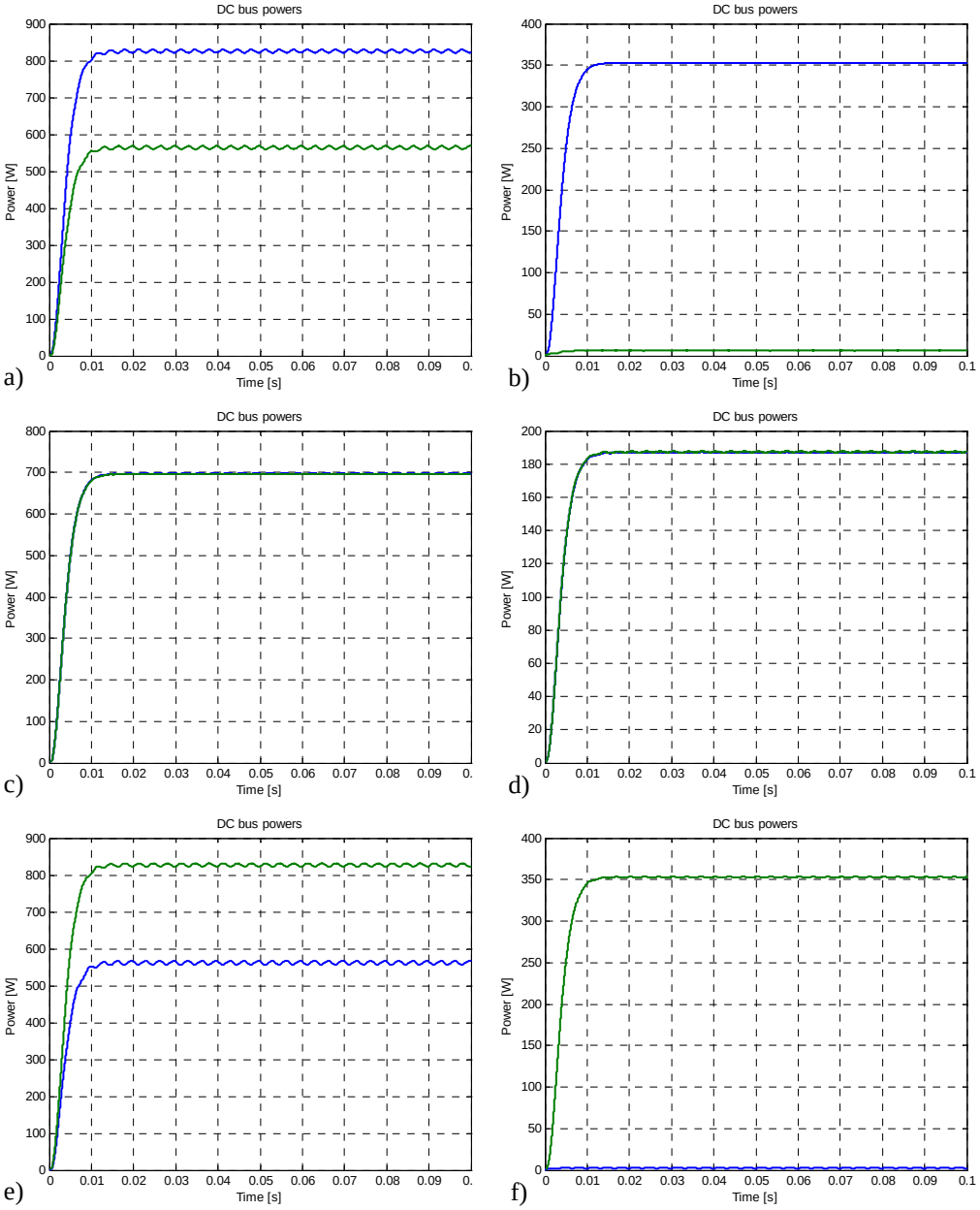


Figure 6.15: DC bus powers of inverter A (blue line) and inverter B (green line). a) Reference 1, power sharing coefficient 1; b) Reference 0.5, power sharing coefficient 1; c) Reference 1, power sharing coefficient 0.5; b) Reference 0.5, power sharing coefficient 0.5; a) Reference 1, power sharing coefficient 0; b) Reference 0.5, power sharing coefficient 0.

have been made with the same reference equal to 1 (modulation index 0.866), whereas Figure 6.15b), d) and f) have been made with a reference equal to 0.5 (modulation index 0.433). Figure 6.15a) and b) have been made with the same power sharing coefficient equal to 1; Figure 6.15c) and d) have been made with a power sharing coefficient equal to 0.5; Figure 6.15e) and f) have been made with a power sharing coefficient equal to 0.

Figure 6.15c) and d) clearly show that the powers absorbed by the two inverters are equal in both cases, as imposed by the power sharing coefficient equal to 0.5. The dependency on the reference value is evident in the other pictures. The power of inverter B is expected to be more or less zero in Figure 6.15a) and b), because the power sharing coefficient is equal to 1. This happens when the reference equal to 0.5, as Figure 6.15b) shows. When the reference is equal to 1, the control algorithm made inverter B absorb as few power as possible following the maximum limit of power sharing coefficient for the given reference. This is reflected on Figure 6.15a). A similar situation is described by Figure 6.15e) and f), but the two inverters change roles.

6.3.3. Performance

To conclude the simulation overview, the load power quality is analysed in this Section. Table 6.1 reports RMS and THD of load phase voltage and current similarly to what was done for other simulation results in Chapter 4.

		Voltage		Current	
Ref.	k	RMS	THD	RMS	THD
1	1	74.8663 V	0.35413	6.7328 A	0.0051494
	0.5	74.8669 V	0.35389	6.7334 A	0.0044338
	0	74.8644 V	0.35396	6.7331 A	0.0067871
0.5	1	42.8458 V	0.68347	3.3748 A	0.0092786
	0.5	42.8345 V	0.68794	3.3669 A	0.0081883
	0	42.8143 V	0.69228	3.3585 A	0.010222

Table 6.1: Load power quality. Voltage RMS and THD, current RMS and THD.

The data shown in Table 6.1 were caught in the same conditions as the powers shown above: power sharing coefficient equal to 1, 0.5 and 0 for two different references values (1 and 0.5).

Comparing these results with the ones obtained using analogue modulations it can be seen that they are quite close. In particular voltage THDs are comparable with the best results given by analogue controllers. Unfortunately, current THDs are slightly worse because current spectra have numerous harmonics even at low frequencies.

Chapter 7

Set-up implementation

7.1. Introduction

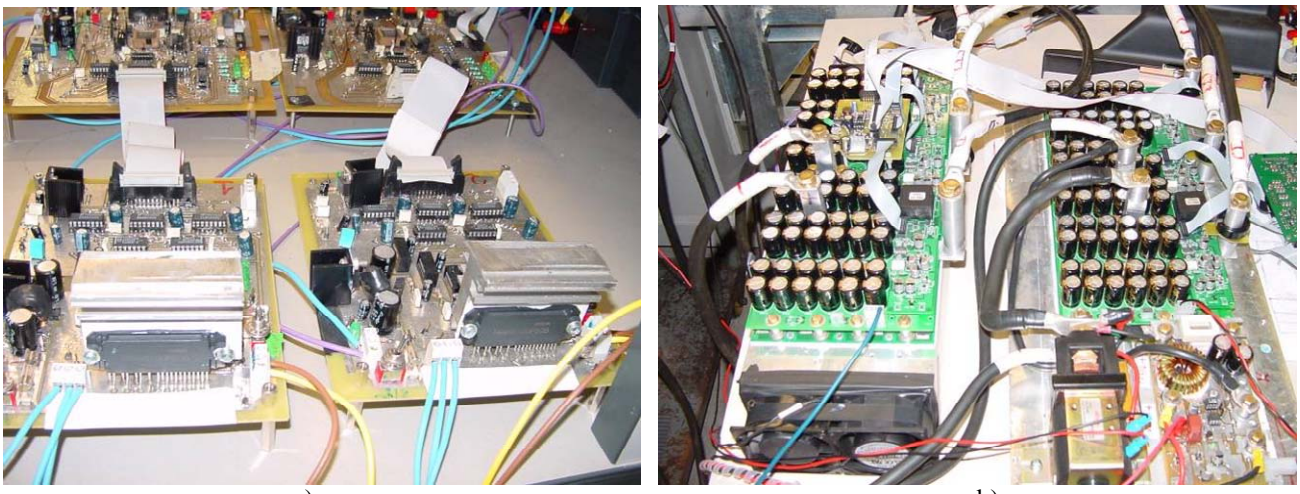
7.1.1. System overview

Two dual 2-level inverter systems have been implemented, rated for different powers. Figure 7.1a) shows reduced scale converter, whereas Figure 7.1b) depicts the full scale converter.

The full scale converter is rated 180 V DC bus voltage and 220 A RMS output current. The two inverters are built using discrete components: all twelve switches are realized by several power MOSFETs in parallel connection.

The reduced scale converter is the first prototype made and it is the only structure to which the following description is referred. This converter has been implemented using two integrated 3-phase 2-level inverters manufactured by International Rectifier. These power modules are rated for 450 V over the DC bus and 10 A as maximum phase current output RMS value: the voltage limits is largely greater than the 48 V effectively applied by battery banks.

Figure 7.2 shows the seven boards compose the system: TMS320C2812 evaluation board, one



a) b)

Figure 7.1: Dual two level inverter implementations. a) Reduced scale converter; b) Full scale converter.

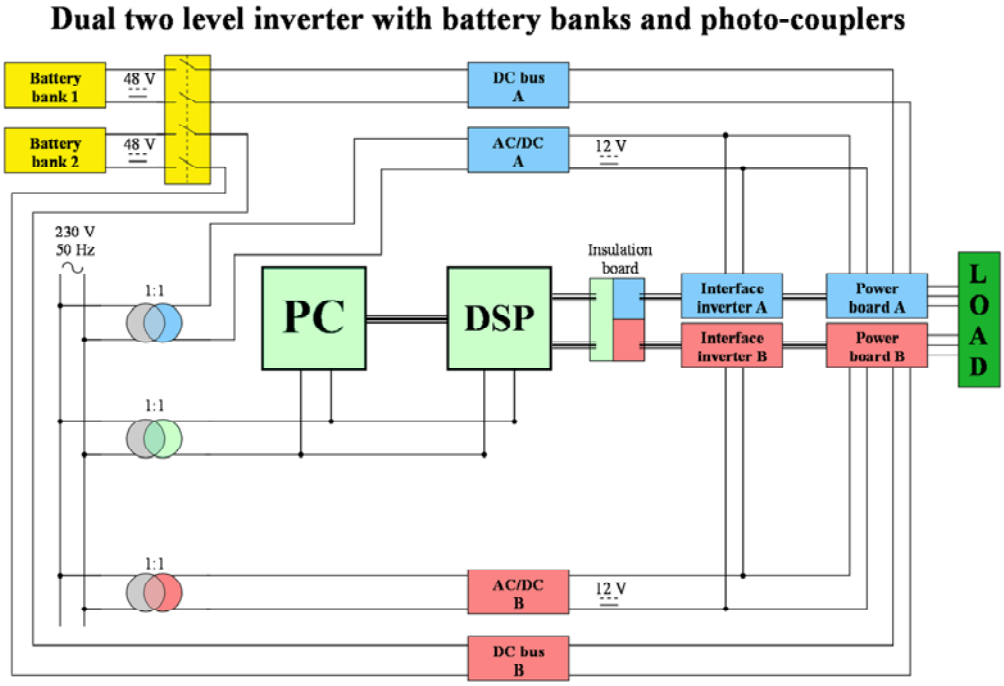


Figure 7.2: Scheme of dual 2-level inverter which was implemented.

custom made expansion board for DSP, one insulation board, two interface boards and two power boards. Two battery banks, some protection switches and three insulation transformers complete the hardware.

Considering Figure 7.2, the yellow background indicates battery banks and the switch to quickly disconnect them from the converter in case of fault. Light green background indicates PC, DSP boards and all the stuff related to the control part of the system. Light blue and pink backgrounds indicate boards and supplies related to inverter A and inverter B respectively. Finally, the block representing 3-phase load is filled in dark green.

In this Chapter all the parts composing the dual 2-level inverter will be deeply described and analysed. Now it is necessary to underline the importance of electrical insulation among inverter A, inverter B and control boards, also highlighted by the different colours used for their background. A fault in the insulation may critically invalidate the right operation of the converter.

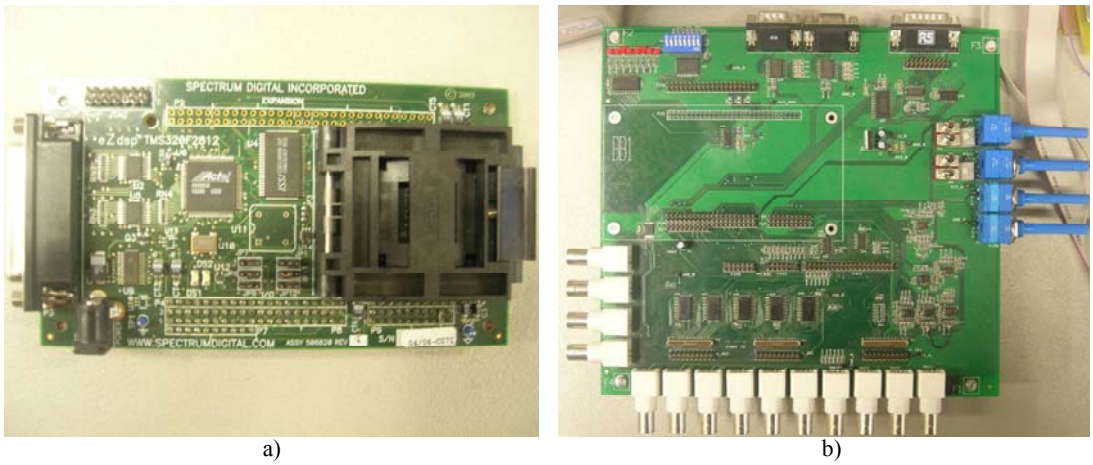
Moreover, the code written for the DSP will be commented in the last section of this Chapter with the aim to give the essential knowledge to understand it, if it is necessary.

7.2. Hardware

7.2.1. Digital signal processor and control hardware

The core of the control is implemented on a TMS320F2812 DSP manufactured by Texas Instrument. The control circuitry connecting DSP to the two inverters is composed by three boards: the commercial evaluation board for TMS320F2812 manufactured by Spectrum Digital (F2812ezDSP), one custom made expansion board to implement DAC and filters, one board made to redistribute and insulate the gating signals.

Figure 7.3a) shows the F2812ezDSP. This board contains the DSP, the hardware which is strictly necessary to feed it properly and to connect it to Code Composer Studio environment via JTAG connection. Because some peripherals, like DAC, must be provided by an external board, the expansion board, shown in Figure 7.3b), has been designed at the Department of Electrical



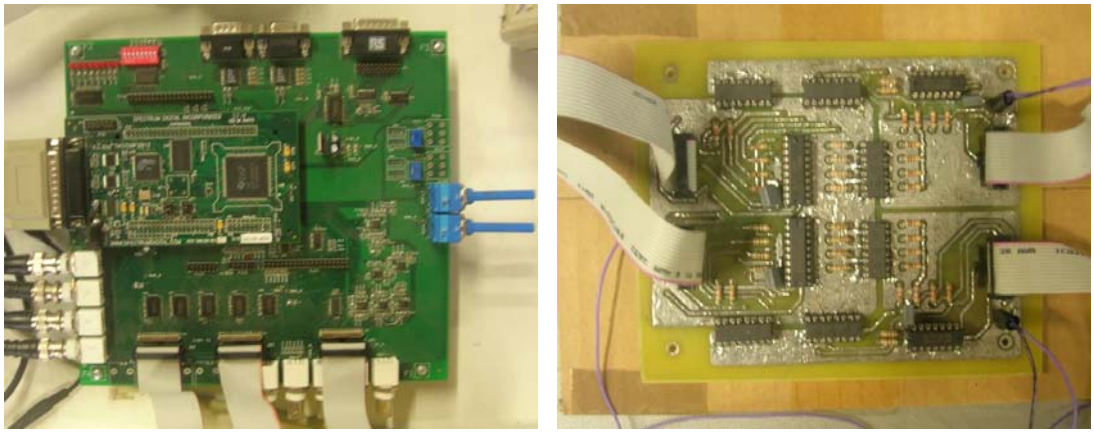
a) b)

Figure 7.3: DSP boards. a) F2812ezDSP evaluation board; b) Custom made expansion board.

Engineering. It provides four 16-bit DAC channels using a DAC8534 integrated circuit and connecting it to the DSP throughout the Xintf interface [78]. Moreover, the expansion board provides BNC connector, potentiometers, switches and all the conditioning circuitry necessary to obtain clean input signals inside the voltage bands allowed by DSP. For other purposes than multilevel converter application, the expansion board contains also eCAN [79] and RS-232 [79-80] connectors.

To allow fast communications and minimize the noises related to bit transmissions, the board-to-board connection between expansion board and evaluation was preferred to flat-cables or others. In can be noticed, in Figure 7.3b), the room necessary to fit the DSP evaluation board. Figure 7.4a) shows how the two boards appear when connected.

The insulation board is shown in Figure 7.4b). This board has been made considering two particular needs. First of all, it was necessary to redistribute the signals provided by the connectors of the expansion board. Indeed, the pins distribution in the expansion board was conceived for the design of the board itself, not for the connection with the interface boards. Moreover, the functional insulation among control, inverter A and inverter B requires fiberoptic or photo-coupler transmission. In Figure 7.4b) three ground plane are clearly distinguishable. On the left there are the connectors with the expansion board. The signals are buffered using SN74ABT244AN to properly drive the photo-couplers, which must be quite fast to follow the commutations imposed by the control system. On the right of the picture there are the ground plane related to the two inverters and the flat cables providing the connection with the interface boards.



a) b)

Figure 7.4: Control circuitry for the dual 2-level inverter. a) Evaluation and expansion boards connected; b) Insulation board.

7.2.2. Interface boards

The system is composed of two interface boards, shown in Figure 7.5. The main function for which this board was designed is to provide transform leg control signals in switch control signal and provide the necessary dead-times. Moreover some safety functionalities have been also implemented. The core of this board is Xilinx XC9572XL [82] which is the CPLD placed in the middle of the board. The program in the CPLD uses an internal state machine to produce the switch gating signals with dead-times of selectable length (0, 2, 4 and 8 μs).

Moreover, three pins of the CPLD are dedicate to fault protection, commutation enable and reset signals. The commutation enable is a signal which can be generated either by a manual switch or the DSP. When this signal is low, the CPLD forces all the gate signals to zero opening all the switches. When the enable is high, CPLD let the gating signal be applied to the inverters.

Fault protection works similarly. Several information coming from the power board enter in a multi-port NAND-gate to generate the signal driving the fault input. When one of the error occurs (its signal goes low) the fault input is driven high and the CPLD forces all the gating signals to zero.

Reset signals is used to bring CPLD to initial state after a fault. The blue button on the top of the picture is used to manually input reset signal to CPLD. After a fault, CPLD enters in an idle state and it does not receive the leg control signals coming from DSP. Pressing the reset button is necessary to bring CPLD out of idle state.

A photo-coupler is dedicated to the communication of incidental faults to the twin board. It is located on the right side (white chip), nearby the dedicated connector.

The communication with the power board exploits the connector on the bottom. All the signals are buffered using DS8922 differential transceivers to increase the robustness of the transmission against the noises produced by power switches commutation.

Several LEDs are scattered on the board. In Figure 7.5, all the LEDs are identified by a number. The green LED number 1 advices that the enable signal is not set, so the CPLD forces all the output to zero when this LED is turned on. The LEDs number 2, 3 and 4 identify the presence of external, 5 V and 3.3 V voltage supplies respectively. The 5 V supply is obtained using a LM2575 switching regulator, whereas the 3 V supply is synthesized by a LM1117 linear regulator.

On the right side, LED number 5 reveals that the precharge circuitry is active. When this LED is turned on a precharge resistor is series connected to DC bus to avoid current spikes due to the capacitors charge. The LEDs number 6 and 7 are associated to faults. The red LED reveals an

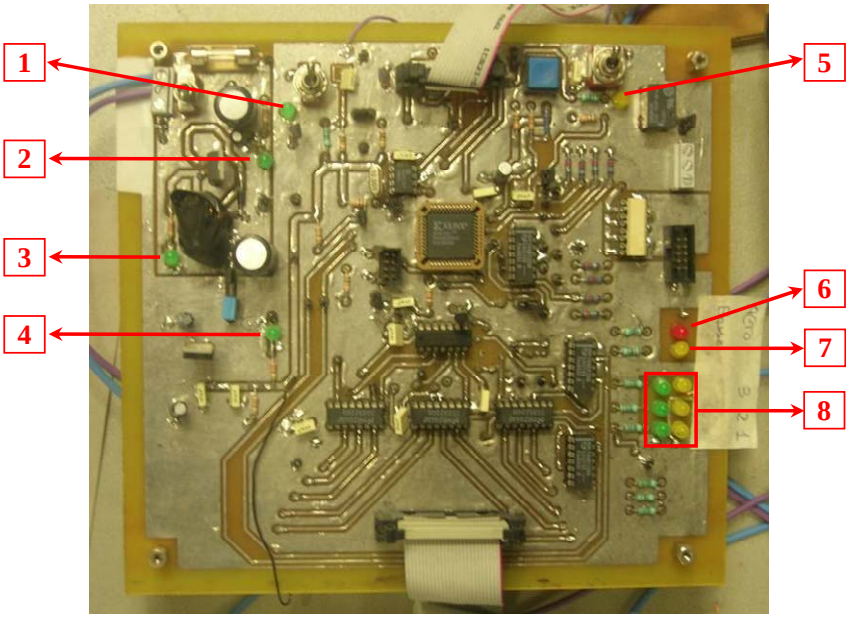


Figure 7.5: Interface board.

overcurrent fault, while the yellow LED is related to 800µ fault. Overcurrent fault happens when the current over the switches overcome the maximum allowed limit. The 800µ fault happens when the leg state does not change for more than 800µs. Unfortunately, some modulation technique presented in this book is incompatible with this protection and it is better to disable it. Finally, the six LEDS identified with number 8 are associate to the state of the six switches: when they are turned on the respective switch is conducting.

7.2.3. Power boards

The power board, shown in Figure 7.6, implements all the circuitry to drive the power. The core of this board is the IRAMS10UP60B [83] integrated inverter manufactured by International Rectifier. This chip, placed on the right side of the board under the heat-sink, is a complete 3-phase inverter able to drive 10 A RMS output current in each phase. The overcurrent fault signal is provided by the chip itself.

The typical application connection proposed by datasheet exploits the possibility of the IRAMS10UP60B to use bootstrap capacitors, but for the purposes of dual 2-level inverter three insulated sources are needed to ensure a stable configuration even at very low commutation frequency.

The insulated sources are obtained using AM2D-1215 [84] DC-DC converters manufactured by Aimtec. These converters are the three black chip in the middle of the board. As can be seen, they are quite small even if they are able to insulate up to 3 kV.

The differential transceivers for the communication with the interface are placed on the right side of the board, near the flat cable connector. Like the interface board, DS8922 are used even in power module to transmit signals with high robustness to noises.

Even in this board there are LM2575 and LM1117 DC-DC converters to stabilize 5 V and 3.3 V voltage levels. The ground plane near to the switching converter is connected to the other ground through a small jumper to maximize the impedance of the path for noises produced by the switching converter itself, preventing a pollution of the other signals through the digital ground.

Some LEDs are used to give information about the state of the converter. The green LEDs on the bottom are used to signal the presence of 5 V and 3.3 V supplies. In the upper side of the board, the two rows of green and yellow LEDs notify the gating signals, so when they are turned on the

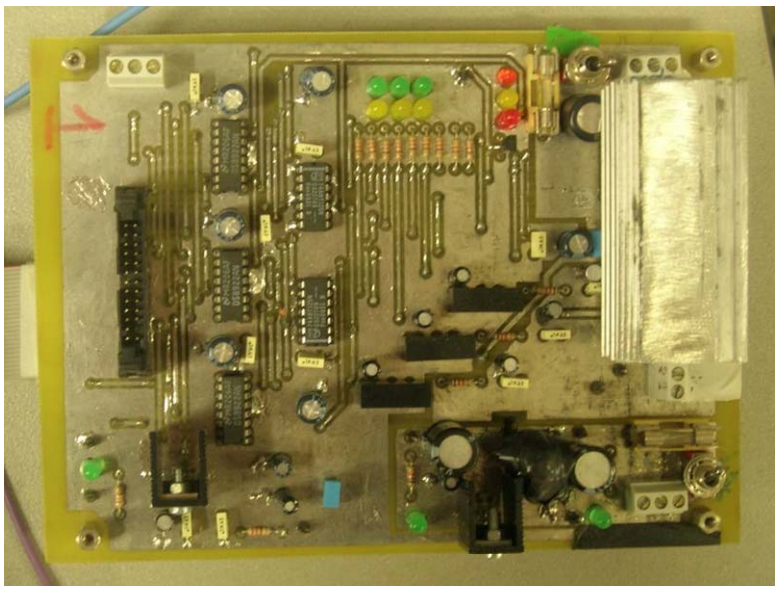


Figure 7.6: Power board.

a) b)

Figure 7.7: Dual 2-level inverter hardware. a) Resistors and inductor used as 3-phase load, b) Whole converter.

correspondent switch is conducting. The red LED is related to overcurrent fault signal coming from the inverter. The other two LEDs (orange and yellow) inform about the disconnection of the DC bus through the nearby manual switch. Indeed, this manual switch can open or close the path connecting the positive pole of DC bus to the connector of the battery bank.

7.2.4. Other hardware

To complete the system, a 3-phase load has been connected to the converter. Each branch of the load is composed by a resistor and an inductor series connected. The resistors and the 3-phase inductor used are shown in Figure 7.7a). The resistor are wound around a cylindrical ceramic support and mounted on metal frame with a rack of electric fans in the back for forced aircooling. The 3-phase inductor is wound on a metal core and the three windings allow to select among four different inductance values. For experimental set-up, 5.5 Ω and 0.120 mH have been chosen in each phase as total resistance and total inductance values.

Besides the load, even some external power sources are necessary to feed the boards. F2812ezDSP and its expansion boards are fed by the power sources provided with the DSP. Two external power sources are needed to feed interface and power boards. Indeed, an external 13.5 V insulated power supply is needed for the circuitry feeding each inverter.

To ensure the three insulated grounds required by the converter, three insulation transformers are necessarily used. They have to provide insulation between control, inverter A, inverter B grounds and the grid. If insulation transformers were not used, there would be a path for the common mode current and the system would loose multilevel converters properties.

Figure 7.7b) shows the whole system at a glance. Starting from the left side of the picture there are: F2812ezDSP mounted on the expansion board, the insulation board and the two interface boards connected to their respective power boards.

7.3. Software

7.3.1. Implemented algorithms

The implementation of reduced scale converter took time because it was the first prototype of dual 2-level converter built at the Department of Electrical Engineering. Several adjustments were

done to first design to get to an operative multilevel converter. In particular, the lack of a good insulation among control ground and inverters grounds made the first implementation trial fail.

In the meanwhile the reduced scale converter was being debugged and completed, the full scale dual 2-level converter was built achieving better performances than its forerunner. Hence, both converter were used to achieve experimental results which will be shown in the following.

Anyway, for the purpose of this dissertation, only the algorithm implemented on the reduced scale converter is described. It is a bit different to the one simulated for two reasons mainly. First of all, the DSP used is a fixed-point architecture and most of the functions used in simulation can not be implemented on it or their implementation will require a lot of resources and program memory. Moreover, the algorithm used in simulation can not be implemented using standard PWM based on the comparison between carriers and references.

A simple algorithm has been implemented to prove that the converter really works as expected. The simplest way to synthesize a given reference is to use a modulation strategy imposing six step to one inverter and modulating the remaining part with the other one. After testing this kind of control it is simple to implement the second way to obtain power sharing described in Chapter 5.

7.3.2. Position determination algorithm

The fixed-point architecture of DSP does not allow to use some mathematical functions exploited in Matlab-Simulink for the determination of the position. In particular, complex numbers are not practical in DSP code: space vectors must be treated as real and imaginary parts. Moreover, functions like arc tangent are available in IQMath library, but can result time expensive.

The algorithm for position determination implemented on the DSP exploits comparisons between the real and imaginary parts of the reference with constant values to determine where it lays.

The function **DetSect** implements the algorithm whose flow diagram is shown in Figure 7.8. This function needs three arguments: the real part and the imaginary part of the normalized reference and a flag which can be 0 or 1. When the components of a given vector are passed to it and the flag is set to 1, function **DetSect** returns the Sector to which the vector belongs considering

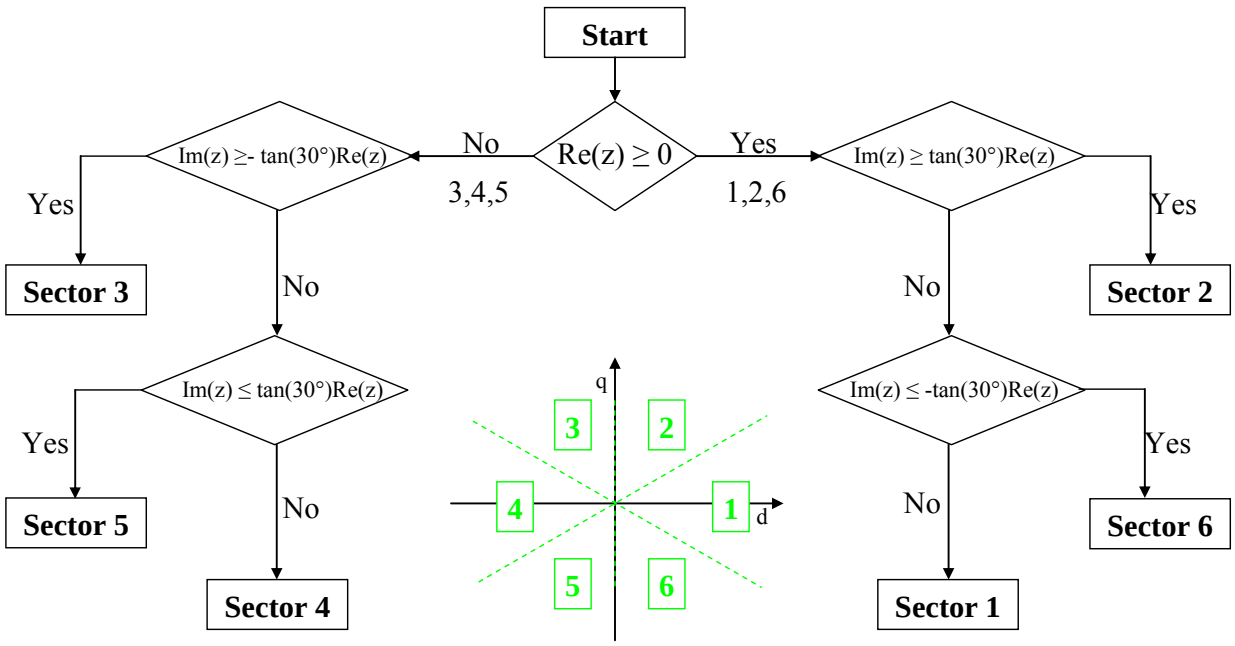


Figure 7.8: Flow diagram of DSP algorithm for position determination.

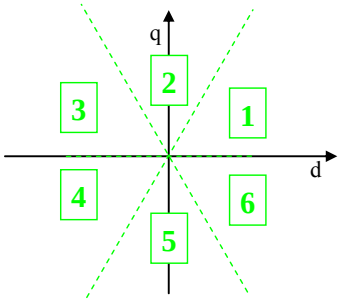


Figure 7.9: Alternative Sector map returned by DetSect.

the numbering given in the middle of Figure 7.8. In this way, the first part of the label identifying the position can be determined.

Concerning the second part of the label, a different subdivision of the d-q plane must be considered: it is shown in Figure 7.9. **DetSect** can be used again, but some tricks must be used. Instead of passing to it real and imaginary parts of the vector whose position has to be determined it is necessary to follow the following procedure: the imaginary part must be passed as first parameter, the opposite of the real part must be passed as second parameter and the flag must be set to 0.

To achieve the label defining reference position two steps are required. The reference is passed to DetSect with flag equal to 1. The first part of the label is returned and it can be used to determine the vector bisecting the identified Sector. The difference between the reference and the so determined vector must be passed to DetSect following the proper procedure describe above. In this way, the label identifying the position of the voltage reference is obtained.

7.3.3. Implemented switching tables

Even the switching tables are different than those presented in Chapter 5. Mainly because the applied vector are ordered to minimize the number of commutations of each leg during a cycle. Figure 7.10 shows the convention used to identify voltage vectors in the following switching tables. The two diagram on the left concern inverter A (blue) and inverter B (red) generated vectors. Together to the usual voltage vectors $\bar{e}_\alpha$, $\bar{e}_\beta$ and $\bar{e}_\gamma$, two new vectors are introduced: $\bar{e}_{\delta 1}$ and $\bar{e}_{\delta 2}$.

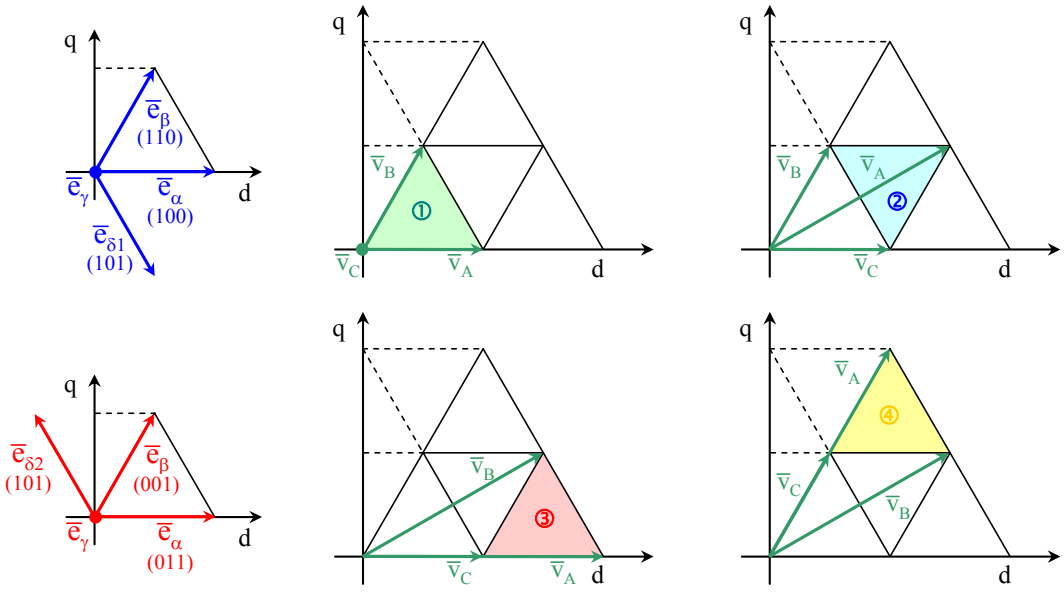


Figure 7.10: Conventions used to identify voltage vectors in implemented switching tables considering both inverters and whole converter points of view.

The other four diagrams concern whole converter output voltages in each of the four Regions taken into account.

Keeping in mind the convention just described, Table 7.1 shows the implemented switching tables for Region ① with reference to the particular Sector highlighted in Figure 7.10.

$\bar{v}$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\gamma$					$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$
s_{1A}	0	0	0	0	0	0	1	1	1	0
s_{2A}	0	0	0	0	0	0	0	1	0	0
s_{3A}	0	0	0	0	0	0	0	0	0	0
s_{1B}	1	0	0	0	1	1	1	1	1	1
s_{2B}	1	1	0	1	1	1	1	1	1	1
s_{3B}	1	1	1	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\gamma$				

Table 7.1: Implemented switching table for Region ①.

Table 7.2 is related to, Region ②. It can be noticed that in this case there are no double commutation at all This means that dead-times do not produce the annoying effects described in Chapter 5.

$\bar{v}$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_A$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\alpha$					$\bar{e}_\alpha$	$\bar{e}_{\delta 1}$	$\bar{e}_\gamma$	$\bar{e}_{\delta 1}$	$\bar{e}_\alpha$
s_{1A}	1	1	1	1	1	1	1	1	1	1
s_{2A}	0	0	0	0	0	0	0	1	0	0
s_{3A}	0	0	0	0	0	0	1	1	1	0
s_{1B}	0	1	1	1	0	0	0	0	0	0
s_{2B}	0	0	1	0	0	0	0	0	0	0
s_{3B}	1	1	1	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\beta$	$\bar{e}_{\delta 2}$	$\bar{e}_\gamma$	$\bar{e}_{\delta 2}$	$\bar{e}_\beta$	$\bar{e}_\beta$				

Table 7.2: Implemented switching table for Region ②.

Table 7.3 and Table 7.4 are related to Region ③ and Region ④ respectively.

$\bar{v}$		$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\alpha$					$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$
s_{1A}	1	1	1	1	1	1	1	1	1	1
s_{2A}	0	0	0	0	0	0	1	1	1	0
s_{3A}	0	0	0	0	0	0	0	1	0	0
s_{1B}	0	0	0	0	0	0	0	0	0	0
s_{2B}	1	0	0	0	1	1	1	1	1	1
s_{3B}	1	1	0	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\gamma$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\alpha$				

Table 7.3: Implemented switching table for Region ③.

$\bar{v}$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_B$	$\bar{v}_A$
$\bar{e}_A$	$\bar{e}_\beta$					$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\beta$
s_{1A}	1	1	1	1	1	1	1	0	1	1
s_{2A}	1	1	1	1	1	1	0	0	0	1
s_{3A}	0	0	0	0	0	0	0	0	0	0
s_{1B}	0	0	1	0	0	0	0	0	0	0
s_{2B}	0	1	1	1	0	0	0	0	0	0
s_{3B}	1	1	1	1	1	1	1	1	1	1
$\bar{e}_B$	$\bar{e}_\beta$	$\bar{e}_\alpha$	$\bar{e}_\gamma$	$\bar{e}_\alpha$	$\bar{e}_\beta$	$\bar{e}_\beta$				

Table 7.4: Implemented switching table for Region ④.

All the tables are made to highlight the two parts composing the cycle: in the first part inverter A is in fixed configuration and inverter B is modulating, whereas in the second part the roles are exchanged.

7.3.4. Compiling process overview

After the explanation of the main changes made in implementation code in the respect of the simulation, the description of the algorithm can be expounded more clearly. Figure 7.11 shows how the programming process works. The software used is **Code Composer Studio** (**CCS**), the environment provided by Texas Instrument to program the whole C2000 DSP family. This environment allows the user to write all the necessary code and to organize it in several files grouped together by an entity called project.

The programming languages supported by CCS are mainly ANSI C/C++ and Assembly. Due to the complexity of the architecture of newest DSP, using C/C++ rather than Assembly is highly

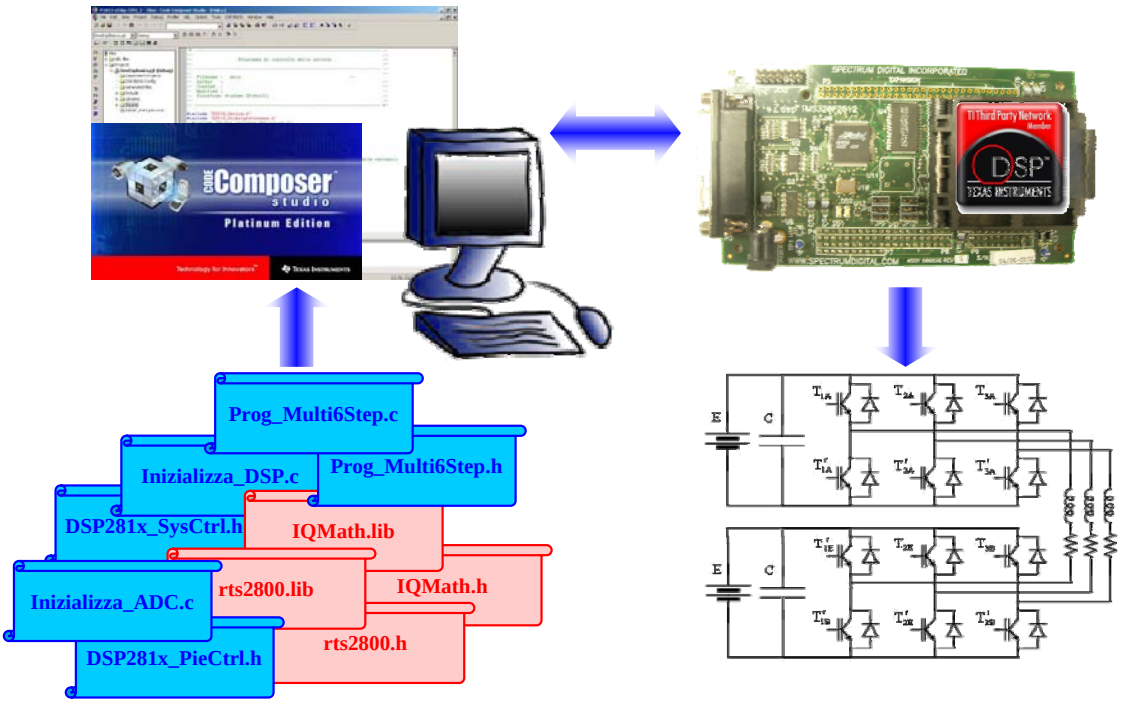


Figure 7.11: Code implementation using Code Composer Studio.

suggested. Moreover CCS environment is able to control code execution on-line; this is useful in debugging contest. For further information on CCS environment, Texas Instruments offers specific literature [85].

Figure 7.11 can be read clockwise, starting from the bottom-left corner. Blue parchments represents files specifically made for the dual 2-level control, whereas red parchments represent code provided by Texas Instruments. The user-made code has been split in several source (.c) files dependently on the tasks executed. For instance, all the code used to initialize the DSP is written in the file **Inizializza_DSP.c**, whereas all the code necessary to initialize the **Analog-to-Digital Converter** (**ADC**) is written in file **Inizializza_ADC.c**. The file containing all the code necessary to implement the control algorithm and the main function of C code is **Prog_Multi6Step.c**. Other files are included in the project, each one implementing its own logical function. Moreover, two libraries provided by Texas Instruments are used: **IQMath.lib** and **rts2800.lib**. These two files contain pre-compiled code for the execution of mathematical functions and some instructions on how manage the DSP internal memory to accept compiled code. In order to call the functions stored in these files the respective header files are needed.

CCS manages all the files within a project, building and linking them under the directives included in the linker file (**.cmd**). The compiling process ends when the object (**.obj**) file is made. This file contains the bit-code necessary to make the DSP operate as desired by the user.

Using the JTAG connection, the bit-code is transferred to DSP and the emulation RAM is written. Now the DSP can be powered on and the code can be executed and debugged under CCS control. In debugging contest, CCS results to be very effective offering to the user several tools to find bugs, infinite loops and so on. Moreover, being under CCS control, the DSP can be held at any time in case of fault preventing the system to be seriously damaged.

7.3.5. Code analysis

Accordingly to Figure 7.12, the code implemented on DSP can be subdivided into two main parts: **initialization** and **loop**.

Initialization contains all the function used to initialize the system. These functions are called only once during program execution. In particular all the DSP peripherals necessary are set and two tables are written. The first table, called **mvVector**, contains all the data related to the voltage vectors generable by dual 2-level inverter. The second table, called **mtTable**, contains all the switching patterns necessary to obtain proper commutations.

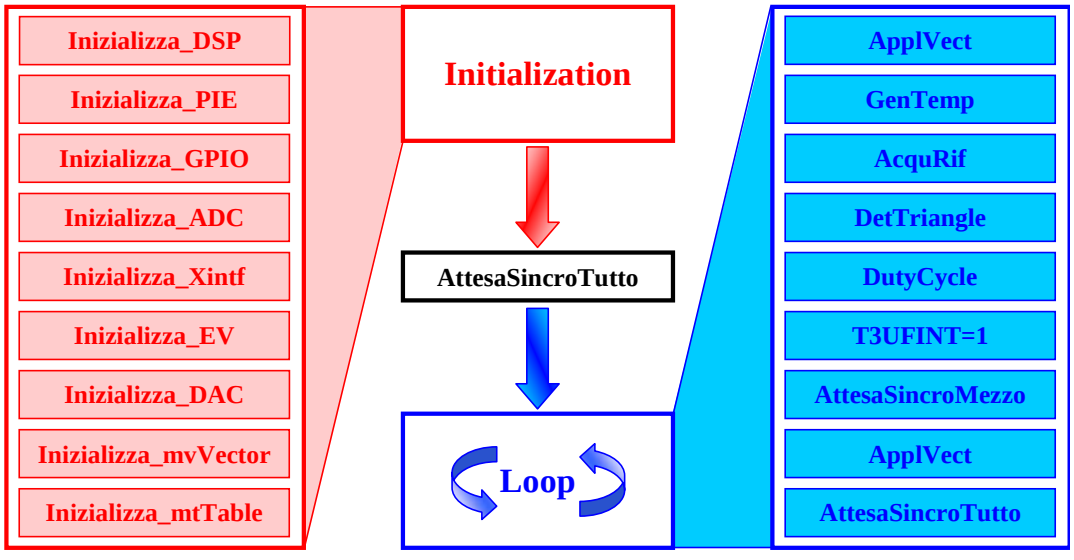


Figure 7.12: Flow diagram of the algorithm implemented on DSP.

After initialization, the algorithm waits for synchronizing with the DSP timers and then the loop begins. The loop is the core of the control software. It is never-ending and contains all the functions necessary to generate the desired gating signals.

As first task, **ApplVect** sets up the DSP to generate the proper outputs on the second half of the current cycle. Then **GenTemp** calculates time reference to be passed to **AcquRif**. This functions acquires the value of one potentiometer as amplitude and generates the rotating reference using the time just calculated.

After the reference is ready, **DetTriangle** can calculate the position in which the reference lays and can reports it to Sector I. Now, **DutyCycle** can easily calculates whole converter, inverter A and inverter B duty-cycles.

The bit **T3UFINT** is reset in order to make **AttesaSincroMezzo** work: the function waits until **T3UFINT** bit is set by the underflow of Timer 3. After this event has been occurred, **ApplVect** sets the DSP to generate the proper gating signals on the first half of the next cycle and the algorithm waits for the ending of the current cycle. Then the loop starts again.

Chapter 8

Experimental results

8.1. Introduction

8.1.1. Aim of the experiments

The reduced scale converter, the first prototype, was built to prove the effectiveness of proposed multilevel topology. During the construction of the prototype, several problems have been fixed.

The most critical problem concerns the insulation among the three grounds there are in the system. Indeed, if the insulation fails the common mode current will be free to flow and the multilevel will not work properly anymore. The first test had the aim to verify insulation applying switching voltage to only one phase, just to prove the absence of homopolar current.

Then, some tests were done to see the effectiveness of dual 2-level inverter as multilevel converter. For this purpose, a twelve-step modulation was been implemented and some screenshots have been captured.

To conclude the tests on reduced scale converter, a hybrid modulation was implemented. The aim of this test bench was to verify that the converter can be properly used with a high frequency modulation strategy.

After the test on the reduced scale converter, some test benches were implemented even for the full scale converter. On the full scale converter, the SVM and the power sharing capability were tested.

8.2. Reduced scale converter

8.2.1. Common mode voltage

The first test which had been carried out was aimed to prove the insulation among the three grounds of the system. It has been executed keeping five legs on low state and modulating the other one at 10 kHz. In this way, one of the two 3-phase inverters was held in a null configuration acting

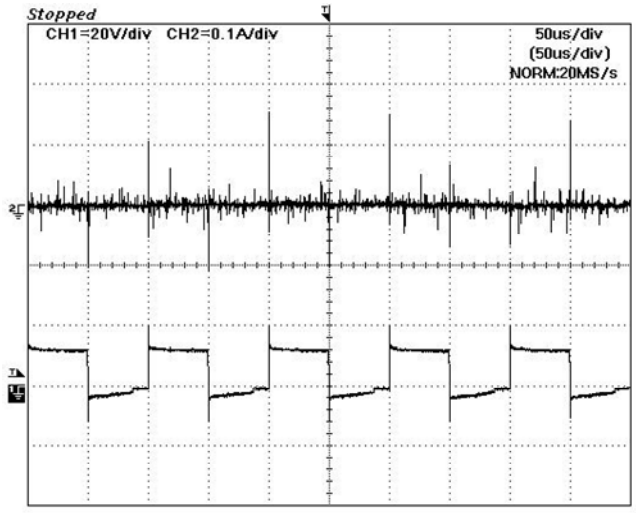


Figure 8.1: Common mode current and voltage on dual 2-level inverter.

as neutral point. The other inverter, due to the modulation of one phase, was able to impose homopolar voltage which made the neutral point float creating common mode voltage between negative poles.

Figure 8.1 shows common mode current and voltage. Despite there is a common mode voltage, the insulation prevents common mode current flow, as expected.

8.2.2. Twelve-step implementation

A twelve-step modulation has been implemented to investigate the voltage levels produced by the dual 2-level inverter. Like six-step modulation for standard 3-phese inverters, twelve-step is the analogous for the multilevel converter. Indeed, all the voltage vectors on the outer hexagon are applied to the output. This can be easily seen from Figure 8.2a) or b).

In particular Figure 8.2a) shows the voltage and current in case of pure resistive load. The load phase voltage assumes all the possible levels, nine in total. Obviously, being the load a pure resistance, the current follows the voltage waveform quite closely.

The load voltage and current on a R-L load are shown in Figure 8.2b). The level assumed by voltage waveform are identical to previous case, but the current is filtered by the inductance. In fact,

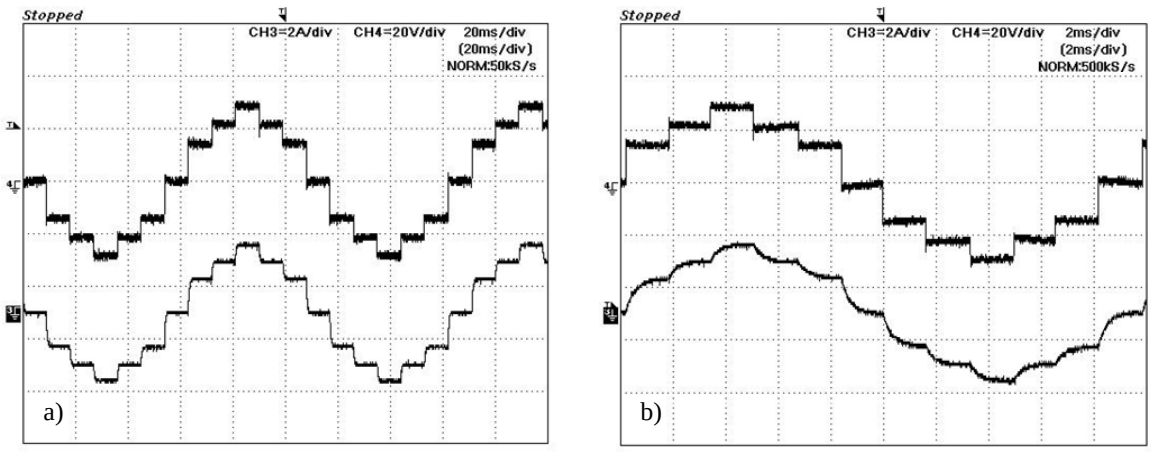


Figure 8.2: Twelve-step modulation. a) Load phase voltage and current on resistive load; b) Load phase voltage and current on R-L load.

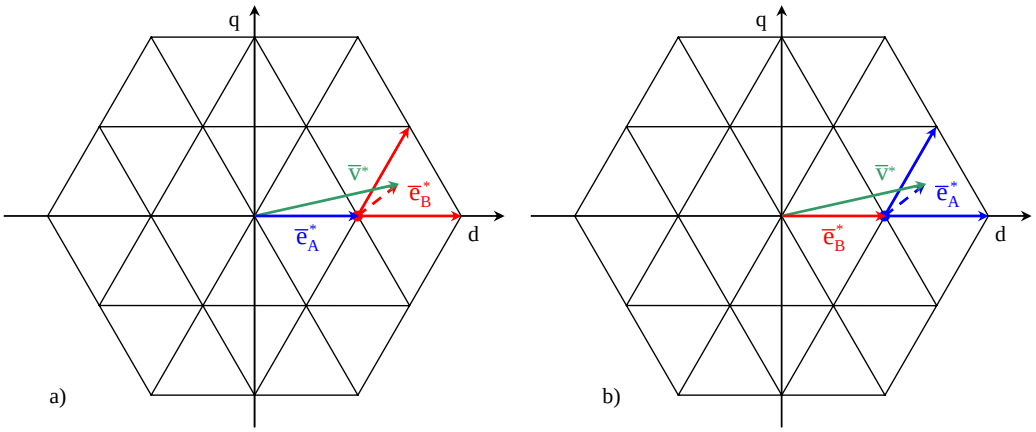


Figure 8.3: Modulation strategy implemented on the reduced scale converter. a) Inverter A is modulating in six-step, whereas inverter B is synthesizing the remaining part of the reference; b) Inverter B is modulating in six-step, whereas inverter A is synthesizing the remaining part of the reference.

the current waveform has a smoother appearance and does not show the steps.

8.2.3. Six-step and modulation

The first trial to implement SVM was done with a hybrid modulation combining six-step and the standard 3-phase 2-level SVM. One inverter was controlled to generate the active vector nearest to the reference and the other inverter was modulating the remaining part of the requested reference. This approach is schematically depicted in Figure 8.3. Figure 8.3a) shows inverter A producing the active vector (blue) nearest to the reference, whereas inverter B is synthesizing the vector difference between the reference and inverter A output (represented by a dashed red arrow). Figure 8.3b) show the reciprocal situation in which inverter A and inverter B exchange their roles. To make the modulation as symmetric as possible between the two inverters, the role exchange happens once per cycle.

Figure 8.4a) shows load phase voltage and current waveforms with the maximum sinusoidal reference, that is $\frac{2}{\sqrt{3}}$ times DC bus voltage. Being 24 V the voltage of each battery bank, the maximum sinusoidal reference is 27.71 V. Moreover, with this battery voltage, the maximum level assumed by the phase voltage is expected to be 32 V, as Figure 8.4a) clearly shows. Furthermore, Figure 8.4a) depicts that the control of the dual 2-level inverter imposes a proper multilevel

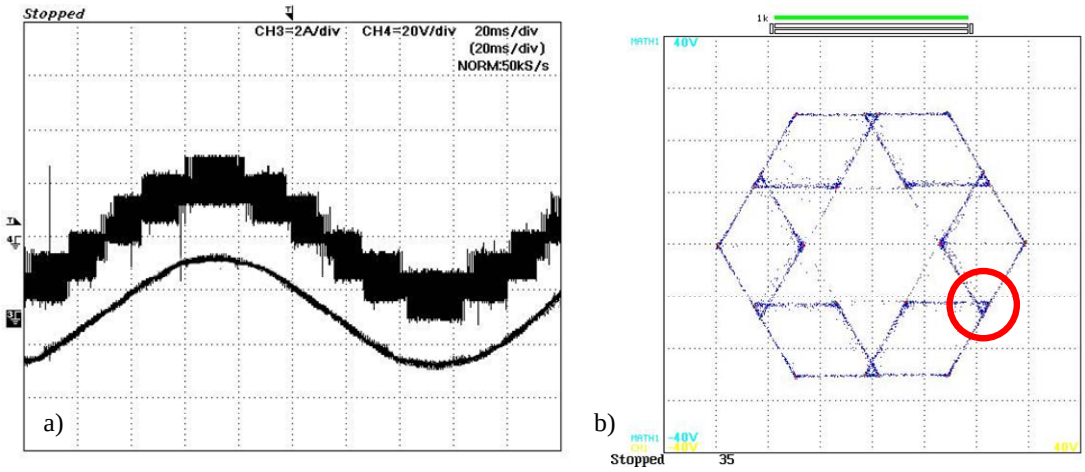


Figure 8.4: Six-step and modulation. a) Load voltage and current waveforms; b) Load voltage vector locus on d-q plane.

modulation to the converter. The level exploited in the synthesis of the output are only three in each cycle, as expected. Regarding the current, its waveform is quite good even if IGBTs forward voltage drops are not negligible with respect to the battery voltage. Figure 8.4b) shows the voltage locus on d-q plane. As expected, only outer vectors are applied. The small triangles on the borders (one of them is highlighted by a red circle) depend on the difference voltage of the two sources. This makes the voltage composition not be symmetrical: when the two inverter exchange roles they do not produce exactly the same voltage vectors.

8.3. Full scale converter

8.3.1. SVM implementation

An SVM technique has been implemented on the full scale converter at the first attempt. To verify the effectiveness of the modulation, Figure 8.5a) shows load phase voltage and current with a reference on the outer hexagon, quite near to the maximum sinusoidal reference. Being 80 V on the DC busses of the full scale converter, the maximum sinusoidal allowed reference voltage is 92.37 V, whereas the maximum applied voltage is 106.66 V.

The voltage waveform, shown in the top of Figure 8.5a), highlight the correct multilevel

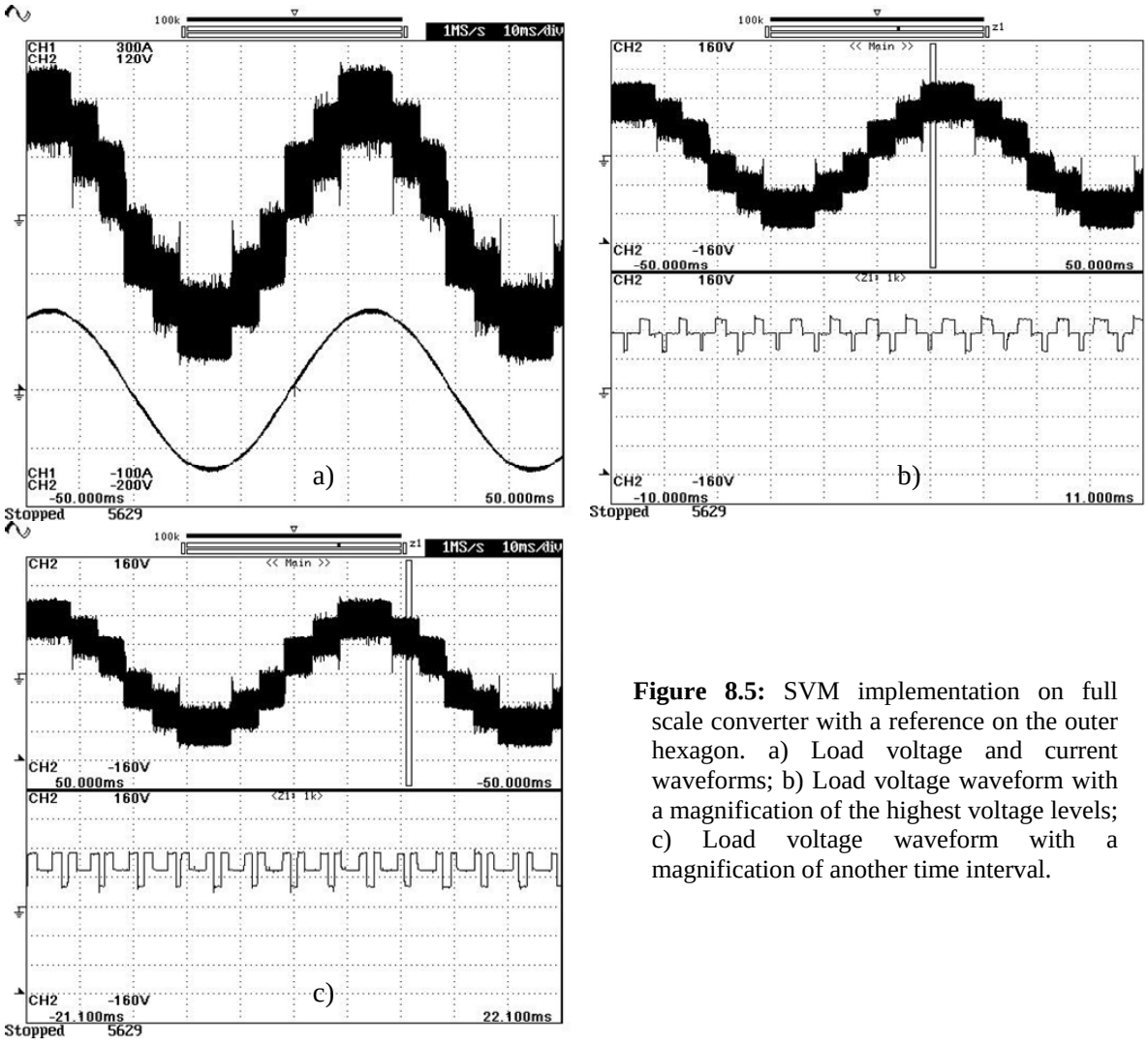


Figure 8.5: SVM implementation on full scale converter with a reference on the outer hexagon. a) Load voltage and current waveforms; b) Load voltage waveform with a magnification of the highest voltage levels; c) Load voltage waveform with a magnification of another time interval.

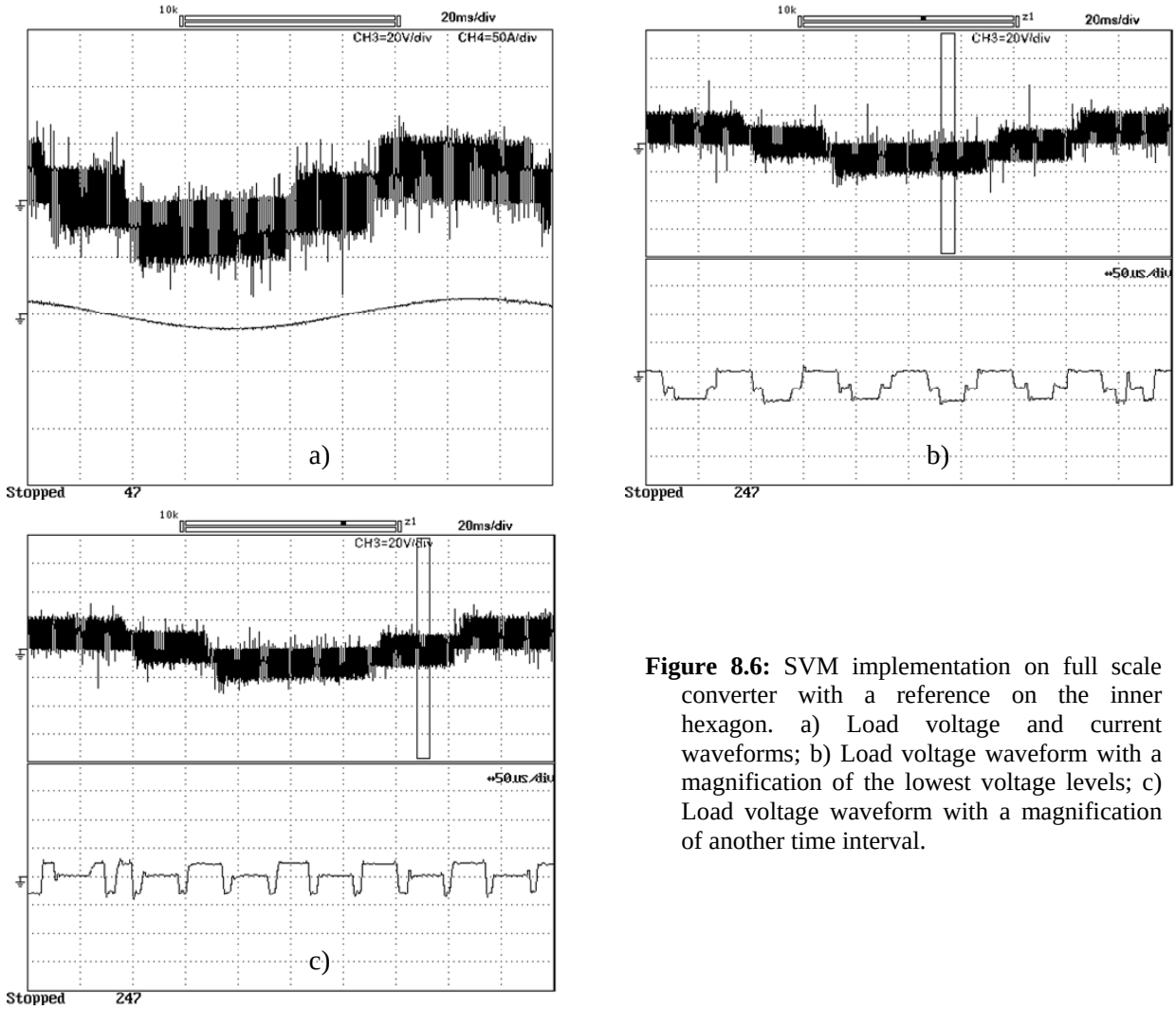


Figure 8.6: SVM implementation on full scale converter with a reference on the inner hexagon. a) Load voltage and current waveforms; b) Load voltage waveform with a magnification of the lowest voltage levels; c) Load voltage waveform with a magnification of another time interval.

modulation of the converter. The current is quite close to a perfect sinusoid. Figure 8.5b) and c) show the level assumed by the voltage during a cycle. Indeed the three levels assumed by the voltage are clearly visible.

Figure 8.6a) shows load phase voltage and current waveforms when the reference is inside the inner hexagon, so it is expected a smaller number of voltage levels applied to the load than in the previous case. In fact, the voltage levels applied are five instead of 9, as a proper multilevel modulation requires. Figure 8.6b) and c) show that only three voltage levels are used in a cycle, even when the reference is inside the inner hexagon.

8.3.2. Power sharing

To conclude the overview of experimental results, some screenshots proving the effectiveness of power sharing technique will be shown.

The phase voltage oprovided by the two inverters are filtered using a low pass filter with cut frequency of 500 Hz. In this way only the fundamental harmonic is considered. Being the current equal for both inverters, the mean voltage on a cycle is proportional to the power delivered by the inverter itself. In this way it is possible to verify power sharing only looking at voltage amplitudes.

Figure 8.7a) shows the powers delivered by the two inverters with a power sharing coefficient equal to 0.5. In this case both inverters are forced to deliver the same power to the load and their output voltage have the same amplitude, but opposite phases.

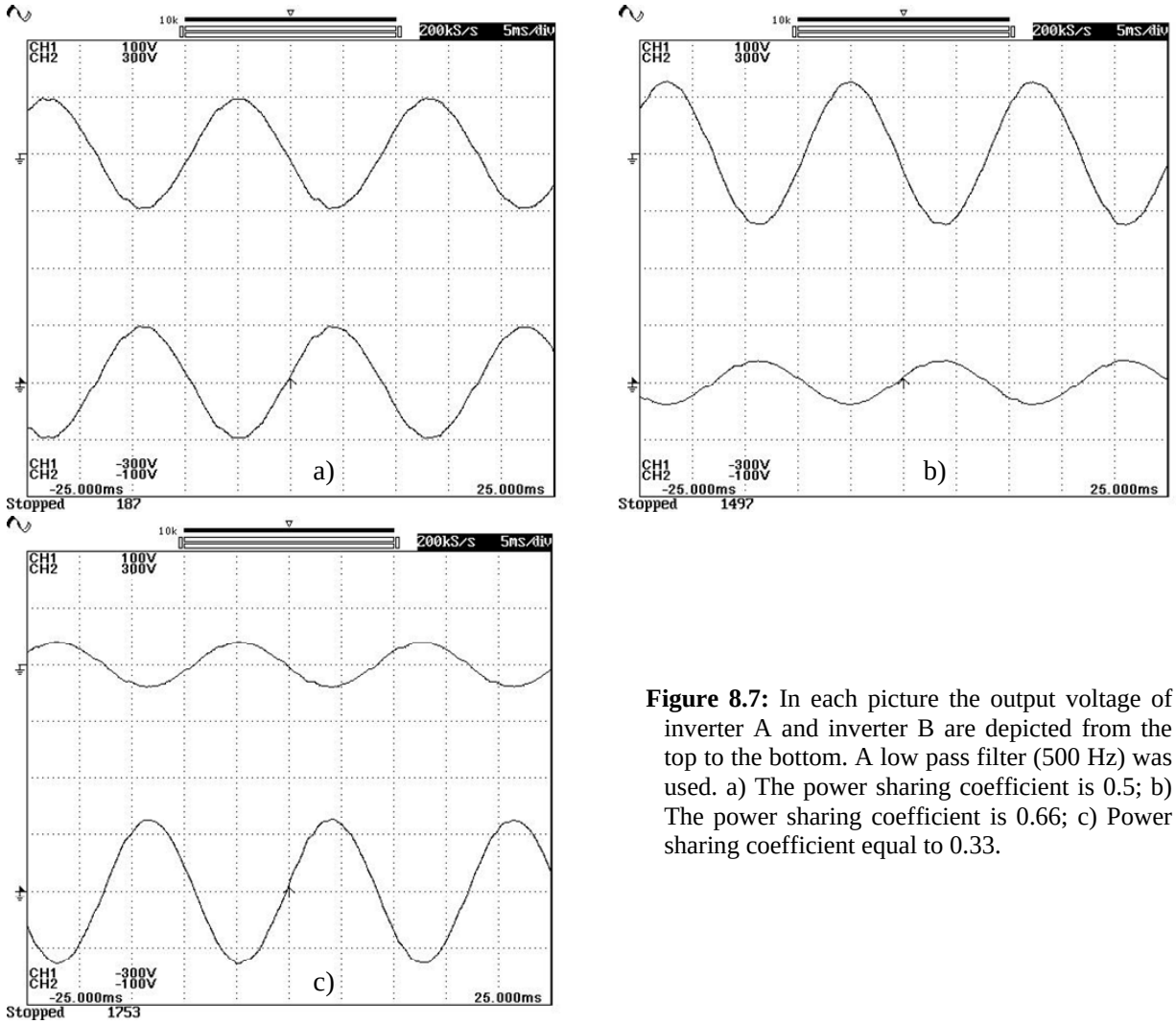


Figure 8.7: In each picture the output voltage of inverter A and inverter B are depicted from the top to the bottom. A low pass filter (500 Hz) was used. a) The power sharing coefficient is 0.5; b) The power sharing coefficient is 0.66; c) Power sharing coefficient equal to 0.33.

When the power sharing coefficient is set to $\frac{2}{3}$, inverter A delivers twice the power inverter B does. In this case, the amplitude of inverter A output is twice with respect to inverter B, as Figure 8.7b) clearly shows.

The opposite situation is shown by Figure 8.7c), captured when the power sharing coefficient was set to $\frac{1}{3}$: the voltage inverter A produces is half of that inverter B produces, as well as delivered powers.

It is clear, from Figure 8.7, that the implemented power sharing algorithm works properly, allowing the users to share the powers coming from the DC sources with a ratio imposed by the control and not only by the evolution of the system.

8.4. Conclusion

8.4.1. Conclusion

The dual 2-level inverter is a converter structure composed by two standard 3-phase 2-level inverters, parts widely commercialized and reliable. That allows to construct this kind of converter using standard parts, instead of using custom made components as other multilevel converters

require. This is a great advantage of dual 2-level inverter against diode-clamped and flying-capacitor structures.

On the other hands, more dual 2-level inverters can not be cascaded to increase the number of levels because this connection will determine short-circuits among the DC sources. This can be considered the principal limit of the converter. Hence, the maximum number of voltage levels which can be produced on the load phase voltages is 9.

The dual 2-level inverter requires only two insulated DC sources: this represent both an advantage and a disadvantage. Surely, in many applications is easily to create two insulated sources instead of the three cascade H-bridge requires, but the insulation is so critical which has to be taken into account carefully. Indeed, just a creep in the insulation allowing a path for the homopolar current will stop the correct operation of the converter. A careful design of the boards and a correct placement of photo-couplers can warrant the required insulation.

Despite of this critical drawback, the dual 2-level inverter is suited for several applications. First of all, it can be adopted in automotive traction systems to overcome the limits on the maximum power still present. In industrial traction applications there is a limit on the allowed maximum voltage of battery banks for safety reasons. In Italy this limit is 96 V. In other land traction application, the limit on maximum voltage are imposed by the market: the cost of power MOSFET has its minimum for the components rated about 150 V. These limits on the voltage, together to the maximum current allowed by the switches, draw the limits of drive power. Indeed, the dual 2-level inverter can upgrade the power of an existing drive exploiting the same components still used.

Moreover, the power sharing, controlling the power flows through the two inverters, is useful to balance battery discharge and keep the life of the drive longer. But this is not the only advantage that power sharing can offer. In other applications, power sharing can be used to optimize the efficiency of the system. This is the case of hybrid naval propulsion, where the dual 2-level inverter can be fed by two diesel engines which work always at the maximum of their efficiency. When the required power is quite low, only one engine and one inverter will work. When the request of power is high, both engines end both inverters will work. In this case, using the power sharing capability is possible to deliver power making the diesel engines operate at high efficiency.

Lately, a third application has been found: the dual 2-level inverter can be used as active filter fed by photovoltaic panels. The coupling between the converter and the grid is done by a transformer with six-wire on one side (converter) and a standard connection on the other one (grid).

All this applications make the dual 2-level inverter be an interesting structure to be investigated. Several peculiarities must be examined deeply and several other characteristics must be found and studied. If the investigation on this converter continues for the right amount of time, it could reveal to be a good deal both in scientific and commercial field.

Appendices

Appendix 1

Comparison among drives

A1.1. Introduction

A1.1.1. Standard 3-phase induction motor drive

A comparison, considering also the economical aspect, among the different possibilities available to increment the power in traction applications can be interesting to conclude this work. First of all it is important to advise that the determination of the correct price of each solution is a hard task and, sometimes, can be even impossible because some parts can be not commercial, so their costs are not truthful.

In Figure A1.1 is schematically represented the standard drive adopted in traction applications. In the following it will be the model to which compare other solutions. To be as clear as possible, it will be called **standard solution**.

The motor is supposed to be a 3-phase induction machine. To control this kind of motor, 3-phase 2-level inverter is required together with all the necessary control circuitries. Finally, to complete the system, one battery bank is needed.

The definition of the power rates is important to make the comparison be meaningful, indeed prices can vary a lot dependently on the power for which the system is rated. First of all, due to the standard in force, the battery bank is supposed to be rated 96 V, just to consider both industrial and road vehicles at once.

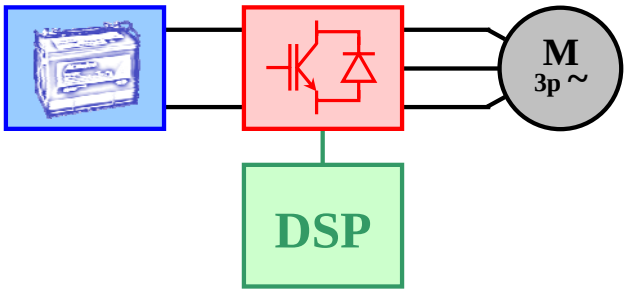


Figure A1.1: Standard drive used in traction application.

AC SINGLE INVERTERS MAIN MODELS	24V	36V	48V	72V	80V	96V
AC-X SSL	100A	100A	100A			
AC-0 SSL	150A	150A				
AC-0 PLUS	200A	200A				
AC-1 SSL	250A	250A	225A		160A	
ACE2 350	350A	350A	350A			
ACE2 450	450A	450A	450A			
AC2 FLASH	500A	450A	450A	400A	400A	
AC3 FLASH		600A	600A	600A	600A	350A
AC4		750A	750A	650A	650A	450A

Table A1.1: Inverter gamma proposed by Zapi.

After the determination of DC voltage, it is possible to look for the inverter matching the 96 V requirement. One of the most famous Italian factory which manufactures industrial drives proposes the inverter table shown in Table A1.1. The inverter allowing the greatest power is rated 80 V and 650 A of DC bus current. This model is chosen to be part of the drive.

Regarding the control, a standard TMS320F2812 DSP can be used together with a custom-built control board providing the necessary support to the microprocessor.

To complete the system, a low voltage motor has been chosen. Accordingly to the limits on the voltage and current imposed by the inverter, it can be rated 56 V, 220 A.

To conclude, some prices can be given for the proposed parts. The value of the inverter can be estimated about 800 € . The same price is attributable to the motor. The price for a 80 V battery bank rated 560 Ah is 7000 € more or less. Regarding the control, 300 € can be a good estimation of costs. Hence the total cost for a 12 kW drive is 8900 €.

A1.1.2. Alternative solutions

The first idea to increment drive power can be to double the power rating for each part. This is possible for battery bank, if there is sufficient room in the vehicle. Unfortunately, finding a commercial inverter rated 1300 A is almost impossible. Hence, this part has to be custom-built incrementing a lot its price. Moreover, MOSFETs rated 1300 A are not so common and can be difficultly tracked down.

Other solutions have to be taken into account. For instance, it is possible to double the drive and shrink one motor on each tractor wheel, as represented in Figure A1.2. This system will be called **two motors solution**.

Other two possibilities are given by using the double 3-phase motor or the dual 2-level inverter. The two systems are represented in Figure A1.3 and Figure A1.4 respectively. They will be called **double 3-phase solution** and **dual 2-level inverter solution** just to fix univocally the names.

In the following Section, a punctual analysis of all the three alternative solutions will be done with the purpose to make a comparison among them using the standard solution presented above as common reference.

A1.2. Analysis of alternative solutions

A1.2.1. Two motors solution

This solution is the most easy to be implemented, even if a restructuring of vehicle bodywork must be necessary to fit the two electrical motors. As can be seen from Figure A1.2, the system is composed by two inverters, two motors, two control circuitries and one battery bank.

Actually, the picture shows two battery banks to highlight the idea that twice the energy stored in standard solution is needed to insure the same autonomy of the vehicle. Anyway, the battery bank can be a single unity even in this case.

Also the control does not need to be doubled, but a more complex circuit or software is surely necessary to properly drive the system. Hence, the cost of the control system can be evaluated about 1.5 times the cost of the standard solution.

Economically, the two motors solution costs more or less twice the standard solution because all the costs are doubled, but the control. To be rigorous, the costs for the implementation of this solution can be estimated in 17700 €.

Economical the cost for unity of power is unchanged with respect to the standard solution if the analysis does not take into account mechanical parts. Indeed vehicles are built following some standards, which expect a single engine. Hence, fit the two motors can be difficult in a commercial bodywork. Moreover, the two motors must be shrunken on the wheels to avoid the use of particular differential gears. This is not so common and may require the study of special bearings.

Another drawback can be found in the reliability of the system. Indeed, both inverters must operate simultaneously to make the vehicle move in a straight way. So in case of fault of one part, the vehicle must stop its march. One objection to this way of reasoning can be to assert that in standard solution happens the same. This is correct, but in standard solution the number of components in the system is smaller as far as the fault probabilities.

Considering all these facts, the two motors system can be a viable solution to the problem of doubling the power of a standard 3-phase induction motor drive for traction applications. Actually, there are other possibilities which arise to be better solutions and more fault tolerant.

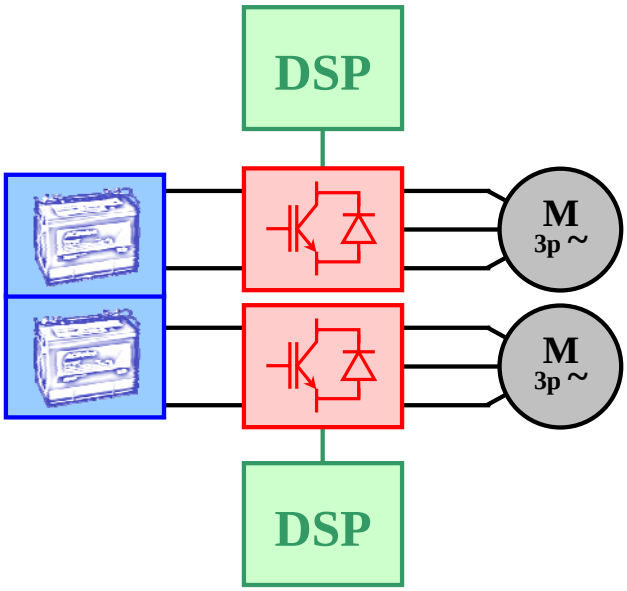


Figure A1.2: Two motors solution.

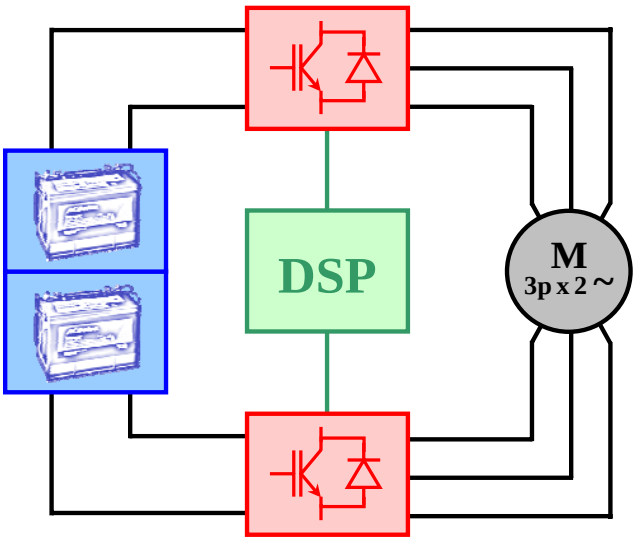


Figure A1.3: Double 3-phase motor solution.

A1.2.2. Double 3-phase motor solution

This system is composed by a battery bank of the same size as the one in two motors solution, a control circuit which can be implemented using a TMS320F2812, two inverters and one motor rated for double the power than standard solution.

The peculiarity of the motor is to be wound with two 3-phase windings displaced of thirty electrical degrees. In this way, referring to the same voltage as in standard solution the power is twice because the current injected in the motor is doubled. Unfortunately this is not sufficient to estimate the price of the motor. Other considerations must be done. First of all, the difference between the required motor and a standard one is only the type of winding. Hence the increment of price due to the special windings can be neglected. Moreover, the increment of power is supposed to be obtained as increment of torque: this means that the deepness of the motor is doubled, but the sheets are unchanged. With these considerations, a value slightly less than the double of the motor in standard solution can be estimated.

The cost of the whole system can be quantified in about 17600 €, that is not so less to justify the adoption of this choice than the two motor solution.

The increment of reliability of the system intervenes in favour of this solution. In fact, in case of fault of one windings or one inverter, the vehicle is still able to move. When such a kind of fault happens, the broken part can be cut off and the motor can be fed as a standard 3-phase motor. Obviously the power is decreased because the maximum current is halved as far as the maximum torque, but the vehicle can be still controlled by the driver.

This system has to be preferred to two motors solution because it is more fault tolerant, even if the reduction of torque makes the vehicle unable to cover steep slopes or to move at full load. Moreover, this solution can be easily adapted to standard bodyworks designed for internal-combustion engines.

A1.2.3. Dual 2-level inverter solution

To conclude this comparison, the dual 2-level inverter solution is described. This system is represented in Figure A1.4. It is composed by two battery banks which absolutely need to be electrically insulated. Anyway, this necessity does not increment the cost of batteries, which can be specifically connected for this purpose. The two inverters, the control circuit and the motor are

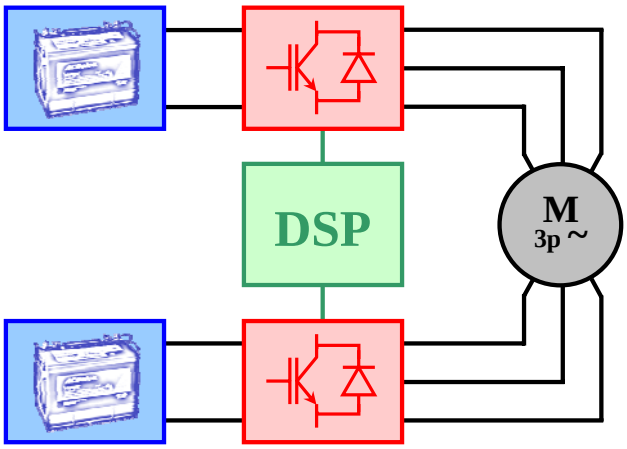


Figure A1.4: Dual 2-level inverter solution.

standard parts. Hence the total cost of this solution can be estimated to be equal to double 3-phase motor solution and can be fixed in17600 €.

Economically, dual 2-level inverter and double 3-phase motor solutions are equivalent and not so cheaper to justify their implementation instead of the two motors solution.

The advantages of this system are in its robustness. Indeed it can be considered more fault tolerant than the double 3-phase motor system. In case of fault, the broken part can be cut off, simply short-circuiting the conductors nearby the motor. In this way, the system decreases the maximum power, as the double 3-phase motor solution, but in this case is the maximum voltage to be halved. Being the current injected in the motor unchanged, the maximum torque the system can transmit to the wheels is the same in all the operating conditions, but the maximum speed is halved in case of fault. Hence, using this system the vehicle is able to cover the same roads both when it is healthily and in case of fault allowing the users to reach a garage.

Appendix 2

Power Balancing of a Multilevel Converter with Two Insulated Supplies for Three-Phase Six-Wire Loads

Power balancing of a multilevel converter with two insulated supplies for three-phase six-wire loads

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Keywords

Converter control, Modulation strategy, Multilevel converters, Voltage Source Inverters (VSI)

Abstract

A multilevel converter topology feeding three-phase open-end winding loads is considered in this paper. The scheme is based on two insulated dc supplies, each one feeding a standard two-level, three-phase inverter. A three-phase, six wires load is connected across the output terminals. A new modulation technique able to regulate the sharing of the output power between the two dc sources within each switching cycle is presented. The performance of the whole system has been verified by numerical simulations.

1. Introduction

In battery powered electric vehicles the standard solution for the traction system is given by a two-level inverter feeding a three phase motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V). With this solution the practical feasibility of a high power ac drive (>20 kW) is limited mainly by the high cost of the semiconductor power switches of the inverter due to the resulting high current rating.
The high cost together with the circuit complexity due to the parallel connection of the power switches can prevent the realization of standard three-phase drives for the traction system of heavy electric vehicles, such as buses, industrial truck, etc…
A viable solution introduced to overcome this problem is given by the use of a six-phase machine supplied by a six-phase inverter [1]-[4]. This solution allows sizing the power switches at half the rated current of an equivalent three-phase scheme, but requires the realization of a six-phase machine.
Another solution for high power electrical drives is the use of a multilevel inverter, which can be realized with semiconductor devices having lower voltage rating. The typical structure of such a system was introduced in [5] and, nowadays, it is widely used to drive three-phase electrical machine with high supply voltages. Several topologies of multilevel converters have been also presented for low voltage applications [6]. Among these, the cascaded converter can be conveniently used with a battery supply system, because it is relatively easy to split the supply in several electrically separated sources.
In this paper a multilevel converter composed of a dual two-level inverter feeding open-end, three-phase ac motor [7]-[9] is considered. The scheme of the multilevel converter is shown in Fig.1. This

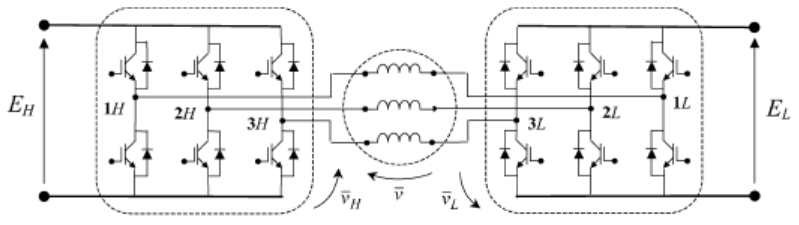

Fig.1: Multilevel converter for six-wire applications composed of two traditional two-level inverters.

scheme is based on the use of two insulated supplies, each one feeding a standard, three-phase two-level inverter. A three-phase, six-wires load is connected across the six output terminals of the inverters. The two separate dc sources can be easily obtained on board of an electric vehicle by splitting the batteries in two separate banks.
This solution should be preferred to other multilevel configurations because of some advantages: no generation of common mode (zero sequence) currents on the motor winding, best dc bus voltage utilization, use of two standard three-phase, two-level inverters.
New switching techniques, based on a proper application of the space vector modulation (SVM), are presented in the paper. The main feature of these techniques is the capability to regulate the load power sharing between the two dc sources. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks.
Furthermore, the dual inverter topology is a high reliability solution. In case of fault in one inverter, it must be short-circuited at the output terminals, and the drive can be operated using the other one as a standard three-phase two-level inverter. This possibility allows the operation of the motor at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed).

2. Multilevel Modulation Strategy

With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector $\bar{v}$ is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter H and inverter L, respectively,

$$\bar{v} = \bar{v}_H + \bar{v}_L . \tag{1}$$

The voltages $\bar{v}_H$ and $\bar{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to

$$\bar{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\, e^{j\frac{2}{3}\pi} + S_{3H}\, e^{j\frac{4}{3}\pi}\right) \quad \text{and} \quad \bar{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\, e^{j\frac{2}{3}\pi} + S_{3L}\, e^{j\frac{4}{3}\pi}\right), \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs. A space vector representation of $\bar{v}_H$ and $\bar{v}_L$ is given in Fig. 2.
The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 3(a). By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 E. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2E/\sqrt{3}$ (i.e., the radius of the inscribed circle).

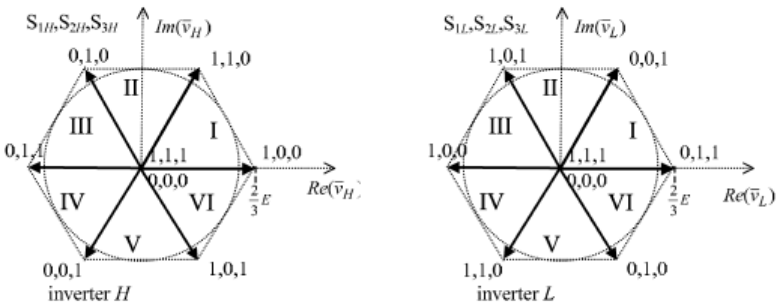

Fig.2: Switch configurations, sectors, and corresponding voltage vectors for inverters H and L.

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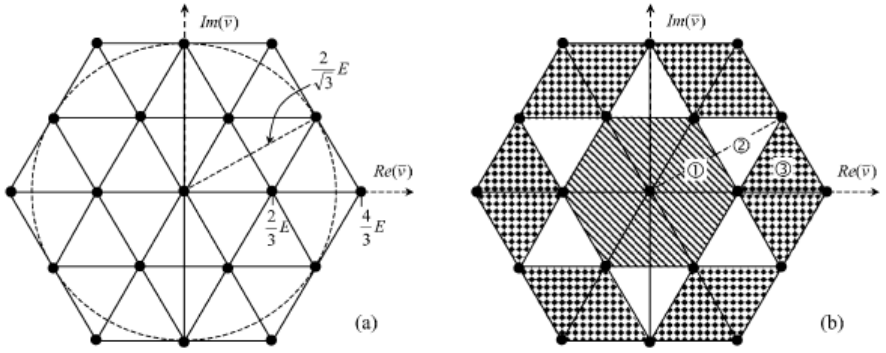


Fig. 3: (a) Output voltage vectors generated by the dual, two-level inverter.
(b) Highlight of the triangles in the three different regions ①, ②, and ③.

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 3(b), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted).
In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\bar{v}$ is synthesized by using the vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, as represented in Fig. 4 for the three types of triangles.
Considering the standard SVM technique, $\bar{v}$ is obtained as

$$\bar{v} = \mu \bar{v}_A + \lambda \bar{v}_B + \gamma \bar{v}_C, \tag{3}$$

where the duty cycle μ, λ, γ can be determined as

$$\begin{cases} \mu = \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \lambda = -\dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_A - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \gamma = 1 - (\mu + \lambda) = 1 - \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_A)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \end{cases} . \tag{4}$$

A simple modulation strategy consists of modulating one inverter in the six-step mode, i.e., $\bar{v}_H = \bar{v}_C$, and the other inverter in the SVM mode for generating the residual output voltage $\bar{v}_L = \bar{v} - \bar{v}_C$. As an example, Fig. 5 shows the vector composition considering $\bar{v}$ laying in the outer triangle (region ③).
This simple modulation technique leads to a power unbalance between the two inverters. In fact, the inverter voltages ($\bar{v}_H$, $\bar{v}_L$) have different magnitude and different phase angle with respect to the out-

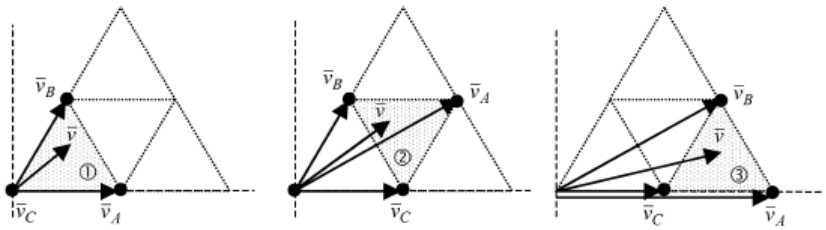


Fig.4: Voltage vectors used for generating the output voltage in the three regions.

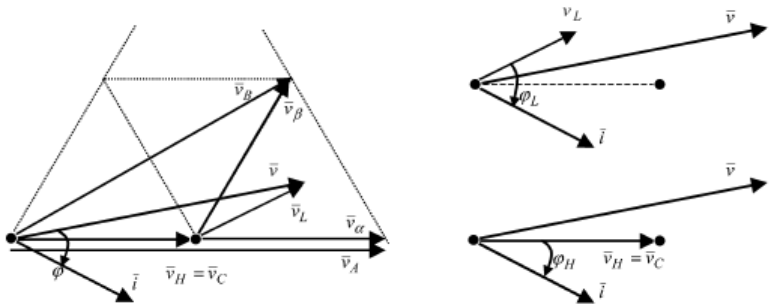


Fig.5: Vector composition of the output voltage combining six-step mode and SVM mode for the two inverters.

put current $\bar{i}$ (the same for both), as shown in Fig. 5.
The problem of balancing the power between the two dc sources could be solved in a simple way, by exchanging the role of the inverter operating in the six-step mode with the one operating in the SVM mode. The commutation can be actuated during a switching period, a triangle change, or a fundamental period. This solution is satisfactory for exactly balancing the powers, but does not allow any different regulation of the power sharing.

3. Regulation of the Power Sharing

A novel modulation technique, able to regulate the power sharing between the two dc sources, is presented in this section. The balanced operation can be considered a particular case.
Introducing the power ratio k, the output power p (average value over a switching period) can be shared between the dc sources (H and L) according to

$$p = \frac{3}{2}\bar{v}\cdot\bar{i} = p_H + p_L \quad \rightarrow \quad \begin{cases} p_H = \frac{3}{2}\bar{v}_H\cdot\bar{i} = k\cdot p \\ p_L = \frac{3}{2}\bar{v}_L\cdot\bar{i} = (1-k)\cdot p \end{cases} \tag{5}$$

Assuming the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ in phase with the output voltage vector $\bar{v}$, (5) leads to

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \end{cases}. \tag{6}$$

Fig. 6 shows the particular case with k = 0.5 corresponding to $\bar{v}_H = \bar{v}_L = 1/2\ \bar{v}$, i.e., balanced power for the dc sources. In order to synthesize an output vector $\bar{v}$, the two inverters must generate the corresponding fraction of $\bar{v}$ by applying only their active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector. Being $\bar{v}_H$ and

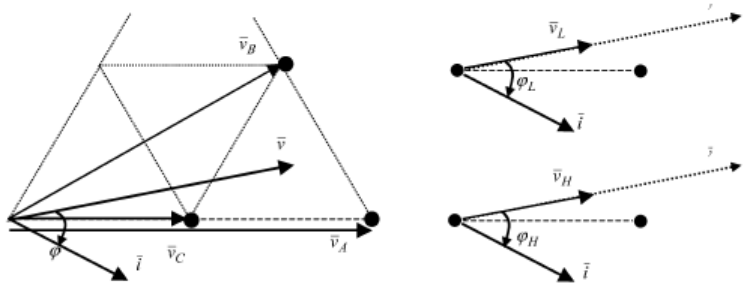


Fig.6: Vector composition of the output voltage with balanced power between the inverters (k = 0.5).

$\bar{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$, as shown in Fig. 7.

The duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *H*. The duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *L*. In this way, the voltage generated by the two inverters are

$$\begin{cases} \bar{v}_H = \mu_H \bar{v}_\alpha + \lambda_H \bar{v}_\beta \\ \bar{v}_L = \mu_L \bar{v}_\alpha + \lambda_L \bar{v}_\beta \end{cases} . \tag{7}$$

By using standard SVM equations, the duty-cycles of inverters *H* and *L* are given by

$$\begin{cases} \mu_H = \dfrac{\bar{v}_H \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \gamma_H = 1-(\mu_H+\lambda_H) = 1-\dfrac{\bar{v}_H \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \end{cases} \text{ and } \begin{cases} \mu_L = \dfrac{\bar{v}_L \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_L = -\dfrac{\bar{v}_L \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \gamma_L = 1-(\mu_L+\lambda_L) = 1-\dfrac{\bar{v}_L \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \end{cases} . \tag{8}$$

4. Determination of the Operating Limits

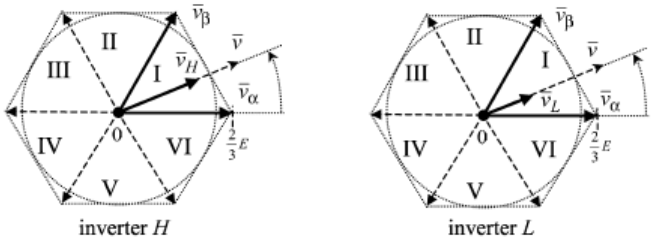
The constrains of the duty-cycles expressed by (8) are

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases} \text{ and } \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases} . \tag{9}$$

These constrains introduce a limit in the range of variation of the power ratio *k*. In particular, the range of variation of *k* can be evaluated as a function of the desired output vector $\bar{v}$. Introducing in (9) the expressions (8) of duty cycles, and representing $\bar{v}_H$ and $\bar{v}_L$ in terms of *k* by (6), leads to

$$\begin{cases} \dfrac{k\bar{v} \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\dfrac{k\bar{v} \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \dfrac{k\bar{v} \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1 \end{cases} \text{ and } \begin{cases} \dfrac{(1\text{-}k)\bar{v} \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\dfrac{(1\text{-}k)\bar{v} \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \dfrac{(1\text{-}k)\bar{v} \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1 \end{cases} . \tag{10}$$

The solution of (10) can be found in each one of the six sectors where $\bar{v}_H$ and $\bar{v}_L$ can be located.



inverter *H* inverter *L*

Fig.7: Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

If the output voltage vector is written as $\bar{v} = Ve^{j\vartheta}$, the modulation index m can be defined as

$$m = \frac{V}{\frac{2}{\sqrt{3}}E}, \quad 0 \le m \le 1 \text{ for sinusoidal output voltages.} \tag{11}$$

Then, with reference to sector I ($0 \le \vartheta \le \frac{\pi}{3}$), the solution of (10) is given by

$$\begin{cases} k \le \dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \\ k \ge 1-\dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \end{cases} \rightarrow \quad \frac{1}{2}-a \le k \le \frac{1}{2}+a \quad \text{being} \quad a = \frac{1-m\,cos(\pi/6-\vartheta)}{2m\,cos(\pi/6-\vartheta)}. \tag{12}$$

Eq. 12 gives the possible values of k as a function of the modulation index m and the output voltage phase angle ϑ. It can be noted that for any modulation index, the most stringent condition for k is given in the middle of the sector, i.e. for $\vartheta = \pi/6$. Fig. 8 represents the boundaries of k as a function of the phase angle ϑ for $m = 1$ and $m = 2/3$.
Similar considerations can be made for the other sectors (II ÷ VI).
In most applications is required to share the output power between the dc sources in equal parts. This means that k must be fixed to 0.5 during the whole fundamental period, $0 \le \vartheta \le 2\pi$.
If the maximum output voltage is required ($m = 1$), there is no possibility to regulate the power sharing between the dc sources. In this case only the value $k = 0.5$ is admissible, as shown in Fig. 8.
For values of the modulation index lower than 1, the parameter k can be changed, under the limits imposed by (12). Fig. 9 shows the upper and lower limits of k with reference to sinusoidal output voltages as a function of the modulation index m. It can be noted that for $m < 0.5$ the power ratio k can be greater than unity and lower than zero. It means that an amount of power can be transferred from a dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase oppositions, as shown by (5) and (6). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources. In this paper only the range $0 \le k \le 1$ is discussed.
For $m \le 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if k is set to 0 all the load power is supplied by inverter L, whereas if k is set to 1 all the load power is supplied by inverter H. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only.

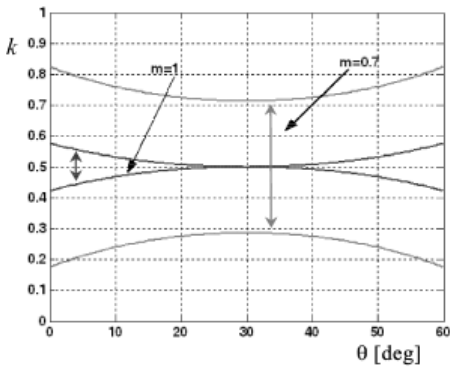


Fig. 8: Possible values of the power ratio k for modulation indexes $m = 1$ (blu) and $m = 0.7$ (red).

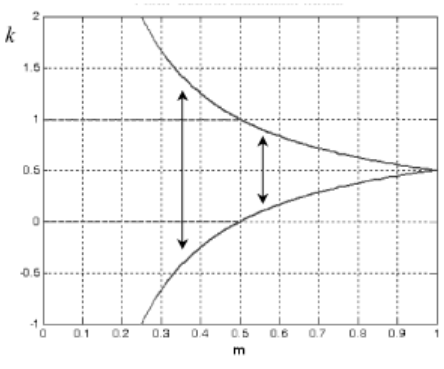


Fig. 9: Limits of the power ratio k as function of the modulation index m.

5. Determination of the Switching Sequence

Once the limits for k has been defined, and the required inverter voltages $\bar{v}_H$ and $\bar{v}_L$ have been determined, the duty-cycles $\mu_H, \lambda_H, \gamma_H$ and $\mu_L, \lambda_L, \gamma_L$ can be calculated by (8). As stated above, for achieving a correct multilevel operation, the three vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, adjacent to the desired output voltage vector $\bar{v}$, must be generated by properly combining active vectors ($\bar{v}_\alpha, \bar{v}_\beta$) and null vector of the two inverters. For regions ①, ②, and ③ shown in Figs. 3 and 4, three different vector compositions are defined, according to the following equations

Region ① Region ② Region ③

$$\begin{cases} \bar{v}_A = \bar{v}_\alpha + 0 \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = 0 + 0 \end{cases} \text{(a)} \qquad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \text{(b)} \qquad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \text{(c)} \qquad (13)$$

On the basis of (13), the duty-cycles for the vectors $\bar{v}_\alpha, \bar{v}_\beta$ and 0 of inverters H and L, can be related to the duty-cycles μ, λ, γ of the output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$ calculated in (4). It can be noted that $\bar{v}_\alpha, \bar{v}_\beta$ and 0 are the same vectors for the two inverters. Then, when the output vector $\bar{v}_\alpha$ must be applied, the application time of $\bar{v}_\alpha$ can be subdivided in two sub-intervals. In the first time interval, inverter H generates $\bar{v}_\alpha$ and inverter L generates 0. In the second time interval, inverter L generates $\bar{v}_\alpha$ and inverter H generates 0. The same procedures can be adopted for generating the output vectors $\bar{v}_\beta$ and $\bar{v}_\alpha + \bar{v}_\beta$. For the other possible output vectors, $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and 0, the subdivision is trivial. The resulting switching sequence inside a switching period is represented in Tab. I with reference to all the three regions ①, ②, and ③.

The sub-intervals introduced in Tab. I can be determined for the three different regions on the basis of main duty-cycles μ, λ, γ and duty-cycles $\mu_H, \lambda_H, \gamma_H$, $\mu_L, \lambda_L, \gamma_L$ of the two inverters, as follows

Region ① Region ② Region ③

$$\begin{cases} \mu' = \mu_H \\ \mu'' = \mu_L \\ \lambda' = \lambda_H \\ \lambda'' = \lambda_L \\ \gamma \text{ is known} \\ - \end{cases} \text{(a)} \qquad \begin{cases} \mu' + \gamma' = \mu_H \\ \mu'' + \lambda' = \lambda_H \\ \lambda'' + \gamma'' = \gamma_H \\ \mu'' + \gamma'' = \mu_L \\ \mu' + \lambda'' = \lambda_L \\ \lambda' + \gamma' = \gamma_L \end{cases} \text{(b)} \qquad \begin{cases} \mu \text{ is known} \\ - \\ \lambda' = \lambda_L \\ \lambda'' = \lambda_H \\ \gamma' = \gamma_L \\ \gamma'' = \gamma_H \end{cases} \text{(c)} \qquad (14)$$

It can be noted that for regions ① and ③ the sub-intervals are five, whereas for region ② the sub-intervals are six and they can be determined by solving a system of six equations. Only five of these equations are linear independent. In fact, the sum of the first three equations in (14b) gives the same result than the sum of the last three equations, as expressed by (8). Then, the equation system (14b) can be solved in parametric form. Assuming γ' as parameter, the sub-intervals result

Table I: Resulting switching sequence for multilevel operations

	region ①					region ②						region ③				
output vectors	$\bar{v}_A = \bar{v}_\alpha$		$\bar{v}_B = \bar{v}_\beta$		$\bar{v}_C = 0$	$\bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta$		$\bar{v}_B = \bar{v}_\beta$		$\bar{v}_C = \bar{v}_\alpha$		$\bar{v}_A = 2\bar{v}_\alpha$	$\bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta$			$\bar{v}_C = 0$
$\bar{v}_H$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0
$\bar{v}_L$	0	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$
duty cycles	μ'	μ"	λ'	λ"	γ	μ'	μ"	λ'	λ"	γ'	γ"	μ	λ'	λ"	γ'	γ"

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Table II: Switching sequence corresponding to three-steps operation for each inverter

	region ①					region ②						region ③				
H duty cycles	γ_H			μ_H	λ_H	μ_H		γ_H		λ_H		μ_H			λ_H	γ_H
$\bar{v}_H$	0			$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$		0		$\bar{v}_\beta$		$\bar{v}_\alpha$			$\bar{v}_\beta$	0
output vectors	$\bar{v}_\alpha$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$	$2\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$
$\bar{v}_L$	$\bar{v}_\alpha$	$\bar{v}_\beta$	0			0	$\bar{v}_\beta$		$\bar{v}_\alpha$		0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$		
L duty cycles	μ_L	λ_L	γ_L			$\leftarrow\gamma_L$	λ_L		μ_L		$\gamma_L\rightarrow$	λ_L	γ_L	μ_L		
sub-int.	μ"	λ"	γ	μ'	λ'	γ'	μ'	λ"	γ"	μ"	λ'	λ'	γ'	μ	λ"	γ"

$$\begin{cases} \mu' = \mu_H - \gamma' \\ \mu'' = \lambda_H - \gamma_L + \gamma' \\ \lambda' = \gamma_L - \gamma' \\ \lambda'' = \lambda_L - \mu_H + \gamma' \\ \gamma'' = \mu_L + \gamma_L - \lambda_H - \gamma' \end{cases} . \tag{15}$$

Introducing the condition that all intervals must be not negative, $\mu', \mu'', \lambda', \lambda'', \gamma', \gamma'' \geq 0$, the admissible range of parameter γ' is determined. By choosing a value for γ' inside this range, the values of the other sub-intervals are determined by (15). In particular, it can be shown that, by selecting a proper value for γ', it is always possible to null one of the six sub-intervals. In this way the six-step commutation sequence collapses in five steps, as it happens in regions ① and ③.
Once all the sub-intervals are determined, they can be grouped in the switching sequence shown in Tab. II. In this way, for each inverter, a traditional three-step commutation within the switching period is obtained, involving active and null vectors $\bar{v}_\alpha, \bar{v}_\beta$, 0.

6. Implementation of the switching sequence and results

The proposed switching techniques have been numerically implemented in the Simulink environment of Matlab by using appropriate S-functions. In particular, the typical discretizations caused by a realistic digital control system have been taken into account. A simplified ideal model has been considered for power switches, without additional dead times. The tests have been carried out considering the same dc voltage for the dc sources: E = 100 V, and sinusoidal balanced reference output voltages (f = 50 Hz). In order to emphasize the switching actions, a large switching period has been adopted: T_S = 500 μs (f_S = 2 kHz).
The voltage waveforms generated by the two inverters are shown in Figs. 10 and 11, from top to bottom: (1) line-to-line voltage of inverter H (v_{12H}), (2) line-to-line voltage of inverter L (v_{12L}), and (3) load phase voltage (v_1). The solid blue lines represent the instantaneous values, whereas the dotted green lines represent their moving average over a switching period.
It can be noted that the line-to-line voltages are distributed on three levels (0, ±E), as expected for traditional three-phase inverters, whereas the output phase voltage is distributed on nine levels (0, ±1/3E, ±2/3E, ±E, ±4/3E), as expected for a multilevel converter with 6 switches and according to

$$v_1 = \frac{v_{12H} - v_{31H}}{3} - \frac{v_{12L} - v_{31L}}{3} \tag{16}$$

Fig. 10(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, m = 1 ($v = 2/\sqrt{3}\ E$), and k = 1/2. In this case, the two inverters generate the same voltages and then supply the same power.

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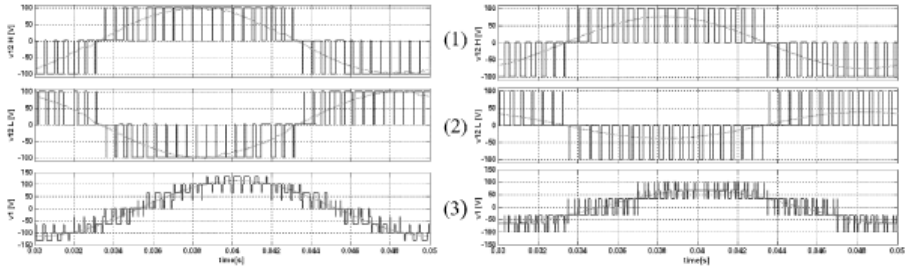
Fig. 10(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, $v = 2/3\ E$ ($m = 1/\sqrt{3}$), and $k = 2/3$. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being $k = 2/3$, the voltages and the power generated by inverter H are double with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that the output voltage is distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 4.

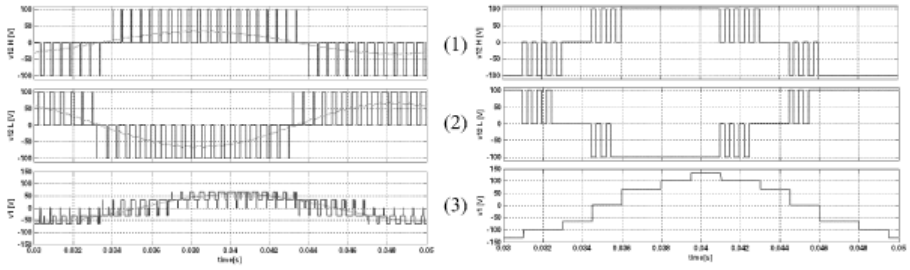
Fig. 11(a) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, $v = 1/\sqrt{3}\ E$ ($m = 1/2$), and $k = 1/3$. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio $k = 1/3$, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

Fig. 11(b) shows the waveforms corresponding to the twelve-step behavior of the multilevel converter, with a power ratio $k = 1/2$. In this case, only the output main vectors $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and $\bar{v}_\alpha + \bar{v}_\beta$ are involved; each vector is applied for a time interval equal to 1/12 of the fundamental period, and the output phase voltage is distributed on seven levels. In particular, the output vector $\bar{v}_\alpha + \bar{v}_\beta$ is obtained by combining $\bar{v}_\alpha, \bar{v}_\beta$ or $\bar{v}_\beta, \bar{v}_\alpha$, whereas the vectors $2\bar{v}_\alpha$ and $2\bar{v}_\beta$ correspond to the applications of $\bar{v}_\alpha$ and $\bar{v}_\beta$ for each inverter, respectively. In this way, the commutations of the inverters allow the power sharing within each switching period, while the output voltage behaves in the twelve-step mode.



(a) $\boldsymbol{m = 1}$ ($v = 2/\sqrt{3}\ E$), $\boldsymbol{k = 1/2}$ ($1-k = 1/2$) (b) $\boldsymbol{m = 1/\sqrt{3}}$ ($v = 2/3\ E$), $\boldsymbol{k = 2/3}$ ($1-k = 1/3$)

Fig. 10: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).



(a) $\boldsymbol{m = 1/2}$ ($v = 1/\sqrt{3}\ E$), $\boldsymbol{k = 1/3}$ ($1-k = 2/3$) (b) **twelve-step**, $\boldsymbol{k = 1/2}$ ($1-k = 1/2$)

Fig. 11: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).

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7. Conclusion

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding three-phase open-end winding loads has been considered in this paper. This scheme has the advantages of avoiding homopolar components and of maximizing the output voltage without additional circuitry. The paper has been focused on the development of a modulation strategy able to regulate the power sharing between the dc sources. It has been shown that the operation with balanced powers between the two inverters is always achievable within the switching cycle with correct multilevel voltage generation. Switching tables for each inverter have been proposed and the limits of the power ratio as function of the modulation index have been determined. The multilevel converter has been numerically implemented by the Simulink environment of Matlab. The simulation results confirm the effectiveness of the proposed switching strategies.

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Appendix 3

Double Inverter as a Multilevel Converter: Circuit Topology, Modulation Strategies and Applications

Double Inverter as a Multilevel Converter: Circuit Topology, Modulation Strategies and Applications

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Abstract— **A way to achieve a multilevel converter using two standard three-phase two-level inverters is presented in this paper. In order to obtain the typical multilevel voltage waveforms it is necessary to synchronize the commutations of the two inverters by a proper modulation strategy. Two modulation strategies are presented: the first one allows only generating the characteristic multilevel line-to-line voltages; the second one allows controlling the power flows from the two inverters too. The proposed converter topology can be applied in the automotive and naval fields.**

Index Terms— **Converters, Multilevel systems. Road vehicle propulsion.**

I. Introduction

MULTILEVEL converters have been introduced in high-power applications such as utility and large motor drive systems. The desired output voltage waveform is synthesized from the multiple voltage levels with lower distortion, lower switching frequency, higher efficiency, and lower voltage device ratings. There are three major multilevel topologies: cascaded, diode clamped, and capacitor clamped [1]. Usually, all these topologies require more complex power circuitry and more complex modulation strategies with respect to traditional three-phase inverters.

Multilevel inverters were initially proposed for high voltage applications to lower the voltage rating of the power switches in order to design feasible converters. Nowadays, many multilevel applications can be found in low voltage systems, in the place of standard three-phase inverters, with the aim of reducing waveform distortions and costs. As in example, in battery powered electric vehicles the standard solution for the traction system is given by a two-level inverter feeding a three phase motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V). With this solution the practical feasibility of a high power ac drive (>20 kW) is limited mainly by the high cost of the semiconductor power switches of the inverter due to the resulting high current rating.

The high cost together with the circuit complexity due to the parallel connection of the power switches can prevent the realization of standard three-phase drives for the traction system of heavy electric vehicles, such as buses, industrial truck, etc…

A viable solution introduced to overcome this problem is given by the use of a six-phase machine supplied by a six-phase inverter [2]-[5]. This solution allows sizing the power switches at half the rated current of an equivalent three-phase scheme, but requires the realization of a six-phase machine.

Another solution for high power electrical drives is the use of a multilevel inverter, which can be realized with semiconductor devices having lower voltage rating. The typical structure of such a system was introduced in [6] and, nowadays, it is widely used to drive three-phase electrical machine with high supply voltages. Several topologies of multilevel converters have been also presented for low voltage applications [7]. Among these, the cascaded converter can be conveniently used with a battery supply system, because it is relatively easy to split the supply in several electrically separated sources.

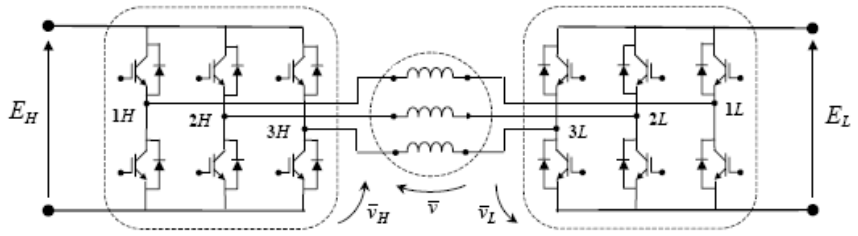


Fig.1: Multilevel converter for six-wire applications composed of two traditional two-level inverters.

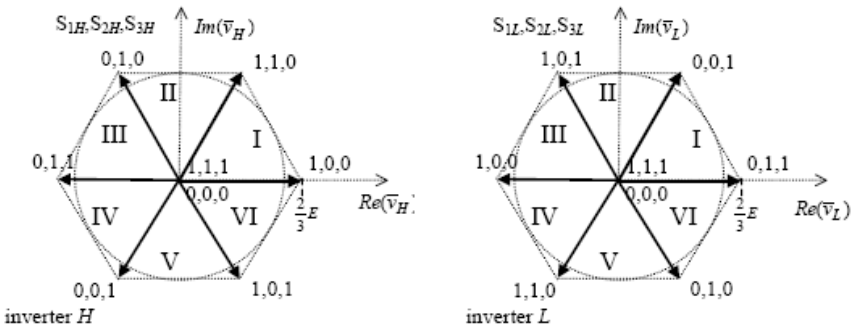


Fig.2: Switch configurations, sectors, and corresponding voltage vectors for inverters *H* and *L*.

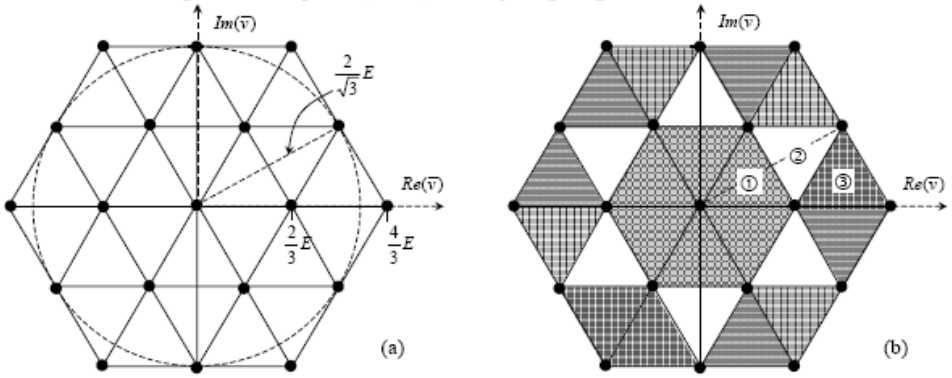


Fig. 3: (a) Output voltage vectors generated by the dual, two-level inverter. (b) Highlight of the triangles in the three different regions ①, ②, and ③.

In this paper a multilevel converter composed of a dual two-level inverter feeding open-end, three-phase ac motor [8]-[10] is considered. The scheme of the multilevel converter is shown in Fig.1. This scheme is based on the use of two insulated supplies, each one feeding a standard, three-phase two-level inverter. A three-phase, six-wires load is connected across the six output terminals of the inverters. The two separate dc sources can be easily obtained on board of an electric vehicle by splitting the batteries in two separate banks.

This solution should be preferred to other multilevel configurations because of some advantages: no generation of common mode (zero sequence) currents on the motor winding, best dc bus voltage utilization, use of two standard three-phase, two-level inverters.

New switching techniques, based on a proper application of the space vector modulation (SVM), are presented in the paper. The main feature of these techniques is the capability to regulate the load power sharing between the two dc sources. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks.

Furthermore, the dual inverter topology is a high reliability solution. In case of fault in one inverter, it must be short-circuited at the output terminals, and the drive can be operated using the other one as a standard three-phase two-level inverter. This possibility allows the operation of the motor at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed).

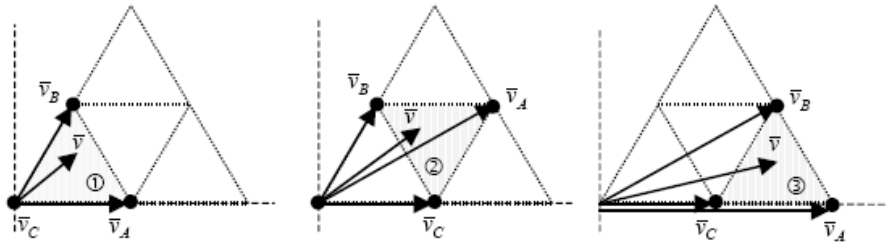


Fig.4: Voltage vectors used for generating the output voltage in the three regions.

II. MULTILEVEL MODULATION STRATEGY

With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector $\overline{v}$ is given by the contribution of the voltage vectors $\overline{v}_H$ and $\overline{v}_L$, generated by inverter H and inverter L, respectively,

$$\overline{v} = \overline{v}_H + \overline{v}_L \tag{1}$$

The voltages $\overline{v}_H$ and $\overline{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to

$$\overline{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\,e^{j\frac{2}{3}\pi} + S_{3H}\,e^{j\frac{4}{3}\pi}\right)$$
$$\overline{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\,e^{j\frac{2}{3}\pi} + S_{3L}\,e^{j\frac{4}{3}\pi}\right) \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs. A space vector representation of $\overline{v}_H$ and $\overline{v}_L$ is given in Fig. 2.

The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 3(a). By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 E. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2E/\sqrt{3}$ (i.e., the radius of the inscribed circle).

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 3(b), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted).

In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\overline{v}$ is synthesized by using the vectors $\overline{v}_A, \overline{v}_B, \overline{v}_C$, as represented in Fig. 4 for the three types of triangles.

Considering the standard SVM technique, $\overline{v}$ is obtained as

$$\overline{v} = \mu\,\overline{v}_A + \lambda\,\overline{v}_B + \gamma\,\overline{v}_C\,, \tag{3}$$

where the duty cycle μ, λ, γ can be determined as

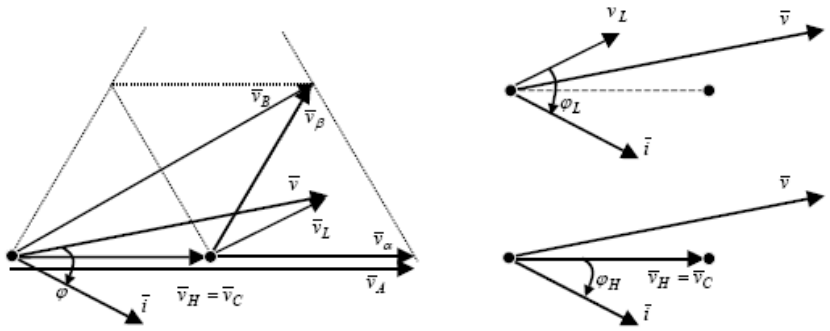


Fig.5: Vector composition of the output voltage combining six-step mode and SVM mode for the two inverters.

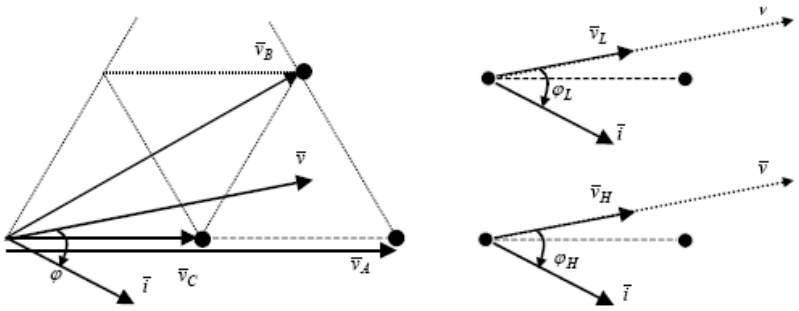


Fig.6: Vector composition of the output voltage with balanced power between the inverters ($k = 0.5$).

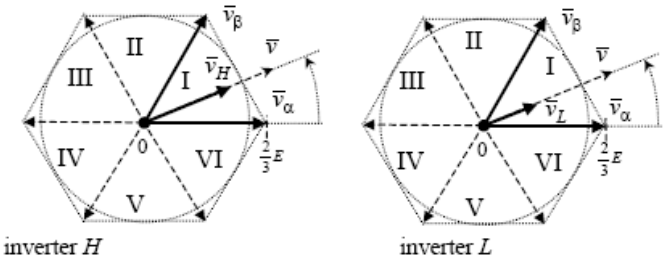


Fig.7: Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

$$\begin{cases} \mu = \dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \\ \lambda = -\dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_A-\bar{v}_C)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \\ \gamma = 1-(\mu+\lambda) = 1-\dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_A)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \end{cases} \quad (4)$$

A simple modulation strategy consists of modulating one inverter in the six-step mode, i.e., $\bar{v}_H = \bar{v}_C$, and the other inverter in the SVM mode for generating the residual output voltage $\bar{v}_L = \bar{v} - \bar{v}_C$. As an example, Fig. 5 shows the vector composition considering $\bar{v}$ laying in the outer triangle (region ③).

This simple modulation technique leads to a power unbalance between the two inverters. In fact, the inverter voltages $(\bar{v}_H, \bar{v}_L)$ have different magnitude and different phase angle with respect to the output current $\bar{i}$ (the same for both), as shown in Fig. 5.

The problem of balancing the power between the two dc sources could be solved in a simple way, by exchanging the role of the inverter operating in the six-step mode with the one operating in the SVM mode. The commutation can be actuated during a switching period, a triangle change, or a fundamental period. This solution is satisfactory for exactly balancing the powers, but does not allow any different regulation of the power sharing.

III. Regulation of the Power Sharing

A novel modulation technique, able to regulate the power sharing between the two dc sources, is presented in this section. The balanced operation can be considered a particular case.

Introducing the power ratio k, the output power p (average value over a switching period) can be shared between the dc sources (H and L) according to

$$p = \frac{3}{2}\bar{v}\cdot\bar{i} = p_H + p_L$$
$$\Downarrow \quad (5)$$
$$\begin{cases} p_H = \dfrac{3}{2}\bar{v}_H\cdot\bar{i} = k\cdot p \\ p_L = \dfrac{3}{2}\bar{v}_L\cdot\bar{i} = (1-k)\cdot p \end{cases}$$

Assuming the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ in phase with the output voltage vector $\bar{v}$, (5) leads to

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \end{cases} \quad (6)$$

Fig. 6 shows the particular case with $k = 0.5$ corresponding

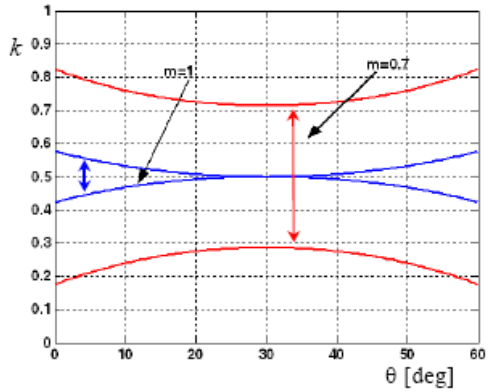


Fig. 8: Possible values of the power ratio k for modulation indexes $m = 1$ (blu) and $m = 0.7$ (red).

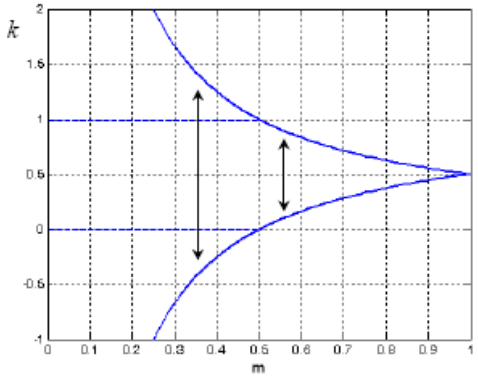


Fig. 9: Limits of the power ratio k as function of the modulation index m.

to $\overline{v}_H = \overline{v}_L = 1/2\,\overline{v}$, i.e., balanced power for the dc sources. In order to synthesize an output vector $\overline{v}$, the two inverters must generate the corresponding fraction of $\overline{v}$ by applying only their active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector. Being $\overline{v}_H$ and $\overline{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\overline{v}_\alpha, \overline{v}_\beta$, as shown in Fig. 7.

The duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector, respectively, for inverter *H*. The duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector, respectively, for inverter *L*. In this way, the voltage generated by the two inverters are

$$\begin{cases} \overline{v}_H = \mu_H\,\overline{v}_\alpha + \lambda_H\,\overline{v}_\beta \\ \overline{v}_L = \mu_L\,\overline{v}_\alpha + \lambda_L\,\overline{v}_\beta \end{cases} . \tag{7}$$

By using standard SVM equations, the duty-cycles of inverters *H* and *L* are given by

$$\begin{cases} \mu_H = \dfrac{\overline{v}_H \cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \\ \lambda_H = -\dfrac{\overline{v}_H \cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \\ \gamma_H = 1-(\mu_H+\lambda_H) = 1-\dfrac{\overline{v}_H \cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \end{cases}$$

and

$$\begin{cases} \mu_L = \dfrac{\overline{v}_L \cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \\ \lambda_L = -\dfrac{\overline{v}_L \cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \\ \gamma_L = 1-(\mu_L+\lambda_L) = 1-\dfrac{\overline{v}_L \cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \end{cases} . \tag{8}$$

IV. Determination of the Operating Limits

The constrains of the duty-cycles expressed by (8) are

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases} \quad \text{and} \quad \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases} . \tag{9}$$

These constrains introduce a limit in the range of variation of the power ratio *k*. In particular, the range of variation of *k* can be evaluated as a function of the desired output vector $\overline{v}$. Introducing in (9) the expressions (8) of duty cycles, and representing $\overline{v}_H$ and $\overline{v}_L$ in terms of *k* by (6), leads to

$$\begin{cases} \dfrac{k\overline{v} \cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ -\dfrac{k\overline{v} \cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ \dfrac{k\overline{v} \cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \leq 1 \end{cases}$$

and

$$\begin{cases} \dfrac{(1-k)\overline{v} \cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ -\dfrac{(1-k)\overline{v} \cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ \dfrac{(1-k)\overline{v} \cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \leq 1 \end{cases} . \tag{10}$$

The solution of (10) can be found in each one of the six sectors where $\overline{v}_H$ and $\overline{v}_L$ can be located.

If the output voltage vector is written as $\overline{v} = Ve^{j\vartheta}$, the modulation index *m* can be defined as

$$m = \frac{V}{\frac{2}{\sqrt{3}}E},\ 0 \leq m \leq 1 \text{ for sinusoidal output voltages.} \tag{11}$$

Then, with reference to sector I ($0 \leq \vartheta \leq \frac{\pi}{3}$), the solution of (10) is given by

$$\begin{cases} k \leq \dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \\ k \geq 1-\dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \end{cases}$$

$$\Downarrow \tag{12}$$

$$\frac{1}{2} - a \leq k \leq \frac{1}{2} + a$$

being $a = \dfrac{1-m\,cos(\pi/6-\vartheta)}{2m\,cos(\pi/6-\vartheta)}$.

Eq. 12 gives the possible values of *k* as a function of the modulation index *m* and the output voltage phase angle ϑ. It can be noted that for any modulation index, the most stringent condition for *k* is given in the middle of the sector, i.e. for $\vartheta = \pi/6$. Fig. 8 represents the boundaries of *k* as a function of the phase angle ϑ for *m* = 1 and *m*=2/3.

Similar considerations can be made for the other sectors (II ÷ VI).

In most applications is required to share the output power between the dc sources in equal parts. This means that *k* must be fixed to 0.5 during the whole fundamental period, $0 \leq \vartheta \leq 2\pi$.

If the maximum output voltage is required (*m* = 1), there is no possibility to regulate the power sharing between the dc sources. In this case only the value $k = 0.5$ is admissible, as

Table I: Resulting switching sequence for multilevel operations

	region ①					region ②						region ③				
output vectors	$\bar{v}_A=\bar{v}_\alpha$		$\bar{v}_B=\bar{v}_\beta$		$\bar{v}_C=0$	$\bar{v}_A=\bar{v}_\alpha+\bar{v}_\beta$		$\bar{v}_B=\bar{v}_\beta$		$\bar{v}_C=\bar{v}_\alpha$		$\bar{v}_A=2\bar{v}_\alpha$	$\bar{v}_B=\bar{v}_\alpha+\bar{v}_\beta$		$\bar{v}_C=0$	
$\bar{v}_H$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0
$\bar{v}_L$	0	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$
duty cycles	μ'	μ''	λ'	λ''	γ	μ'	μ''	λ'	λ''	γ'	γ''	μ	λ'	λ''	γ'	γ''

Table II: Switching sequence corresponding to three-steps operation for each inverter

	region ①					region ②						region ③				
H duty cycles	γ_H			μ_H	λ_H	μ_H		γ_H		λ_H		μ_H			λ_H	γ_H
$\bar{v}_H$	0			$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$		0		$\bar{v}_\beta$		$\bar{v}_\alpha$			$\bar{v}_\beta$	0
output vectors	$\bar{v}_\alpha$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$	$2\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$
$\bar{v}_L$	$\bar{v}_\alpha$	$\bar{v}_\beta$	0			0	$\bar{v}_\beta$		$\bar{v}_\alpha$		0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$		
L duty cycles	μ_L	λ_L	γ_L			$\leftarrow\gamma_L$	λ_L		μ_L		$\gamma_L\rightarrow$	λ_L	γ_L	μ_L		

sub-int.	μ''	λ''	γ	μ'	λ'	γ'	μ'	λ''	γ''	μ''	λ'	λ'	γ'	μ	λ''	γ''

shown in Fig. 8.

For values of the modulation index lower than 1, the parameter k can be changed, under the limits imposed by (12). Fig. 9 shows the upper and lower limits of k with reference to sinusoidal output voltages as a function of the modulation index m. It can be noted that for $m < 0.5$ the power ratio k can be greater than unity and lower than zero. It means that an amount of power can be transferred from a dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase oppositions, as shown by (5) and (6). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources. In this paper only the range $0 \le k \le 1$ is discussed.

For $m \le 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if k is set to 0 all the load power is supplied by inverter L, whereas if k is set to 1 all the load power is supplied by inverter H. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only.

V. Determination of the Switching Sequence

Once the limits for k has been defined, and the required inverter voltages $\bar{v}_H$ and $\bar{v}_L$ have been determined, the duty-cycles $\mu_H, \lambda_H, \gamma_H$ and $\mu_L, \lambda_L, \gamma_L$ can be calculated by (8). As stated above, for achieving a correct multilevel operation, the three vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, adjacent to the desired output voltage vector $\bar{v}$, must be generated by properly combining active vectors $(\bar{v}_\alpha, \bar{v}_\beta)$ and null vector of the two inverters. For regions ①, ②, and ③ shown in Figs. 3 and 4, three different vector compositions are defined, according to the following equations

$$\underline{\text{Region ①}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + 0 \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = 0 + 0 \end{cases} \text{(a)} \qquad \underline{\text{Region ②}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \text{(b)} \qquad \underline{\text{Region ③}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \text{(c)} \tag{13}$$

On the basis of (13), the duty-cycles for the vectors $\bar{v}_\alpha, \bar{v}_\beta$ and 0 of inverters H and L, can be related to the duty-cycles μ, λ, γ of the output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$ calculated in (4). It can be noted that $\bar{v}_\alpha, \bar{v}_\beta$ and 0 are the same vectors for the two inverters. Then, when the output vector $\bar{v}_\alpha$ must be applied, the application time of $\bar{v}_\alpha$ can be subdivided in two sub-intervals. In the first time interval, inverter H generates $\bar{v}_\alpha$ and inverter L generates 0. In the second time interval, inverter L generates $\bar{v}_\alpha$ and inverter H generates 0. The same procedures can be adopted for generating the output vectors $\bar{v}_\beta$ and $\bar{v}_\alpha + \bar{v}_\beta$. For the other possible output vectors, $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and 0, the subdivision is trivial. The resulting switching

sequence inside a switching period is represented in Tab. I with reference to all the three regions ①, ②, and ③.

The sub-intervals introduced in Tab. I can be determined for the three different regions on the basis of main duty-cycles μ, λ, γ and duty-cycles $\mu_H, \lambda_H, \gamma_H$, $\mu_L, \lambda_L, \gamma_L$ of the two inverters, as follows

$$\begin{array}{lll} \text{Region ①} & \text{Region ②} & \text{Region ③} \\ \begin{cases} \mu' = \mu_H \\ \mu'' = \mu_L \\ \lambda' = \lambda_H \\ \lambda'' = \lambda_L \\ \gamma \text{ is known} \\ - \end{cases} & \begin{cases} \mu'+\gamma' = \mu_H \\ \mu''+\lambda' = \lambda_H \\ \lambda''+\gamma'' = \gamma_H \\ \mu''+\gamma'' = \mu_L \\ \mu'+\lambda'' = \lambda_L \\ \lambda'+\gamma' = \gamma_L \end{cases} & \begin{cases} \mu \text{ is known} \\ - \\ \lambda' = \lambda_L \\ \lambda'' = \lambda_H \\ \gamma' = \gamma_L \\ \gamma'' = \gamma_H \end{cases} \\ \text{(a)} & \text{(b)} & \text{(c)} \end{array} \qquad (14)$$

It can be noted that for regions ① and ③ the sub-intervals are five, whereas for region ② the sub-intervals are six and they can be determined by solving a system of six equations. Only five of these equations are linear independent. In fact, the sum of the first three equations in (14b) gives the same result than the sum of the last three equations, as expressed by (8). Then, the equation system (14b) can be solved in parametric form. Assuming γ' as parameter, the sub-intervals result

$$\begin{cases} \mu' = \mu_H - \gamma' \\ \mu'' = \lambda_H - \gamma_L + \gamma' \\ \lambda' = \gamma_L - \gamma' \\ \lambda'' = \lambda_L - \mu_H + \gamma' \\ \gamma'' = \mu_L + \gamma_L - \lambda_H - \gamma' \end{cases} . \qquad (15)$$

Introducing the condition that all intervals must be not negative, $\mu', \mu'', \lambda', \lambda'', \gamma', \gamma'' \geq 0$, the admissible range of parameter γ' is determined. By choosing a value for γ' inside this range, the values of the other sub-intervals are determined by (15). In particular, it can be shown that, by selecting a proper value for γ', it is always possible to null one of the six sub-intervals. In this way the six-step commutation sequence collapses in five steps, as it happens in regions ① and ③.

Once all the sub-intervals are determined, they can be grouped in the switching sequence shown in Tab. II. In this way, for each inverter, a traditional three-step commutation within the switching period is obtained, involving active and null vectors $\overline{v}_\alpha, \overline{v}_\beta$, 0.

VI. Implementation of the Switching Sequence and Results

The proposed switching techniques have been numerically implemented in the Simulink environment of Matlab by using appropriate S-functions. In particular, the typical discretizations caused by a realistic digital control system have been taken into account. A simplified ideal model has been considered for power switches, without additional dead times. The tests have been carried out considering the same dc voltage for the dc sources: E = 100 V, and sinusoidal balanced reference output voltages (f = 50 Hz). In order to emphasize the switching actions, a large switching period has been adopted: TS = 500 μs (fS = 2 kHz).

The voltage waveforms generated by the two inverters are shown in Figs. 10 and 11, from top to bottom: (1) line-to-line voltage of inverter H (v_{12H}), (2) line-to-line voltage of inverter L (v_{12L}), and (3) load phase voltage (v1). The solid blue lines represent the instantaneous values, whereas the dotted green lines represent their moving average over a switching period.

It can be noted that the line-to-line voltages are distributed on three levels (0, ±E), as expected for traditional three-phase inverters, whereas the output phase voltage is distributed on nine levels (0, ±1/3E, ±2/3E, ±E, ±4/3E), as expected for a multilevel converter with 6 switches and according to

$$v_1 = \frac{v_{12H} - v_{31H}}{3} - \frac{v_{12L} - v_{31L}}{3} \qquad (16)$$

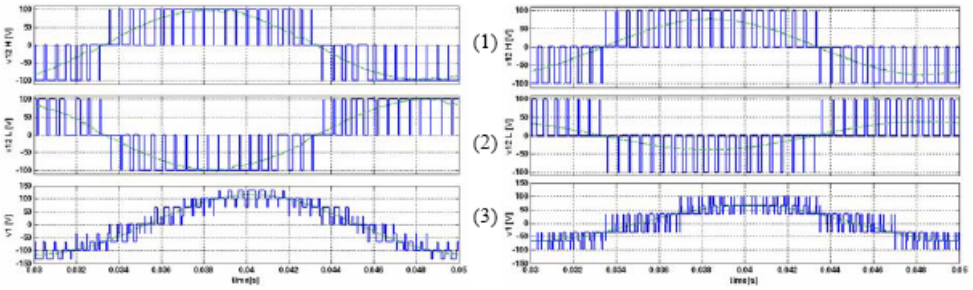
Fig. 10(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, m = 1 (v = 2/√3 E), and k = 1/2. In this case, the two inverters generate the same voltages and then supply the same power.

Fig. 10(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, v = 2/3 E (m = 1/√3), and k = 2/3. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being k = 2/3, the voltages and the power generated by inverter H are double with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that the output voltage is distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 4.

Fig. 11(a) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, v = 1/√3 E (m = 1/2), and k = 1/3. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio k = 1/3, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

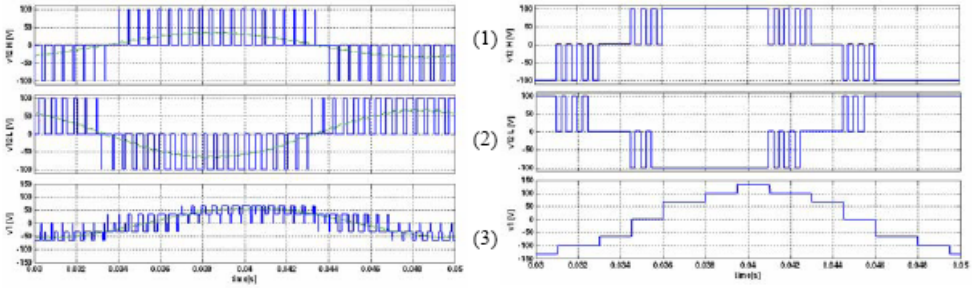
Fig. 11(b) shows the waveforms corresponding to the twelve-step behavior of the multilevel converter, with a power ratio k = 1/2. In this case, only the output main vectors $2\overline{v}_\alpha$, $2\overline{v}_\beta$, and $\overline{v}_\alpha + \overline{v}_\beta$ are involved; each vector is applied for a time interval equal to 1/12 of the fundamental period, and the output phase voltage is distributed on seven levels. In particular, the output vector $\overline{v}_\alpha + \overline{v}_\beta$ is obtained by combining $\overline{v}_\alpha, \overline{v}_\beta$ or $\overline{v}_\beta, \overline{v}_\alpha$, whereas the vectors $2\overline{v}_\alpha$ and $2\overline{v}_\beta$ correspond to the applications of $\overline{v}_\alpha$ and $\overline{v}_\beta$ for each inverter, respectively. In this way, the commutations of the inverters allow the power sharing within each switching period, while the output voltage behaves in the twelve-step mode.



(a) $m = 1$ ($v = 2/\sqrt{3}\,E$), $k = 1/2$ ($1-k = 1/2$)

(b) $m = 1/\sqrt{3}$ ($v = 2/3\,E$), $k = 2/3$ ($1-k = 1/3$)

Fig. 10: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).



(a) $m = 1/2$ ($v = 1/\sqrt{3}\,E$), $k = 1/3$ ($1-k = 2/3$)

(b) twelve-step, $k = 1/2$ ($1-k = 1/2$)

Fig. 11: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).

VII. APPLICATIONS

Multilevel inverters have many advantages with respect of standard three-phase converters, such as lower output THDs and the capability to handle higher voltages. Nevertheless, multilevel converters require a greater number of semiconductor devices and some constrains in the sources. Diode-clamped and flying-capacitors topologies require a subdivision of the dc bus to create the voltage levels; instead cascaded topologies need insulated sources. In some cases there is a natural agreement between the application and the multilevel converter (i.e. photovoltaic and cascaded converter). In automotive field, the energy source can be either a batteries bank or an endothermic engine or both (in hybrid vehicles). In these cases it is useful to employ the multilevel topology proposed in this paper because the necessary insulated dc sources are easy to obtain. In case of battery bank, it is simple to split it in two parts and using them to feed the two inverters. In this way it, is possible to employ the double inverter system easily and using it as a multilevel converter through one of the modulation described in this paper. Furthermore, an equal discharge of the two battery banks is achieved by a proper control of k index.

Similarly, another application for the proposed system is the propulsion in fishing-boat because these ships have two kind of cruising. When the nets are in the water, it is necessary to have high torque at low speed (higher power condition); when fishers need to move high speed and low torque are required (lower power condition). An endothermic engine with two electrical generators shrunk on can be employed to feed the two inverters. In higher power condition both the two inverters are fed and the converter is controlled by one of the multilevel modulation; in lower power condition only one inverter is fed and the other one has its outputs short-circuited [11].

VIII. CONCLUSION

The multilevel converter topology presented in this paper is composed by two standard three-level inverters widely commercialized. This means a lower cost than a diode-clamped or flying-capacitor equivalent solution. In case of fault, it is possible to short-circuit the outputs of the broken inverter so to create a star connection in the load and feed it

through the other inverter as a standard three-phase load. Furthermore, it is easiest to substitute the broken parts due to their high availability.

The two modulation strategies presented in the paper let the inverter system properly work: the voltage waveforms are those typical for multilevel inverters, as shown by simulation results. Moreover it is possible to regulate the power supplied from each of the two inverters, making the system suitable for battery applications. Some possible applications in the automotive and naval fields were presented.

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Appendix 4

Experimental Investigation of a Three-Phase Multi-Level Converter Based on Two Standard Voltage Source Inverters with Insulated DC Supplies

Experimental investigation of a three phase multilevel converter based on two standard voltage source inverters with insulated dc supplies

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Abstract

An experimental investigation of a multilevel converter topology feeding three-phase open-end winding loads is proposed in this paper. The hardware scheme is based on two insulated dc supplies, each one feeding a standard two-level, three-phase inverter. A three-phase, six wires load is connected across the output terminals. A new modulation technique is considered, based on the space vector approach, able to regulate the sharing of the output power between the two dc sources within each switching cycle. The performances of the multilevel converter are discussed on the basis of a complete set of experimental tests.

1. Introduction

Multilevel converters represent a viable solution to overcame the voltage limits of power switching converters. They are able to generate output voltage waveforms consisting in a large number of steps, limiting the stress on the switching devices. In fact, higher voltage levels are synthesized from voltage sources with lower levels, with the additional benefit of a reduced harmonic distortion and dv/dt in the output voltage. These features have made multilevel converter suitable for application in the large and medium induction motor drives.

Several topologies of multilevel converters have been presented for low voltage applications [1]. Among these, the cascaded converter can be conveniently used with a battery supply system, because it is relatively easy to split the supply in several electrically separated sources.

In this paper a complete set of experimental tests on a multilevel converter composed by two standard two-level inverters [2]-[4] are given. This converter is able to supply and drive standard three-phase ac motors, in the open-end winding configuration. The scheme of the multilevel converter is shown in Fig. 1. This scheme is based on the use of insulated supplies, such as two banks of standard lead acid batteries. The three-phase six-wires load is connected across the six output terminals of the inverters. This solution should be preferred to other multilevel configurations because of some advantages: no generation of common mode (zero sequence) currents on the motor winding, best dc bus voltage utilization, use of two standard three-phase, two-level inverters. Furthermore, the dual inverter topology is a high reliability solution. In case of fault in one inverter, its output terminals can be short-circuited, and the drive operates using the other one as a standard three-phase two-level inverter. This possibility allows the operation of the motor at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed).

New switching techniques, based on a proper application of the space vector modulation (SVM), are discussed in the paper. The main feature of these techniques is the capability to regulate the load power sharing between the two dc sources within the switching period [5]. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks.

The capability of the multilevel converter are discussed on the basis of a complete set of experimental tests carried out on both a reduced size and a full power prototype.

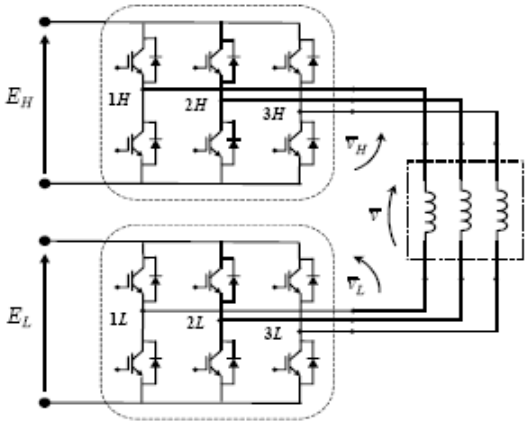


Fig. 1. Electric scheme of the multilevel converter.

2. Multilevel modulation strategy

With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector $\overline{v}$ of the multilevel converter is given by the contribution of the voltage vectors $\overline{v}_H$ and $\overline{v}_L$, generated by inverter *H* and inverter *L*, respectively:

$$\overline{v} = \overline{v}_H + \overline{v}_L \ . \qquad (1)$$

The voltages $\overline{v}_H$ and $\overline{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to:

$$\overline{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\, e^{j\frac{2}{3}\pi} + S_{3H}\, e^{j\frac{4}{3}\pi}\right), \text{ and}$$

$$\overline{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\, e^{j\frac{2}{3}\pi} + S_{3L}\, e^{j\frac{4}{3}\pi}\right), \qquad (2)$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs.

The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 2. By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 *E*. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2/\sqrt{3}\,E$ (i.e., the radius of the inscribed circle).

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 3(a), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted). In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\overline{v}$ is synthesized by using the vectors $\overline{V}_A, \overline{V}_B, \overline{V}_C$, as represented in Fig. 3 (b) for the three types of triangles.

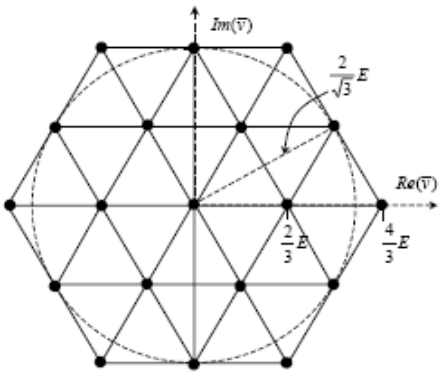


Fig. 2. Output voltage vectors of the multilevel converter.

Considering the standard SVM technique, $\overline{v}$ is obtained on the basis of the duty cycles μ, λ, γ :

$$\overline{v} = \mu\,\overline{v}_A + \lambda\,\overline{v}_B + \gamma\,\overline{v}_C \ . \qquad (3)$$

3. Regulation of the Power Sharing

A novel modulation technique, able to share the output power *p* between the two dc sources, is considered in this section. Introducing the power ratio *k* and assuming the inverter voltage vectors $\overline{v}_H$, $\overline{v}_L$ in phase with the output voltage vector $\overline{v}$, leads to the following equations (average values over a switching period):

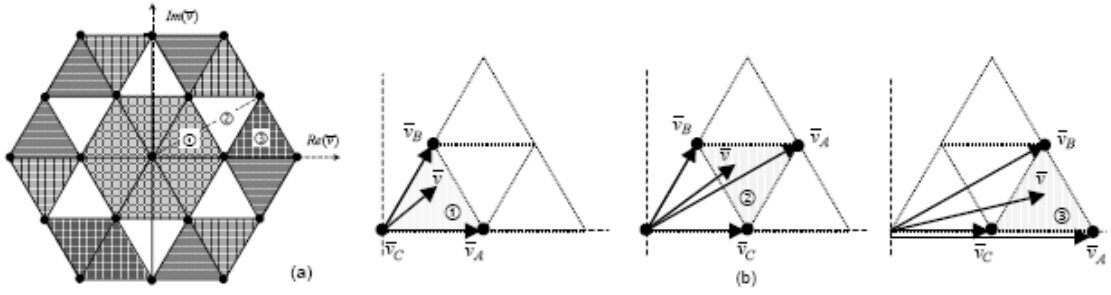


Fig. 3. (a) Highlight of the triangles in the three different regions ①, ②, and ③;
(b) Vector composition to obtain the output voltage in the three different regions.

$$\begin{cases} \overline{v}_H = k\,\overline{v} \\ \overline{v}_L = (1-k)\,\overline{v} \\ p = \dfrac{3}{2}\overline{v}\cdot\overline{i} = p_H + p_L \end{cases} \qquad \begin{cases} p_H = \dfrac{3}{2}\overline{v}_H\cdot\overline{i} = k\cdot p \\ p_L = \dfrac{3}{2}\overline{v}_L\cdot\overline{i} = (1-k)\cdot p \end{cases} \tag{4}$$

In order to synthesize an output vector $\overline{v}$, the two inverters must generate the corresponding fraction of $\overline{v}$ by applying only their active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector. Being $\overline{v}_H$ and $\overline{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\overline{v}_\alpha, \overline{v}_\beta$, as shown in Fig. 4.

The duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector, respectively, for inverter *H*. The duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\overline{v}_\alpha, \overline{v}_\beta$ and null vector, respectively, for inverter *L*. In this way, the voltage generated by the two inverters are:

$$\begin{cases} \overline{v}_H = \mu_H\,\overline{v}_\alpha + \lambda_H\,\overline{v}_\beta \\ \overline{v}_L = \mu_L\,\overline{v}_\alpha + \lambda_L\,\overline{v}_\beta \end{cases}. \tag{5}$$

By using standard SVM equations, the duty-cycles of inverters *H* and *L* are given by:

$$\begin{cases} \mu_H = \dfrac{\overline{v}_H\cdot j\overline{v}_\beta}{\overline{v}_\alpha\cdot j\overline{v}_\beta}\lambda_H = -\dfrac{\overline{v}_H\cdot j\overline{v}_\alpha}{\overline{v}_\alpha\cdot j\overline{v}_\beta} \\ \lambda_H = -\dfrac{\overline{v}_H\cdot j\overline{v}_\alpha}{\overline{v}_\alpha\cdot j\overline{v}_\beta}\ ,\quad \gamma_H = 1-(\mu_H+\lambda_H) \end{cases}, \tag{6}$$

$$\begin{cases} \mu_L = \dfrac{\overline{v}_L\cdot j\overline{v}_\beta}{\overline{v}_\alpha\cdot j\overline{v}_\beta} \\ \lambda_L = -\dfrac{\overline{v}_L\cdot j\overline{v}_\alpha}{\overline{v}_\alpha\cdot j\overline{v}_\beta}\ ,\ \gamma_L = 1-(\mu_L+\lambda_L) \end{cases}. \tag{7}$$

4. Determination of the operating limits

The constrains of the duty-cycles are:

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases} \quad \text{and} \quad \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases}. \tag{8}$$

These constrains introduce a limit in the range of variation of the power ratio *k*. In particular, the range of variation of *k* can be evaluated as a function of the modulation index *m* ($0 \leq m \leq 1$ for sinusoidal output voltages).

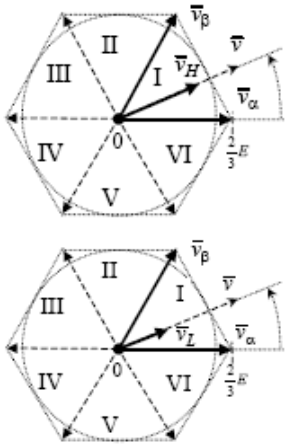


Fig.4. Voltage vectors $\overline{v}_H$ and $\overline{v}_L$ generated by using the same two adjacent active vectors $\overline{v}_\alpha, \overline{v}_\beta$.

Fig. 5 shows the upper and lower limits of *k* with reference to sinusoidal output voltages as a function of the modulation index *m*. It can be noted that for $m < 0.5$ the power ratio *k* could be greater than unity and lower than zero. It means that an amount of power could be transferred from a dc source to the other, and the inverter voltages $\overline{v}_H$ and $\overline{v}_L$ become in phase oppositions, as shown in (4). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources. In this paper only the range $0 \leq k \leq 1$ is discussed. For $m \leq 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if *k* is set to 0 all the load power is supplied by inverter *L*, whereas if *k* is set to 1 all the load power is supplied by inverter *H*. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only.

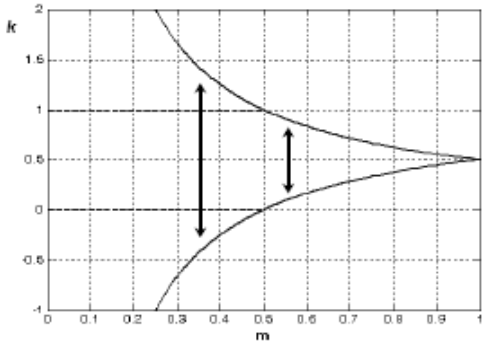


Fig. 5. Limits of the power ratio *k* as function of the modulation index *m*.

6. Numerical simulations

The double inverter configuration has been implemented in the Simulink environment of Matlab by using appropriate S-functions. The simulation results, based on the switching table presented in [5], are shown in Fig. 6.

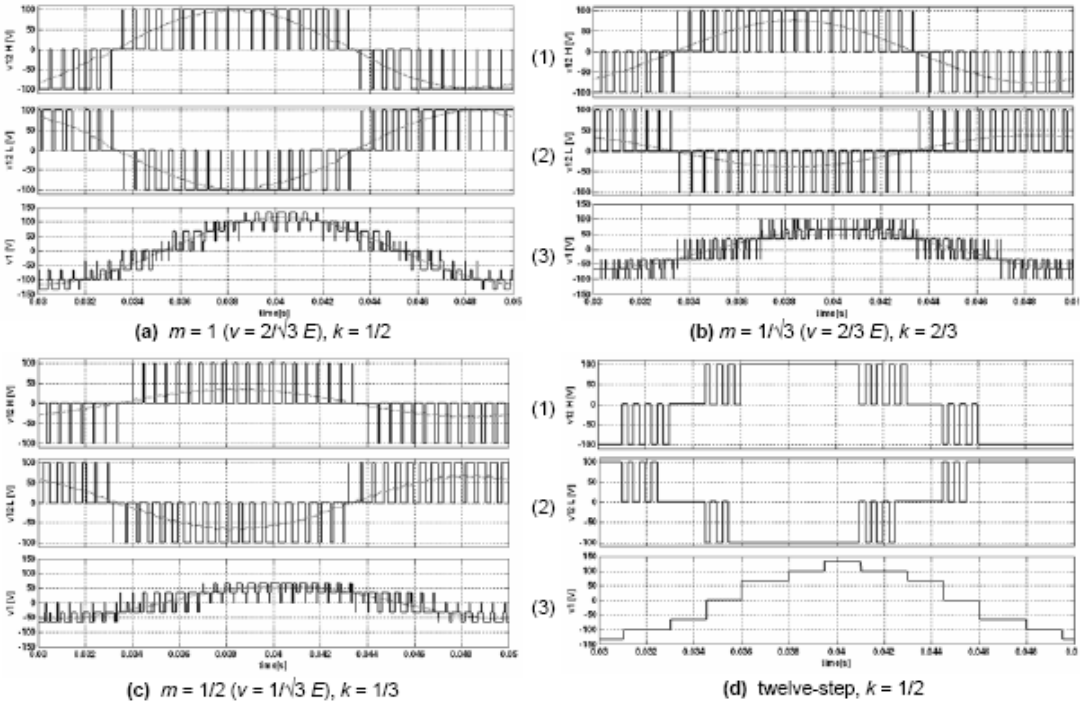
Fig. 6(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, m = 1 (v = 2/√3 E), and k = 1/2. In this case, the two inverters generate the same voltages, i.e., supply the same power. It can be noted that the output phase voltage is distributed on nine levels.

Fig. 6(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, v = 2/3 E (m = 1/√3), and k = 2/3. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being k = 2/3, the voltages and the power generated by inverter H are double with respect to the ones generated by inverter L.

Fig. 6(c) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, v = 1/√3 E (m = 1/2), and k = 1/3. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio k = 1/3, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that the output voltage is always distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 3(b).

Fig. 6(d) shows the waveforms corresponding to the twelve-step behavior of the multilevel converter, with a power ratio k = 1/2. In this case, only the output main vectors $2\overline{v}_\alpha$, $2\overline{v}_\beta$, and $\overline{v}_\alpha + \overline{v}_\beta$ are involved; each vector is applied for a time interval equal to 1/12 of the fundamental period, and the output phase voltage is distributed on seven levels. In particular, the output vector $\overline{v}_\alpha + \overline{v}_\beta$ is obtained by combining $\overline{v}_\alpha, \overline{v}_\beta$ or $\overline{v}_\beta, \overline{v}_\alpha$, whereas the vectors $2\overline{v}_\alpha$ and $2\overline{v}_\beta$ correspond to the applications of $\overline{v}_\alpha$ and $\overline{v}_\beta$ for each inverter, respectively. In this way, the commutations of the inverters allow the power sharing within each switching period, while the output voltage behaves in the twelve-step mode.



(a) m = 1 (v = 2/√3 E), k = 1/2

(b) m = 1/√3 (v = 2/3 E), k = 2/3

(c) m = 1/2 (v = 1/√3 E), k = 1/3

(d) twelve-step, k = 1/2

Fig. 6. Voltage waveforms for different values of m and k: (1) line-to-line voltage generated by inverter H; (2) line-to-line voltage generated by inverter L; (3) load phase voltage (output).

7. Experimental tests

The multilevel inverter has been tested by both a reduced scale prototype and a full size power converter, realized in the Labs of the Dept. of Electrical Engineering in Bologna.
For both converters the control algorithm is based on the switching tables presented in [5]. It has been implemented on a control board based on TMS320F2812® DSP, operating with a clock frequency of 150 MHz, exploiting both its two independent three-phase PWM generators. In this way, no additional control hardware (e.g., FPGA) is necessary beside the DSP for switch commutation management.

Reduced scale converter prototype

The reduced scale system has been realized by using two modular inverters IR-AMS10UP60B® which assemble both power and driver circuits. These components are rated for a dc bus voltage of 450V and a phase current of 10A RMS (25°C). In Fig. 7 is shown a picture of the two power boards. Unfortunately the power and the control grounds are internally connected. Then, to make the required insulation between the two dc sources it has been necessary to introduce photo-couplers.

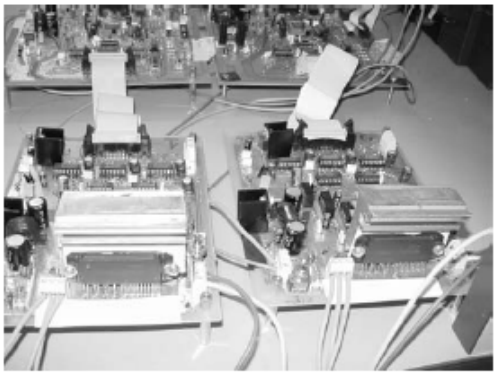


Fig. 7. Picture of the reduced scale converter prototype.

Full size power converter

The power stage of the full size multilevel converter is depicted in Fig. 9. The two 'two-level' inverters have the main data reported in Table I.

Table I. CHARACTERISTICS OF THE POWER INVERTERS

supply system	lead acid battery 80V, 500Ah
rated dc voltage	$E = V_{dc} = 80$ V
rated current	$I_{S(RMS)} = 180$ A
maximum current (t = 60", t = 240")	$I_{SM1(RMS)} = 600$ A , $I_{SM2(RMS)} = 450$ A
technology	MOSFETs - parallel connected on an Insulated Metal Substrate (IMS)

The experimental results are shown in Figs. 8.
Fig. 8(a) shows the square wave operation of the multilevel converter (twelve-step), corresponding to the simulation results represented in Fig. 6(d).
Fig. 8(b) shows the PWM operations over 9 levels of the load phase voltage, corresponding to the simulation results represented in Fig. 6(a) with a required voltage vector outside the inner hexagon. For both figures, the phase voltage and current are shown in the upper and in the lower trace, respectively.

In order to verify the power balancing capability of the multilevel converter, the averaged line-to-line output voltages with reference to different power ratio *k* are investigated.
Fig. 10(a) shows the case of the same power delivered by each inverter ($k = 1/2$), i.e., line-to-line voltages with the same amplitudes and in phase opposition.
Fig. 10(b) shows the case of a power unbalance ($k = 3/4$), resulting in a corresponding line-to-line voltage unbalance.

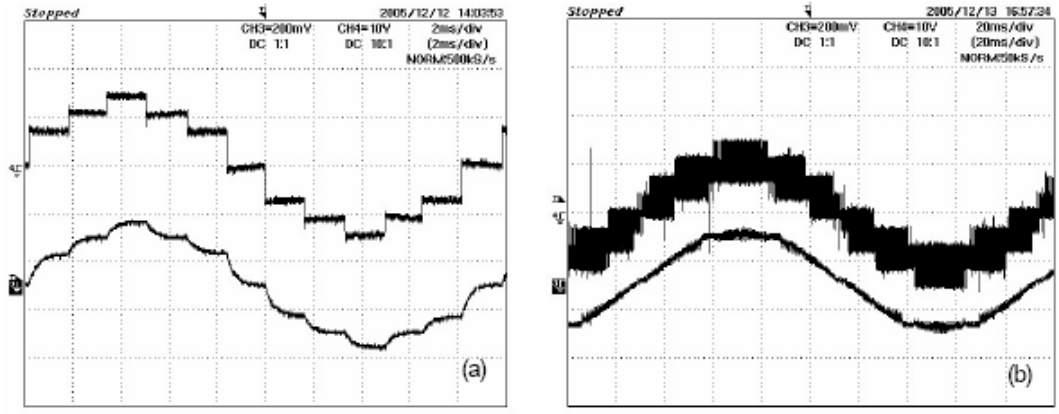


Fig. 8. Reduced scale converter prototype: (a) Square wave operation (twelve-step); (b) PWM operations (over 9 levels).

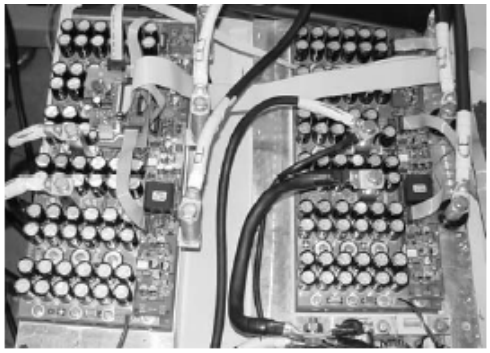


Fig. 9. Picture of the power stage of the full size converter.

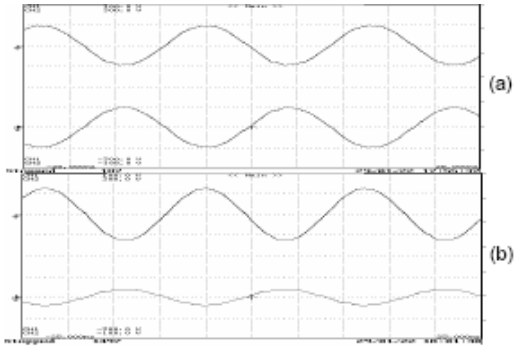


Fig. 10. Averaged line-to-line output voltages: (a) k = 1/2 (balanced); (b) k = 3/4 (unbalanced).

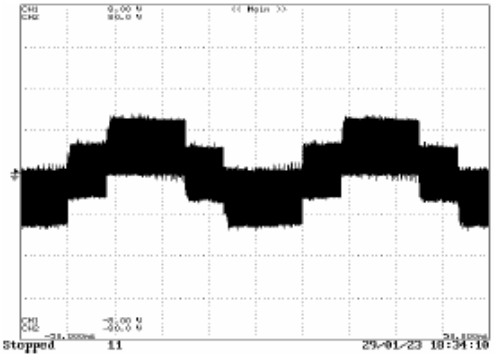


Fig. 11. Output phase voltage (over 5 levels).

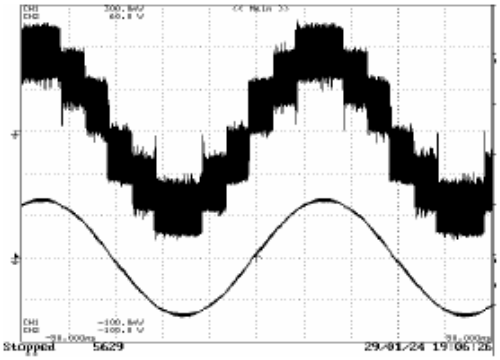


Fig. 12. Output phase voltage (over 9 levels) and current.

The instantaneous output phase voltage is shown in Figs. 11 and 12 with reference to a different modulation index m.

Fig. 11 is referred to the case of an output voltage vector rotating on a circle inside the inner hexagon. Note that the output phase voltage is distributed on the lower five levels only, since only the triangles in region ① are involved.

Fig. 12 shows both the voltage (upper trace) and the phase current (lower trace) referred to an output voltage vector rotating on a circle outside the inner hexagon. In this case all the nine voltage levels are involved. The resulting sinusoidal waveform of the phase current proves the effectiveness of the multilevel modulation algorithm.

8. Conclusion

An experimental investigation of a multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding three-phase six-wires loads has been presented in this paper. The feasibility and effectiveness of both the power and the control schemes have been verified by numerical simulations and a complete set of experimental tests.

In particular, it has been shown that correct multilevel operations with balanced and unbalanced powers between the two inverters are always achievable within a predictable power ratio.

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Appendix 5

Multilevel Operation of a Dual Two-Level Inverter with Power balancing Capability

Multilevel Operation of a Dual Two-Level Inverter with Power Balancing Capability

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***Abstract*—A multilevel converter topology feeding three-phase open-end winding loads is considered in this paper. The scheme is based on two insulated dc supplies, each one feeding a standard two-level, three-phase inverter. A three-phase six-wire load is connected across the output terminals. A new modulation technique able to regulate the sharing of the output power between the two dc sources within each switching cycle is presented. The performance of the whole system has been verified by numerical simulations and experimental tests.**

Index Terms—Multilevel converter, dual two-level inverter, space vector modulation strategy, power sharing, voltage source inverter.

I. INTRODUCTION

There are at least two applications in transport where the capability to supplying an electric motor by using two separate sources could be of a great interest in a near future. The first one concerns battery powered electric vehicles. The second one is related to hybrid thermal-electric powertrains which are under development for both vehicle traction and ship propulsion.

The battery powered electric vehicles such as electric fork lift trucks and industrial trucks in the power rating lower than 20kW represents more than 50% of the market and are frequently preferred to thermal engine vehicles for the undeniable economical and environmental advantages inherent in the electric traction.

In modern battery powered industrial electric vehicles the standard solution for the traction system is given by a two-level inverter feeding a three phase induction motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V) for safety reason. With this solution, it is quite difficult to realize an ac drive for a power rating higher than 20 kW, due to the high cost of the resulting high-current semiconductor power switches of the inverter. This problem limits the expansion of ac/drive and consequently the penetration of electric vehicles on this market.

Several solutions have been proposed in order to reduce the current rating of the power switches. The six-phase machine supplied by a six-phase inverter [1]-[4] allows to size the power switches at half the rated current of an equivalent three-phase scheme, but requires the realization of a six-phase machine. The multi-phase drive solution with 7 or more phases further reduces the power sizing of the converter legs, increase the reliability of the drive, but requires special machine design and complex control hardware [5].

An interesting solution is given by the use of a multilevel inverter, which can be realized with semiconductor devices having a voltage rating that is lower than the voltage applied to the motor. Several topologies of multilevel converters have been presented for low voltage applications [6]-[8]. Among these, the cascaded converter configuration called 'dual two-level inverter' can be conveniently used with a battery supply, due to the simplicity to obtain two electrically separated dc sources [9],[10]. The scheme of this multilevel converter applied to a battery supply system is given in Fig. 1. An important feature of the dual two-level inverter that will be presented

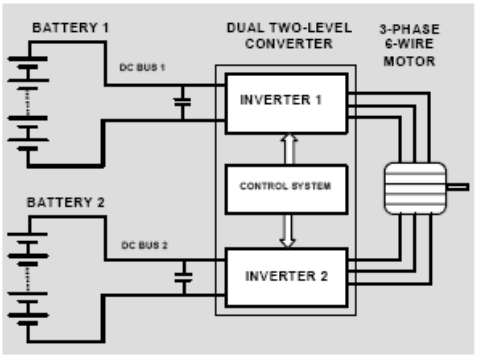

Fig. 1. Basic scheme of the battery powered electric system.

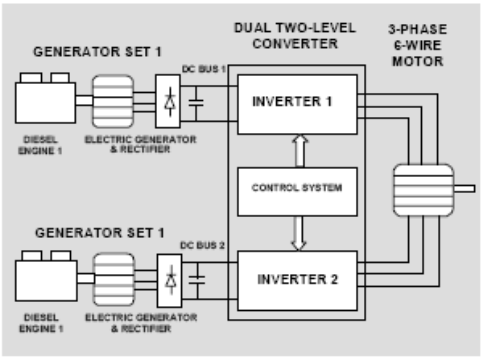

Fig. 2. Basic scheme of the diesel-electric propulsion system.

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in this paper is the capability to regulate the power sharing between the two sources yielding to an optimal control of the charge level of the two battery packs.

The second application regards hybrid powertrains. Nowadays, hybrid power trains in series configuration are developed for the thermal-electric traction system of heavy vehicles (industrial vehicles, trains, buses, etc..) and for the thermal - electric propulsion system of ships.

An attractive solution for hybrid powertrains could be realized by using the dual two-level inverter as it is represented in Fig. 2. This scheme is based on the use of two diesel-generator units supplying the two inputs of the dual two-level inverter connected to the motor. In this system, the two generating units are controlled in order to operate always with the best efficiency with respect to the power demanded by the electric motor connected to the vehicle wheels or to the ship screw. This is made possible by using the dual two-level inverter controlled with the proposed modulating strategy, because it allows to regulate the power sharing between the two sources. A very interesting characteristic of this system is the capability to operate at high efficiency in the low power range (less than 50%). In fact, the multilevel converter can be supplied from only one side, keeping off one diesel engine. This working condition yields to a reduced fuel consumption.

II. MULTILEVEL MODULATION STRATEGY

With reference to the scheme of Fig. 3, using space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter H and inverter L, respectively:

$$\bar{v} = \bar{v}_H + \bar{v}_L \ . \qquad (1)$$

The voltages $\bar{v}_H$ and $\bar{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to:

$$\bar{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\,e^{j\frac{2}{3}\pi} + S_{3H}\,e^{j\frac{4}{3}\pi}\right), \text{ and}$$

$$\bar{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\,e^{j\frac{2}{3}\pi} + S_{3L}\,e^{j\frac{4}{3}\pi}\right), \qquad (2)$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs.

The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 4. By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 E. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2/\sqrt{3}\,E$ (i.e., the radius of the inscribed circle).

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 5 (a), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted).

In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\bar{v}$ is synthesized by using the vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, as represented in Fig. 5 (b) for the three types of triangles.

Considering the standard SVM technique, $\bar{v}$ is obtained on the basis of the duty cycles μ, λ, γ :

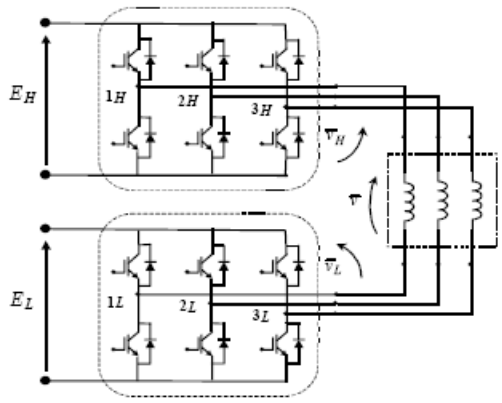


Fig. 3. Electric scheme of the multilevel converter.

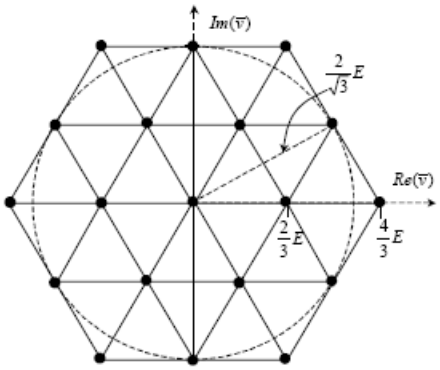


Fig. 4. Output voltage vectors of the multilevel converter.

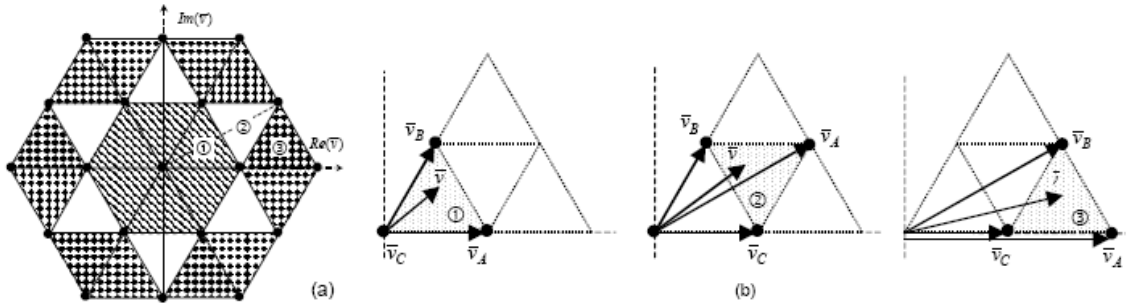


Fig. 5. (a) Highlight of the triangles in the three different regions ①, ②, and ③;
(b) Vector composition to obtain the output voltage in the three different regions.

$$\bar{v} = \mu \bar{v}_A + \lambda \bar{v}_B + \gamma \bar{v}_C . \tag{3}$$

where the duty cycle μ, λ, γ can be determined as

$$\begin{cases} \mu = \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \lambda = -\dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_A - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \gamma = 1 - (\mu + \lambda) = 1 - \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_A)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \end{cases} . \tag{4}$$

III. Regulation of the Power Sharing

A novel modulation technique, able to share the output power p between the two dc sources, is considered in this section. Introducing the power ratio k and imposing the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ to be in phase with the output voltage vector $\bar{v}$, leads to the following equations (average values over a switching period):

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \\ p = \dfrac{3}{2}\bar{v} \cdot \bar{i} = p_H + p_L \end{cases} \quad \begin{cases} p_H = \dfrac{3}{2}\bar{v}_H \cdot \bar{i} = k \cdot p \\ p_L = \dfrac{3}{2}\bar{v}_L \cdot \bar{i} = (1-k) \cdot p \end{cases} \tag{5}$$

In order to synthesize an output vector $\bar{v}$, the two inverters must generate the corresponding fraction of $\bar{v}$ by applying only their active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector. Being $\bar{v}_H$ and $\bar{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$, as shown in Fig. 6. Then, the voltage generated by the two inverters are:

$$\begin{cases} \bar{v}_H = \mu_H \bar{v}_\alpha + \lambda_H \bar{v}_\beta \\ \bar{v}_L = \mu_L \bar{v}_\alpha + \lambda_L \bar{v}_\beta \end{cases} . \tag{6}$$

In (6) the duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter H, whereas the duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter L.

By using standard SVM equations, the duty-cycles of inverters H and L can be calculated as:

$$\begin{cases} \mu_H = \dfrac{\bar{v}_H \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} , \quad \gamma_H = 1 - (\mu_H + \lambda_H) \end{cases} , \tag{7}$$

$$\begin{cases} \mu_L = \dfrac{\bar{v}_L \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_L = -\dfrac{\bar{v}_L \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} , \quad \gamma_L = 1 - (\mu_L + \lambda_L) \end{cases} . \tag{8}$$

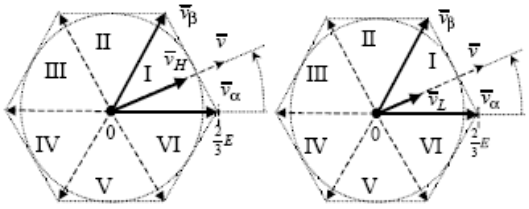


Fig. 6. Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

IV. Determination of the Operating Limits

The constrains of the duty-cycles expressed by (8) are

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases}, \quad \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases}. \tag{9}$$

These constrains introduce a limit in the range of variation of the power ratio k. In particular, the range of variation of k can be evaluated as a function of the desired output vector $\overline{v}$. Introducing in (9) the expressions (8) of duty cycles, and representing $\overline{v}_H$ and $\overline{v}_L$ in terms of k by (5), leads to

$$\begin{cases} \dfrac{k\overline{v}\cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ -\dfrac{k\overline{v}\cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ \dfrac{k\overline{v}\cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \leq 1 \end{cases}, \begin{cases} \dfrac{(1-k)\overline{v}\cdot j\overline{v}_\beta}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ -\dfrac{(1-k)\overline{v}\cdot j\overline{v}_\alpha}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \geq 0 \\ \dfrac{(1-k)\overline{v}\cdot j(\overline{v}_\beta - \overline{v}_\alpha)}{\overline{v}_\alpha \cdot j\overline{v}_\beta} \leq 1 \end{cases}. \tag{10}$$

Assuming sinusoidal output voltages $\left(\overline{v} = Ve^{j\vartheta}\right)$, and the modulation index m defined as

$$m = V \Big/ \frac{2}{\sqrt{3}}E, \quad 0 \leq m \leq 1,$$

with reference to sector I ($0 \leq \vartheta \leq \pi/3$), the solution of (10) is given by

$$\begin{cases} k \leq \dfrac{1}{2m}\dfrac{1}{\cos(\pi/6 - \vartheta)} \\ k \geq 1 - \dfrac{1}{2m}\dfrac{1}{\cos(\pi/6 - \vartheta)} \end{cases}, \tag{11a}$$

introducing the following parameter

$$a = \frac{1 - m\cos(\pi/6 - \vartheta)}{2m\cos(\pi/6 - \vartheta)}$$

in (11a) yields

$$\frac{1}{2} - a \leq k \leq \frac{1}{2} + a. \tag{11b}$$

Similar considerations can be made for sectors II ÷ VI. Eq. 11a gives the possible values of k as a function of the modulation index m and the output voltage phase angle ϑ. It can be noted that for any modulation index, the most stringent condition for k is given in the middle of the sector, i.e. for $\vartheta = \pi/6$. By applying this constrain, that corresponds to sinusoidal output voltages, the limit of the power ratio k is given from (11a) as a function of the modulation index only. Admissible values of the power ratio k are represented by the dashed area shown in Fig. 7. By analyzing this figure the following considerations can be done.

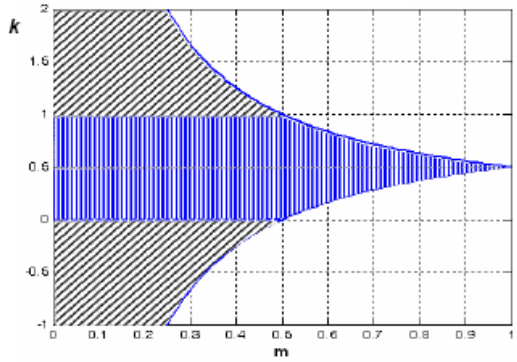


Fig. 7. Limits of the power ratio k vs. the modulation index m.

- If the maximum output voltage is required ($m = 1$), there are no means to regulate the power sharing between the dc sources. In this case only the value $k = 0.5$ is admissible and the two sources supply the same voltages, i.e., the same power;
- for $0.5 \leq m \leq 1$ the ratio k is limited as a function of m;
- for $m < 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if k is set to 0, all the load power is supplied by inverter L, whereas if k is set to 1 all the load power is supplied by inverter H. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only;
- for $m < 0.5$ the power ratio k could be greater than unity or lower than zero. It means that an amount of power could be transferred from one dc source to the other, and the inverter voltages $\overline{v}_H$ and $\overline{v}_L$ become in phase opposition, as shown by (5). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources.

V. Determination of the Switching Sequence

Once the limits for k has been defined, and the required inverter voltages $\overline{v}_H$ and $\overline{v}_L$ have been determined, the duty-cycles $\mu_H, \lambda_H, \gamma_H$ and $\mu_L, \lambda_L, \gamma_L$ can be calculated by (8) and (9). For achieving a correct multilevel operation, the three

TABLE I: SWITCHING SEQUENCE CORRESPONDING TO THREE-STEPS OPERATION FOR EACH INVERTER

	region ①					region ②						region ③				
output vectors	$\bar{v}_A$	$\bar{v}_B$	0	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_B$	$\bar{v}_C$	$\bar{v}_A$	$\bar{v}_B$	$\bar{v}_C$
	$\bar{v}_\alpha$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$	$2\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$
$\bar{v}_H$	0			$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$		0	$\bar{v}_\beta$			$\bar{v}_\alpha$			$\bar{v}_\beta$	0
H duty cycles	γ_H			μ_H	λ_H	μ_H		γ_H	λ_H			μ_H			λ_H	γ_H
$\bar{v}_L$	$\bar{v}_\alpha$	$\bar{v}_\beta$	0			0	$\bar{v}_\beta$		$\bar{v}_\alpha$		0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$		
L duty cycles	μ_L	λ_L	γ_L			$\leftarrow\gamma_L$	λ_L		μ_L		$\gamma_L\rightarrow$	λ_L	γ_L	μ_L		
sub-int.	μ''	λ''	γ	μ'	λ'	γ'	μ'	λ''	γ''	μ''	λ'	λ'	γ'	μ	λ''	γ''

output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, adjacent to the desired output voltage vector $\bar{v}$, must be generated by properly combining active vectors $(\bar{v}_\alpha, \bar{v}_\beta)$ and null vector of the two inverters. For regions ①, ②, and ③ shown in Fig. 5, three different vector compositions are defined, according to the following equations

Region ① Region ② Region ③

$$\begin{cases} \bar{v}_A = \bar{v}_\alpha + 0 \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = 0 + 0 \end{cases} \quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \tag{12}$$

On the basis of (12), the duty-cycles for the vectors $\bar{v}_\alpha, \bar{v}_\beta$ and 0 of inverters H and L, can be related to the duty-cycles μ, λ, γ of the output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$ calculated in (4).

For a given output vector $\bar{v}$ the two inverters H and L modulate with the same active vectors $\bar{v}_\alpha, \bar{v}_\beta$. It means that, at each interval of the switching period, the desired output vector can be obtained with interchangeable combinations of inverters vectors $\bar{v}_\alpha, \bar{v}_\beta, 0$. With reference to the three regions ①, ②, and ③ shown in Fig. 5, the proposed switching sequence is represented in Tab. I. In this switching sequence for example, when the output vector $\bar{v}_\alpha$ must be applied, the application time of $\bar{v}_\alpha$ can be subdivided in two equal sub-intervals. In the first time interval, inverter H generates $\bar{v}_\alpha$ and inverter L generates 0. In the second time interval, inverter L generates $\bar{v}_\alpha$ and inverter H generates 0. The same procedures can be adopted for generating the output vectors $\bar{v}_\beta$ and $\bar{v}_\alpha + \bar{v}_\beta$.

The duty cycles of the sub-intervals introduced in Tab. I can be determined for the three different regions on the basis of main duty-cycles μ, λ, γ and duty-cycles $\mu_H, \lambda_H, \gamma_H$, $\mu_L, \lambda_L, \gamma_L$ of the two inverters, as follows

Region ① Region ② Region ③

$$\begin{cases} \mu' = \mu_H \\ \mu'' = \mu_L \\ \lambda' = \lambda_H \\ \lambda'' = \lambda_L \\ \gamma \text{ is known} \\ - \end{cases} \quad \begin{cases} \mu' + \gamma' = \mu_H \\ \mu'' + \lambda' = \lambda_H \\ \lambda'' + \gamma'' = \gamma_H \\ \mu'' + \gamma'' = \mu_L \\ \mu' + \lambda'' = \lambda_L \\ \lambda' + \gamma' = \gamma_L \end{cases} \quad \begin{cases} \mu \text{ is known} \\ - \\ \lambda' = \lambda_L \\ \lambda'' = \lambda_H \\ \gamma' = \gamma_L \\ \gamma'' = \gamma_H \end{cases} \tag{13}$$

It can be noted that for regions ① and ③ the sub-intervals are five, whereas for region ② the sub-intervals are six and the corresponding duty cycles can be determined by solving a system of six equations. Only five of these equations are linear independent. Then, the equation system (13) for region ② can be solved in parametric form, assuming γ' as parameter.

Introducing the condition that all intervals must be not negative, $\mu', \mu'', \lambda', \lambda'', \gamma', \gamma'' \geq 0$, the admissible range of parameter γ' is determined. By choosing a value for γ' inside this range, the values of the other sub-intervals duty cycles are determined by (14) as

$$\begin{cases} \mu' = \mu_H - \gamma' \\ \mu'' = \lambda_H - \gamma_L + \gamma' \\ \lambda' = \gamma_L - \gamma' \\ \lambda'' = \lambda_L - \mu_H + \gamma' \\ \gamma'' = \mu_L + \gamma_L - \lambda_H - \gamma' \end{cases} . \tag{14}$$

In particular, by selecting a proper value for γ', it is always possible to null one of the six sub-intervals duty cycles. In this way the six-step commutation sequence collapses in five steps, as it happens in regions ① and ③.

Once all the sub-intervals are determined, they can be grouped in the switching sequence shown in Table I. In this

way, for each inverter, a traditional three-step commutation within the switching period is obtained, involving active and null vectors $\bar{v}_\alpha, \bar{v}_\beta$, 0.

VI. Simulation Results

The double inverter configuration has been implemented in the Simulink environment of Matlab by using appropriate S-functions. The simulation results, based on the switching sequence shown in Tab.I are shown in Fig. 8.

Fig. 8(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, $m = 1$ ($v = 2/\sqrt{3}\,E$), and $k = 1/2$. In this case, the two inverters generate the same voltages, i.e., supply the same power. It can be noted that the output phase voltage is distributed on nine levels.

Fig. 8(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, $v = 2/3\,E$ ($m = 1/\sqrt{3}$), and $k = 2/3$. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being $k = 2/3$, the voltage generated by inverter H are double with respect to voltage generated by inverter L.

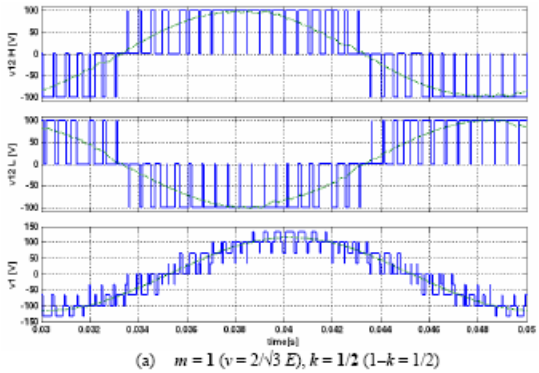
Fig. 8(c) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, $v = 1/\sqrt{3}\,E$ ($m = 1/2$), and $k = 1/3$. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio $k = 1/3$, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that in all the cases shown in Fig. 8 the output voltage is always distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 5(b).

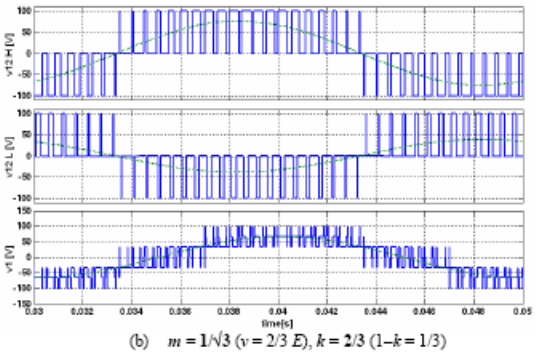
VII. Experimental Results

The multilevel inverter has been tested by both a reduced scale prototype (Fig. 9) and a full size power converter (Fig. 10), realized in the Labs of the Department of Electrical Engineering in Bologna.

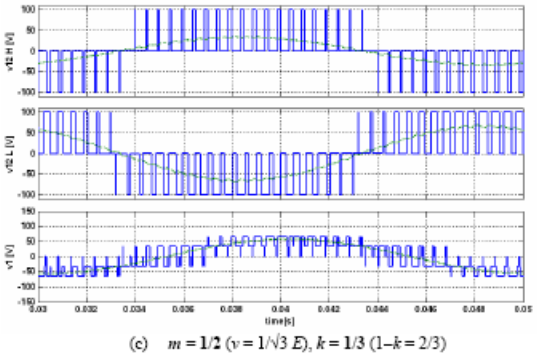
For both converters the control algorithm is based on the switching sequence presented in Table I. The proposed modulation strategy has been implemented on a control board based on TMS320F2812® DSP, operating with a clock frequency of 150 MHz, exploiting both its two independent three-phase PWM generators. In this way, no additional control hardware (e.g., FPGA) is necessary beside the DSP for switch commutation management.



(a) $m = 1$ ($v = 2/\sqrt{3}\,E$), $k = 1/2$ ($1-k = 1/2$)



(b) $m = 1/\sqrt{3}$ ($v = 2/3\,E$), $k = 2/3$ ($1-k = 1/3$)



(c) $m = 1/2$ ($v = 1/\sqrt{3}\,E$), $k = 1/3$ ($1-k = 2/3$)

Fig. 8. Voltage waveforms for different values of m and k. From top to bottom: line-to-line voltage generated by inverter H; line-to-line voltage generated by inverter L; load phase voltage (output).

A. Reduced scale converter prototype

The reduced scale system has been realized by using two modular inverters IR-AMS10UP60B® which assemble both power and driver circuits. These components are rated for a dc bus voltage of 450V and a phase current of 10A RMS (25°C).

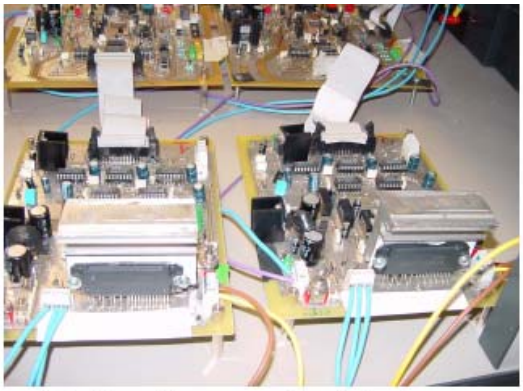


Fig. 9. Picture of the power stage of the reduced scale converter.

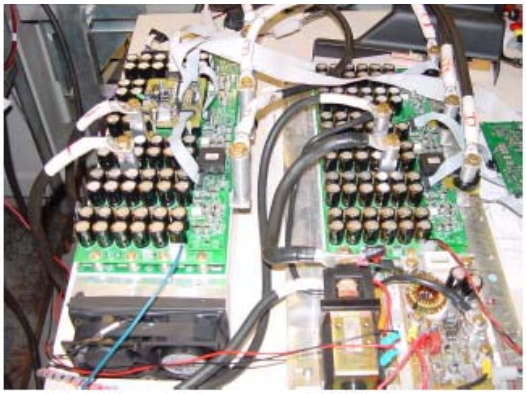


Fig. 10. Picture of the power stage of the full scale converter.

In Fig. 9 is shown a picture of the two power boards. Unfortunately the power and the control grounds are internally connected. Then, to make the required insulation between the two dc sources it has been necessary to introduce photo-couplers.

The experimental results are shown in Figs. 11. Fig. 11(a) shows the square wave operation of the multilevel converter (twelve-step). Fig. 11(b) shows the PWM operations over 9 levels of the load phase voltage, corresponding to the simulation results represented in Fig. 6(a) with a required voltage vector outside the inner hexagon. For both figures, the phase voltage and current are shown in the upper and in the lower trace, respectively.

B. Full size power converter

The power stage of the full size multilevel converter is depicted in Fig. 10. The two 'two-level' inverters have the main data reported in Table II.

In order to verify the power balancing capability of the multilevel converter, the averaged line-to-line output voltages with reference to different power ratio k are investigated. Fig. 12(a) shows the case of the same power delivered by each inverter (k = 1/2), i.e., line-to-line voltages with the same amplitudes and in phase opposition.

Fig. 12(b) shows the case of a power unbalance (k = 3/4), resulting in a corresponding line-to-line voltage unbalance. The instantaneous output phase voltage is shown in Figs. 13 and 14 with reference to a different modulation index m.

Fig. 13 is referred to the case of an output voltage vector rotating on a circle inside the inner hexagon. Note that the output phase voltage is distributed on the lower five levels only, since only the triangles in region ① are involved.

Fig. 14 shows both the voltage (upper trace) and the phase current (lower trace) referred to an output voltage vector rotating on a circle outside the inner hexagon. In this case all the nine voltage levels are involved. The resulting sinusoidal waveform of the phase current proves the effectiveness of the multilevel modulation algorithm.

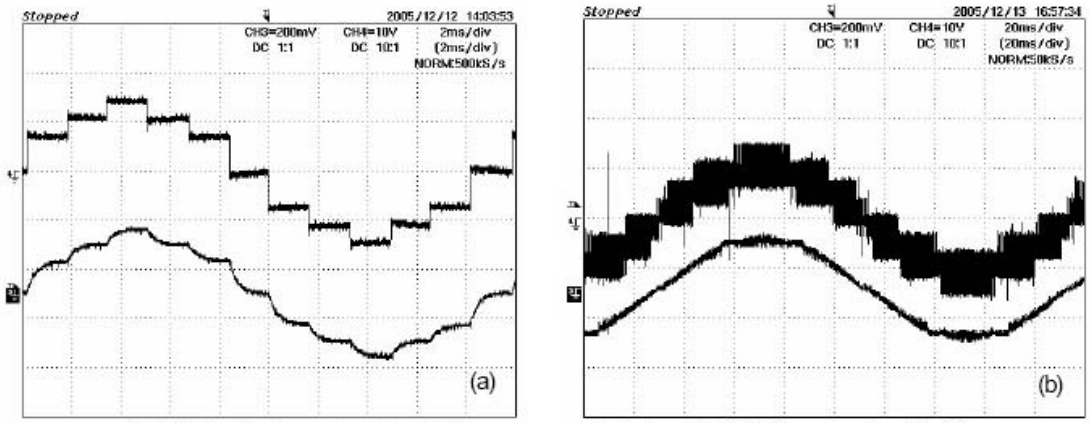


Fig. 11. Reduced scale converter prototype: (a) Square wave operation (twelve-step); (b) PWM operations (over 9 levels).

Table II. CHARACTERISTICS OF THE POWER INVERTERS	
supply system	lead acid battery 80V, 500Ah
rated dc voltage	$E = V_{dc} = 80$ V
rated output current	$I_{SER(RMS)} = 180$ A
maximum output current (t = 60", t = 240")	$I_{SM1(RMS)} = 600$ A , $I_{SM2(RMS)} = 450$ A
technology	MOSFETs - parallel connected on an Insulated Metal Substrate (IMS)

VIII. CONCLUSION

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding three-phase open-end winding loads has been considered in this paper. This scheme has the advantages of both avoiding homopolar components and maximizing the output voltage without additional circuitry. The paper has been focused on the development of a modulation strategy able to regulate the power sharing between the dc sources. It has been shown that balanced power sharing between the two inverters is always achievable within the switching cycle with correct multilevel voltage generation. Switching table for each inverter has been proposed and the limits of the power sharing ratio as function of the modulation index have been determined. Simulation results and experimental tests confirm the effectiveness of the proposed switching strategy.

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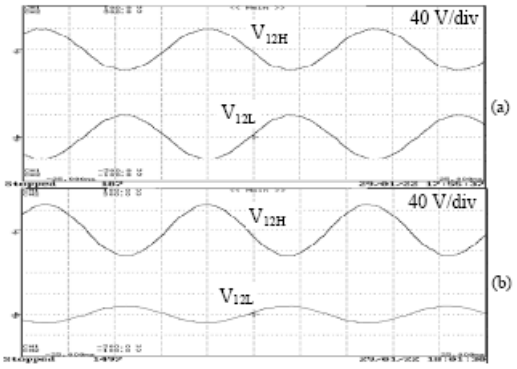

Fig. 12. Averaged line-to-line output voltages
(a) m=1/2, k = 1/2 (balanced); (b) m=1/2, k = 3/4 (unbalanced).

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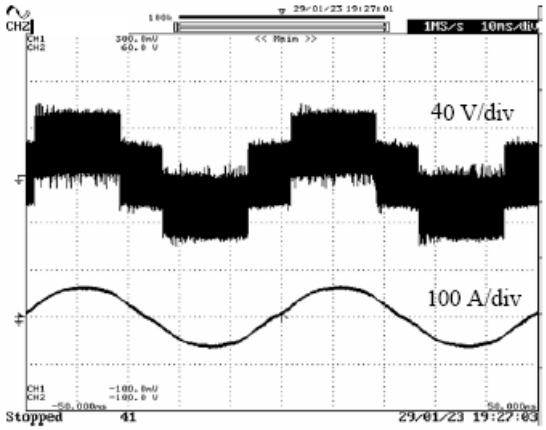

Fig. 13. Output phase voltage (over 5 levels) and current.

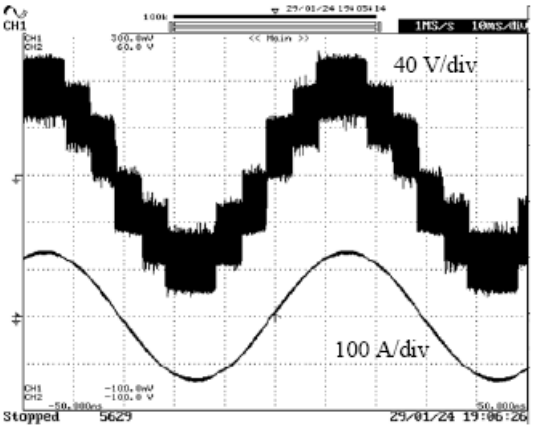

Fig. 14. Output phase voltage (over 9 levels) and current.

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