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A multilevel converter structure for grid-connected PV plants

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Abstract

A new conversion structure for three-phase grid-connected photovoltaic (PV) generation plants is presented and discussed in this Thesis. The conversion scheme is based on two insulated PV arrays, each one feeding the dc bus of a standard 2-level three-phase voltage source inverter (VSI). Inverters are connected to the grid by a traditional three-phase transformer having open-end windings at inverters side and either star or delta connection at the grid side. The resulting conversion structure is able to perform as a multilevel VSI, equivalent to a 3-level inverter, doubling the power capability of a single VSI with given voltage and current ratings.

Different modulation schemes able to generate proper multilevel voltage waveforms have been discussed and compared. They include known algorithms, some their developments, and new original approaches. The goal was to share the grid power with a given ratio between the two VSI within each cycle period of the PWM, being the PWM pattern suitable for the implementation in industrial DSPs. It has been shown that an extension of the modulation methods for standard two-level inverter can provide a elegant solution for dual two-level inverter.

An original control method has been introduced to regulate the dc-link voltages of each VSI, according to the voltage reference given by a single MPPT controller. A particular MPPT algorithm has been successfully tested, based on the comparison of the operating points of the two PV arrays. The small deliberately introduced difference between two operating dc voltages leads towards the MPP in a fast and accurate manner.

Either simulation or experimental tests, or even both, always accompanied theoretical developments. For the simulation, the Simulink tool of Matlab has been adopted, whereas the experiments have been carried out by a full-scale low-voltage prototype of the whole PV generation system. All the research work was done at the Lab of the Department of Electrical Engineering, University of Bologna.

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1. Introduction

1.1. An overview of multilevel inverters

The increase of the world energy demand has entailed the investment of huge amounts of resources, economical and human, to develop new technologies capable to produce, transmit and convert all needed electric power. In addition, the dependence on fossil fuels and the progressive increase of its cost lead to appearance of new cheaper and cleaner energy resources not related to fossil fuels. In ultimate decades, renewable energy resources have been the focus for researchers, and different families of power converters have been designed to integrate these types of supplies into the distribution grid. Beside the generation, electric power transmission needs high-power power electronic systems to assure conversion and the energy quality. Static converters such are high-voltage dc (HVDC), static synchronous compensator (STATCOM) and flexible alternating current transmission system (FACTS) are becoming standard part of the high-voltage grid in addition to traditional transformers and power lines. Last but not least, numerous industry applications, such as for example textile and paper industry, steel mills, electric and hybrid electric vehicles, ship propulsion, railway traction, 'more-electric' aircraft, etc., require utilization of variable speed electric drives. As far as the variable speed operation of electric drives is concerned, this is nowadays invariably achieved by supplying the machine, regardless of the type, from a power electronic converter.

Therefore, power electronic converters have the responsibility to carry out these tasks with high efficiency. At each of these stages rapid development of the power electronic lead to implementation of new power converter topologies and semiconductor technologies. Furthermore, the progress has been enabled by rapid developments in the areas of control algorithms, power semiconductors and microprocessors/digital signal processors (DSPs) during the last decades. Combining fast-switching power semiconductors with computationally powerful DSPs provides a convenient way to realize the complex control algorithms for power converters, so that excellent quality of control is achieved. Modern power semiconductor devices make this design practical for use at medium-voltage level.

A continuous race to develop higher-voltage and higher-current power semiconductors to drive high-power systems still goes on. In this way, the last-generation devices are suitable to support high voltages and currents (around 6.5 kV and 2.5 kA). However, currently there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices. These two concepts are shown in Fig. 1, where multilevel converters built using mature medium-power semiconductors are competing with classic power converters using high-power semiconductors that are under continuous development and not mature. Indeed, multilevel converters using more switching components can be both cheaper and more reliable than standard two-level solution

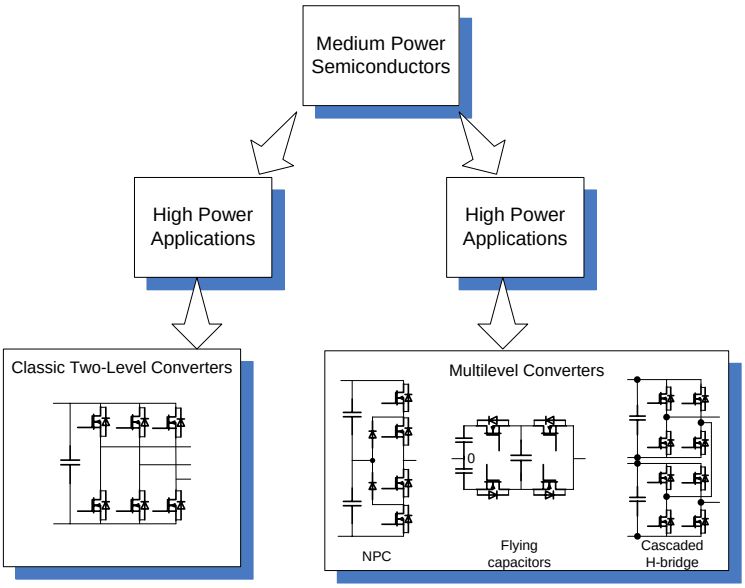


Fig. 1. Classic two-level versus common multilevel power converters.

with rare and more expensive components. In addition, multilevel solution requires smaller filter to satisfy power quality requirements, which can be significant item in high-power range. Nowadays, multilevel converters are a good solution for power applications because they can achieve high power using mature medium-power semiconductor technology [1], [2], covering power range from 1 MW to 30 MW [3].

The maximum power limit of standard three-phase converters is related to the limits of the maximum voltage and current of a switching component. Furthermore, higher is the power of a switch lower is the switching frequency. An initial solution to overcome these limitations was connection of several switches in series or in parallel. The series connection of two or more semiconductor devices faces problems due to the difficulty to synchronize perfectly their commutations. In fact, if one component switches off faster than the others it will blow up because it will be subject to the entire voltage drop designed for the series. Instead, parallel connection is slightly less complicated because of the positive resistance coefficient property of MOSFETs and IGBTs with the increment of junction temperature. When a component switches on faster than the others do, it will conduct a current greater than the rated one. In this way, the component increases its junction temperature and its resistance, in this way limiting the current to some extent. This effect makes possible to overcome the problems coming from a delay among gate signals or from differences among real turn on time of the components. Nevertheless, parallel connection of the switches has its limits: it requires careful I precise design of the system to achieve almost perfect symmetry of the components, a task more difficult to maintain as their number rises.

Moreover, multilevel converters present several other advantages:

- Generate better output waveforms with a lower dv/dt than the standard converters (power quality).
- Increase the power quality due to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses (low switching losses).

- Can operate with a lower switching frequency than two-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards (EMC).
- Can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

The main disadvantages of this technique are:

- Larger number of semiconductor switches required increasing complexity compared to the two-level solution.
- Capacitor banks or insulated sources are required to create the dc voltage steps.

Multilevel converters are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. The increase of maximum output voltage and number of levels is shown in Fig. 2 for two-, three- and four-level inverter with equal dc voltages applied to three-phase star-connected load. To some extent, the structure was born from the previous idea of series switch connection, with a significant modification that voltages across the switches need to be determined (fixed). This concept can be clearly seen for the simplest diode-clamped multilevel inverter shown in Fig. 3(a). Capacitor voltages can be fixed in a simple manner by connection of separate dc sources. If numerous isolated sources are not easily available, the dc bus voltage is split in several equal steps respectively by capacitor banks which need to be held equal by closed-loop control. It should be noted that before the introduction of the multilevel inverters high-power converters were typically realized by current source inverters, increasing the current ratings instead of voltage. This type of inverters are in continuous decline ever since.

The most common multilevel converter topologies are [4]:

- Diode clamped (neutral-point clamped),
- Flying capacitor (capacitor-clamped),
- Cascaded topology.

In addition, numerous hybrid topologies exist, derived from these basic types by varying or cascading them. In should be emphasized that in general all types of multilevel converters can produce the same voltage output, but with significant difference in number of the switches, their

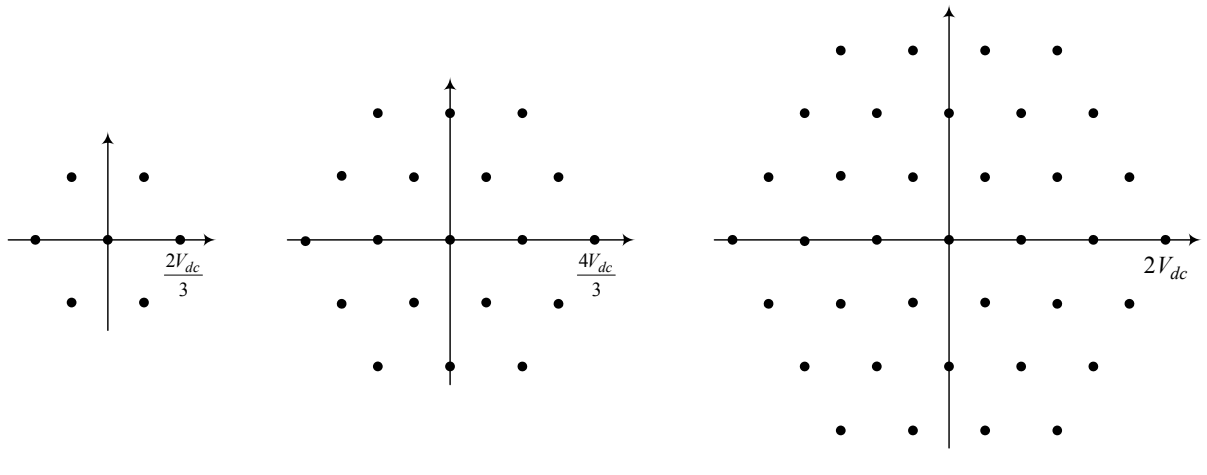


Fig. 2. Space vectors generated by (a) two- (b) three- and (c) four-level inverters with equal dc supply voltages.

topology, average voltage/current, control complexity etc. The first two common types are briefly overviewed in following section, whereas the cascaded topologies will be treated in more details in the next chapter.

1.1.1. Diode clamped inverters

Proposed almost thirty years ago, this converter is based on a modification of the classic two-level converter topology adding new power semiconductors per phase. The simplest NPC converter is shown in Fig. 3(a), implementing three leg voltage levels by doubling the number of switches and adding the same number of diodes to each additional switch. An additional level is clamped through the diodes (clamping diodes) connected to so-called neutral point of the source, as denoted in Fig. 3(a). Using this new topology, each power device has to stand, at the most, half voltage compared with the two-level case with the same dc-link voltage. Therefore, having the same power semiconductors ratings as the two-level case, the output voltage can be doubled. Note that for number of leg voltage levels n higher than three there is no single clamped point, (for even number of levels there is no neutral point at all). Based on the parity of the n converters are divided in neutral point clamped (NPC) for an odd number, and multi-point clamped, when n is even.

The principle of the switching is quite simple: for n-level inverter highest (n-1) adjacent switches need to be turned on together to achieve maximum leg voltage, next (n-1) switches to be turned on for (n-2)-th output level etc, up to the last (n-1) switches, which turned on together give zero leg voltage. There are also limitations: turning on n adjacent switches would lead to shoot-through. This can be illustrated on a three-level and four-level examples (Fig. 3), which are also of the highest practical interest, with the switching combinations given in Tab. 1. There are only three useful combinations for three-level case, whereas the other lead to undefined states. Therefore, this multilevel inverter has no redundant states (i.e. different switching combinations leading to the same output voltage). Similar conclusion can be made from four-level inverter switching states (Tab. 1).

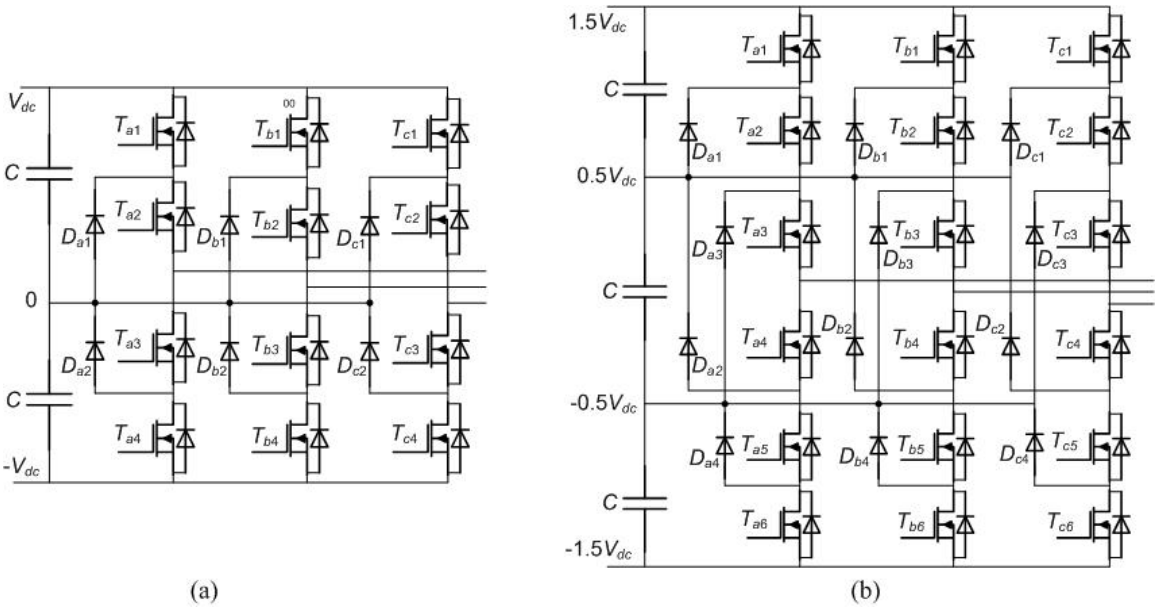


Fig. 3. Diode clamped multilevel inverter (a) three-, (b) four-level.

Tab. 1. Switching states and leg output voltages for three-level and four-level diode-clamped inverters

	State of the switches				3-level
	T_{a1}	T_{a2}	T_{a3}	T_{a4}	Leg voltage
Value	1	1	0	0	V_{dc}
	0	1	1	0	0
	0	0	1	1	$-V_{dc}$

	State of the switches						4-level
	T_{a1}	T_{a2}	T_{a3}	T_{a4}	T_{a5}	T_{a6}	Leg voltage
Value	1	1	1	0	0	0	$1.5V_{dc}$
	0	1	1	1	0	0	$0.5V_{dc}$
	0	0	1	1	1	0	$-0.5V_{dc}$
	0	0	0	1	1	1	$-1.5V_{dc}$

However, four-level inverter has a serious drawback compared to three-level one: additional diodes do not have equal reverse voltage. Indeed, when T_{a5} and T_{a6} are on, diode D_{a2} has to withstand reverse voltage equal to $2V_{dc}$, which is double of the transistors rated voltage. Furthermore, for inverters with higher number of levels this voltage further increases. In addition, switches are not directly clamped to the dc link capacitors by the opposite freewheeling diodes, except for the outmost two, in contrast to two-level inverter. In this way static or stray inductance overvoltage can appear across the switches. These two are the biggest drawbacks of NPC inverters with higher number of levels, because it practically turns back the problem to the initial series connection of switches.

For these reasons, three-level inverter is the most popular within its class. In order to solve these problems for higher number of levels a different diode-clamped topology has been proposed [5]. The structure provides a more direct clamping both diodes and switches to the dc capacitors. An example of four-level inverter is shown in Fig. 4(a). It can be noted that role of the "inner" diodes D_2 D_3 from Fig. 3(b) is shared between more diodes in Fig. 4(a). This topology can be also seen as derived from three-level inverter in Fig. 3(a) by adding "nested" clamping diodes instead of "crossed" as in Fig. 3(b).

Taking the same three-level topology as a starting point another type of multi-point clamped inverter can be derived, as shown in Fig. 4(b). This four level inverter using couples switch-di-

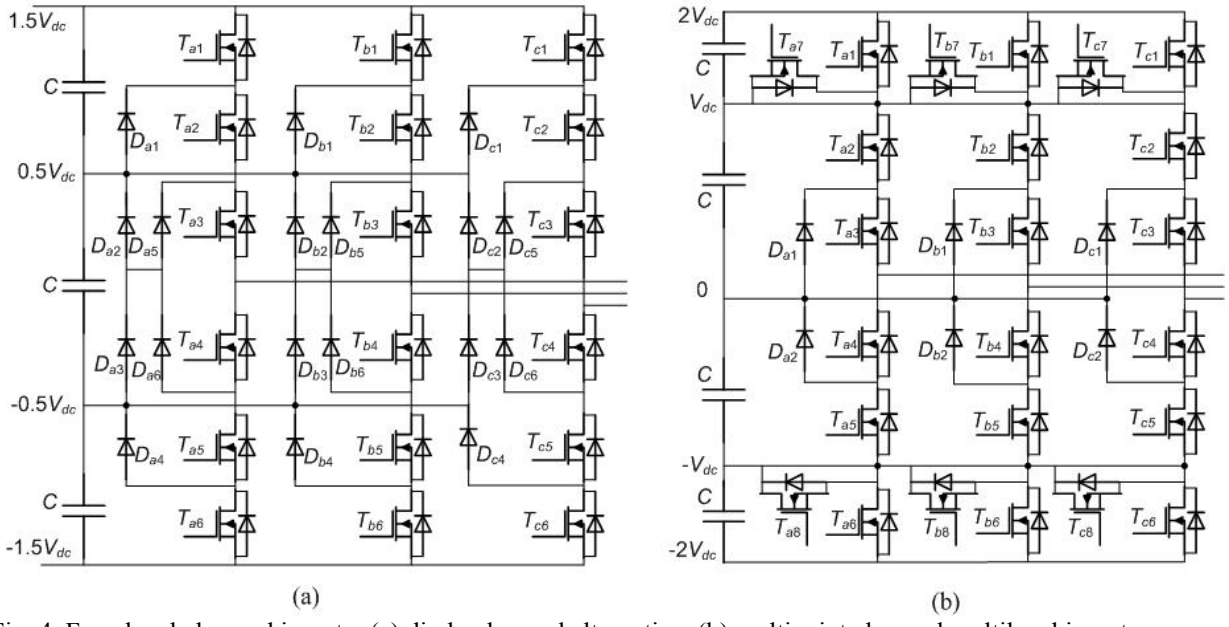


Fig. 4. Four-level clamped inverter (a) diode-clamped alternative, (b) multipoint clamped multilevel inverter.

Tab. 2. Switching states and leg output voltages for four-level multipoint clamped multilevel inverter.

	State of the switches								Leg voltage
Value	T_{a1}	T_{a2}	T_{a3}	T_{a4}	T_{a5}	T_{a6}	T_{a7}	T_{a8}	
	1	1	1	0	0	0	0	1	$2V_{dc}$
	1	1	0	1	0	0	1	0	V_{dc}
	1	0	1	0	0	1	0	1	0
	1	0	0	1	0	1	1	0	0
	0	0	1	0	1	1	0	1	$-V_{dc}$
	0	0	0	1	1	1	1	0	$-2V_{dc}$

ode instead of using a simple diode to clamp voltages. This type of converter contains the same number of the switches as previously presented diode-clamped counterparts, but requires a more complex control due to the presence of additional controllable switches. However, the modulation can be simplified pairing complementary switches as can be seen in Tab. 2. Moreover, the switches in the middle of the leg must carry twice the voltage of the others. The benefits of the structure are lower number of switches in series that conduct and therefore lower losses.

A common drawback for all diode clamped inverters (DCI) is caused by its series connection of controlled switches: the switches closer to the leg output conduct more pulses than those further, e.g. for three-level inverter T_{a2} conducts double of T_{a1} current. Furthermore, the difference increases with the number of levels. Both drawbacks limit the number of levels in practice to a five [6]. Additionally the structure is not modular; increase in number of levels requires complete reconfiguration instead of simple addition of modules. Nevertheless, NPC is one of the most popular multilevel converters in more conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills, which offer solutions for industries including oil and gas, metals, power, mining, water, marine, and chemistry. Another application of this converter is as high-voltage rectifier for grid-supplied loads [7] or wind turbines, where a back-to-back (active front-end) topology became an industrial standard [8].

1.1.2. Flying capacitor inverters

The flying capacitor (FC) topology is in some way derived from it diode clamped predecessor by the simplification – elimination of the clamping diodes. FC inverter uses additional capacitors oppositely charged to be included in series with dc supply, since after the elimination of the diodes it is not possible to connect leg output directly to the desired dc voltage. These capacitors have the same function of the clamping diodes in diode-clamped converter: they keep constant the voltage drop between the busses to which they are connected. For this reason, they are called clamping capacitors, giving the name to the converter [3]. Another name that can be found in the literature is the nest cell converter [9]. The principle of the switching is similar to the DCI, and will be explained for three-level and four-level examples shown in Fig. 5. However, there is a difference in the principle: clamping capacitors need to be connected in series, and must not be short-circuited by turning on switches connected in parallel. The switching table is given in Tab. 3, showing redundancy for leg output voltage equal to zero which is another difference with respect to DCI. These voltage-level redundancies can be used as extra degrees of freedom for

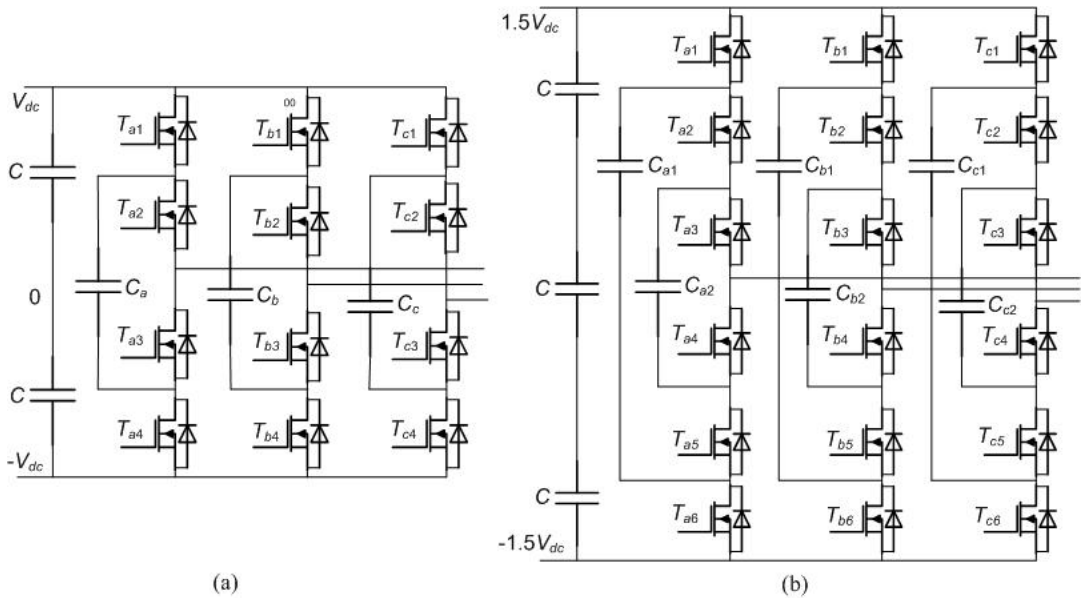


Fig. 5. Flying capacitor inverter (a) three-level, (b) four-level.

control or optimization purposes. However, the main and most important difference with the NPC topology is that the FC has a modular structure that can be more easily extended to achieve more voltage levels, for this reason sometimes called multicell inverter [6]. This can be easily observed by redrawing the FC as illustrated in Fig. 6(a) showing the unit cell of the inverter. This makes possible a modular approach presented in Fig. 6(b).

The main drawback of the FCI is complex control algorithm and many voltage sensors for high number of capacitor voltages to be controlled. Another problem is capacitors flying connection that requires both initialization and control, which requires the use of the redundant states. The hardware disadvantage is requirement for significant number of capacitors. Since the applications are at lower carrier frequencies the high values of capacitors is the major disadvantage of the FCI [3]. In addition, capacitors are unequally rated, as can be noted in Fig. 5(b), where the outer capacitors need to withstand almost full dc voltage, compared to DCI where all capacitors were equal and relatively small. In addition, the drawback of unequal switch currents common with DCI remained. To conclude, the youngest among the common multilevel configurations (proposed less than twenty years ago), this converter remained in the shadow of the other two competitors.

A generalized structure including in itself both diode-clamped and flying capacitor converters has been found [10]. This generalized clamped inverter has modular structure with the same

Tab. 3. Switching states and leg output voltages for three-level flying capacitor inverter

	State of the switches				3-level
Value	T_{a1}	T_{a2}	T_{a3}	T_{a4}	Leg voltage
	1	1	0	0	V_{dc}
	1	0	1	0	0
	0	1	0	1	0
	0	0	1	1	$-V_{dc}$
	0	1	1	0	short-circuit

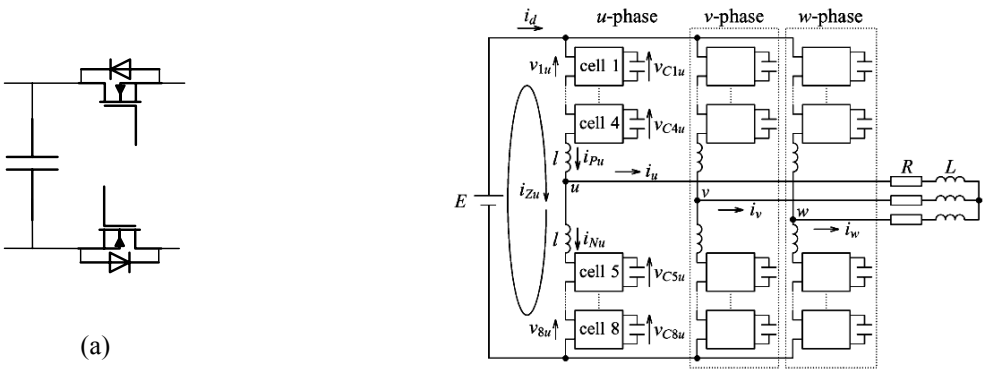


Fig. 6. Modularity of flying capacitor structure (a) unit cell, (b) converter.

basic cell as FCI from Fig. 6(a), as can be seen from Fig. 7(a). By omitting some switches (transistors and/or diodes) basic clamped converters can be derived, such is FC shown in Fig. 7(b). In similar manner, both types of the diode clamped inverters (shown in Fig. 3(a) and Fig. 4(a) respectively) can be derived.

1.1.3. Hybrid configurations

The major advantages of the hybrid structure include the fact that it joins the best performance characteristics of two different power converters, and can achieve similar performance to other multilevel VSCs with a reduced number of switches (e.g. 24 for seven-level hybrid VSC as opposed to 36 for diode-clamped, cascaded, capacitor-clamped VSCs). There are three principles how hybrid configurations are derived:

- Combining from three basic multilevel structures (mixed-level hybrid)
- Combining different dc supplies (asymmetric hybrid)
- Combining different modulation principles

and usually more than one of the principles is used.

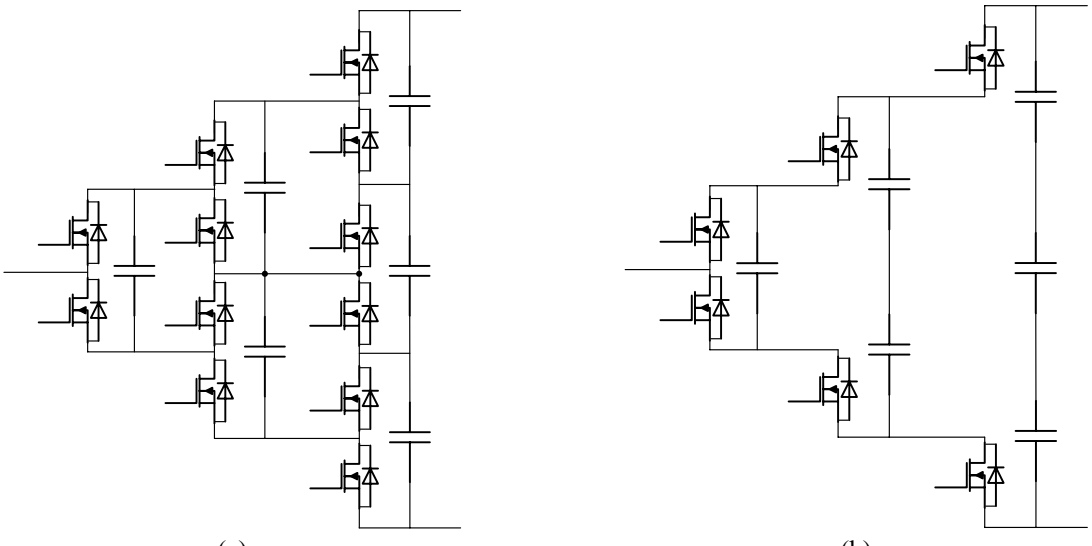
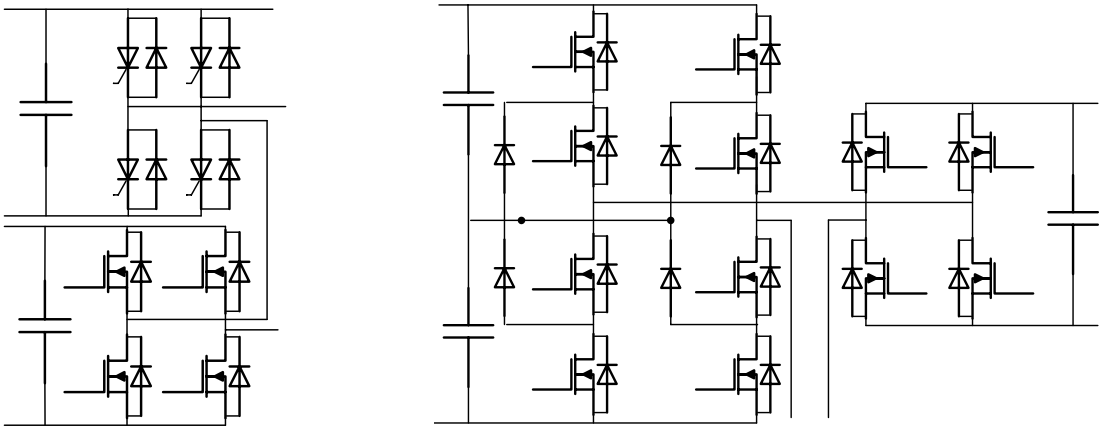


Fig. 7. Generalized clamped inverter (a) four-level example, and (b) derived FCI.



(a) (b)

Fig. 8. Examples of cascaded hybrid inverters (a) same number of levels different ratings, (b) different level number.

A typical example for the third method is combination of high-voltage (high-power) and low-voltage (low-power), as illustrated in Fig. 8. In terms of operation, the hybrid converter uses the HV stage to achieve the bulk power transfer and the LV stage as a means to improve the spectral performance of the overall converter. This enables a HV stage to be made of HV blocking components but not necessarily fast switching ratings (e.g. thyristors), while the LV stage is constructed using devices that have fast switching characteristics but not necessarily high-voltage blocking characteristics (e.g. IGBT). In mixed-level hybrid multilevel cells converter, the H-bridge cells of cascaded leg are substituted by diode-clamped or flying-capacitor. Mixed-level hybrid multilevel cells converter is well suited for high-voltage high-power applications because of the reduction of required insulated sources in the respect of a cascade H-bridge with the same number of output levels. Since most of the hybrid configurations include some way of cascaded connection it will be elaborated in more details in the next chapter.

Drawbacks of the hybrid solutions the converter control is more complex than standard. Furthermore, in case of grid supply different dc sources require additional transformer windings and rectifiers. Another problem that must be addressed for the hybrid converter is that the HV stage will supply more power than the load requires in the middle ranges of the modulation index. Under these operating conditions, the LV stage will be required to operate in a rectification mode, which means that the dc link must be capable of a bidirectional power flow. This necessitates the use of a PWM rectifier on the front end and further complicates the system. However, at medium and high power levels advantages of reduced switch count still make it attractive.

Combinations of the diode-clamped and cascade converters are also possible. Figure 9(a) shows one implementation that combines a three-level NPC with a single-cascade two-level transistor H-bridge (subinverter) in series with each phase. In this case, six levels can be obtained. To keep the power part simple and the efficiency high, the subinverters have no feeding from the net and can only supply reactive power [11]. Another topology is a cascaded-transformer inverter shown in Fig. 9(b), that adds up output voltage on the expense of the transformer windings. In this way, the number of switching devices and other components of conventional multilevel inverters such as diode-clamped, flying capacitors, and cascaded full-bridge cells can be saved.

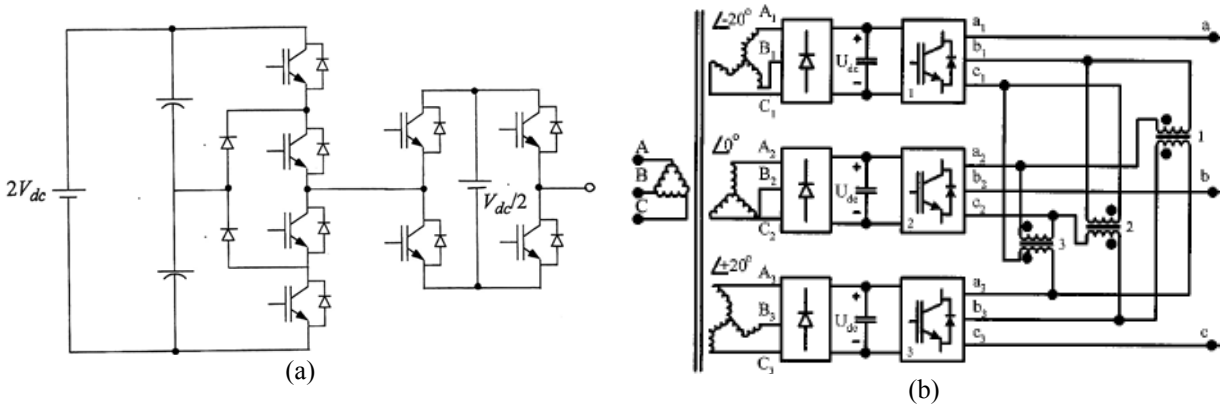


Fig. 9. Examples of cascaded hybrid inverters: (a) diode-clamped and cascade converter combination (b) cascaded multitransformer inverter.

1.2. Photovoltaic conversion

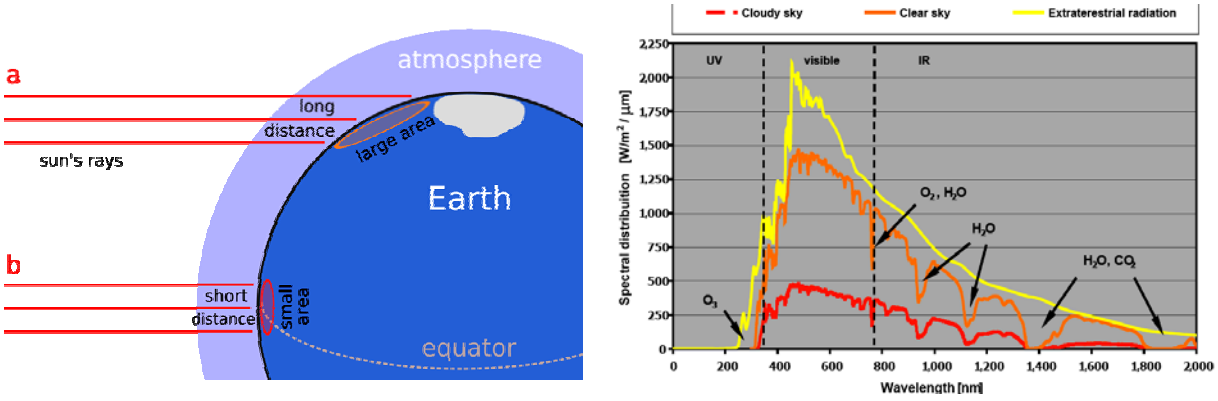
1.2.1. Extraterrestrial solar energy

The Sun is made up of about 80% hydrogen, 20% helium and only 0.1% other elements. Its radiant power comes from nuclear fusion processes, during which the Sun loses 4.3 million tones of mass each second, to be converted into radiant energy. Each square meter of the Sun's surface emits a radiant power of 63 MW, which means that just a fifth of a square kilometer emits an amount of energy equal to the global primary energy demand on Earth. Fortunately, solar irradiance decreases with the square of the distance to the Sun, so only a small part of this energy reaches the Earth's surface. Applying the Stefan-Boltzmann's law to the Sun and Earth the radiant flux, received from the Sun outside the Earth's atmosphere can be calculated as 1360 W/m^2 [12]. Since the distance of the Earth to the Sun changes during the year, solar irradiance outside the earth's atmosphere also varies between 1325 W/m² and 1420 W/m². The annual mean solar irradiance is known as the solar constant and is 1367 W/m². The radiation intensity outside the Earth's atmosphere according to the solar constant is called the extraterrestrial radiation. The first practical conversion of solar to electric energy was to power orbiting satellites and other spacecraft, but today the majority of photovoltaic modules are used for grid connected power generation.

Only a surface that is perpendicular to the incoming sun's rays receives this level of irradiance. Outside the atmosphere, and therefore not subject to its influence, solar irradiance has only a direct component – all solar radiation is virtually parallel. This irradiance is also called direct normal or beam irradiance E_{beam}. Under these conditions, a surface that is oriented parallel to the sun's rays receives no irradiance. The specific direct solar irradiance E_{dir} that reaches an inclined surface is lower depending on the cosine of the angle of incidence φ:

$$E_{dir} = E_{beam} \cos\varphi \tag{1}$$

This is illustrated in Fig. 10(a), where can be seen that for with increase of the angle φ the same radiation power covers larger area, thus decreasing the irradiance as per area value.



(a) (b)

Fig. 10. Earth's atmosphere effect on the solar radiation (a) attenuation (b) spectral distribution.

The Sun's outer surface, namely photosphere, has an effective blackbody temperature of approx. 6000 K. Viewed from the Earth, the radiation emitted from the Sun appears to be essentially equivalent to that emitted from a 6000 K blackbody at, with wavelength maximum around 500 nm - yellow color. The total amount of radiation present, at all frequencies is shown in Fig. 10(b) for radiation incident on a surface, called spectral irradiance, and has SI units W/m^3, or commonly $W \cdot m^{-2} \cdot nm^{-1}$.

1.2.2. Insolation quantities and measurement

Various different terms are used when dealing with solar radiation, often incorrectly even by some solar specialists [13].

- The total specific radiant power, or radiant flux, per area that reaches a surface is called irradiance. Irradiance is measured in W/m² and has the symbol *E*.
- When integrating the irradiance over a certain period it becomes solar irradiation. Irradiation is measured in either J/m² or Wh/m², and represented by the symbol *H*. Since the variation of annual irradiations from year to year can be well over 20 %, a measurement period should cover at least 7–10 years. Insolation (incident solar radiation) is a measure of solar radiation energy received on a given surface area in a given time. It is commonly expressed as average irradiance in watts per square meter W/m^2 or kilowatt-hours per square meter per day $kWh/(m^2 \cdot day)$ (or hours/day).
- For daylight purposes, only the visible part of the sunlight is considered. The analogous quantity to the irradiance for visible light is the illuminance. This uses the unit lm/m² (lumen/m²) or lx (lux). Direct sunlight has a luminous efficacy of about 93 lm/W of radiant flux, which includes infrared, visible, and ultraviolet light. Bright sunlight provides illuminance of approximately 100.000 lux or lumens per square meter at the Earth's surface.
- Direct insolation is the solar irradiance measured at a given location on Earth with a surface element perpendicular to the Sun's rays, excluding diffuse insolation (the solar radiation that is scattered or reflected by atmospheric components in the sky).
- Diffuse insolation is the solar radiation that is scattered or reflected by atmospheric components (clouds, for example) to the Earth's surface.

(a) (b)

Fig. 11. Insolation sensors (a) *Solarc* "Mac-Solar E" meter, (b) *Hukseflux* SR11 first class pyranometer.

Measurement of the solar irradiance is a quite demanding task, dust on the sensors, inaccurate trackers or dirt can reduce the measurement quality significantly. Today common sensors can be classified as:

- Low-cost pyranometers, Fig. 11(a), use silicon sensors with a small photovoltaic cell that generates an electrical current that is nearly proportional to the global solar irradiance. A pyranometer measures the global irradiance and typically does not require any power to operate. However, these sensors measure only part of the solar spectrum – they cannot sense infrared light. The annual accuracy of these sensors is limited because the spectrum changes with the air mass. In the ideal case, it can be in the range of 5 %.
- Pyranometers that are more precise use a black receiver plate that is mounted below a double glass dome, Fig. 11(b), and the plate heats up depending on the incoming irradiance. A thermocouple converts the heat difference between the plate and its surroundings into a voltage signal that is proportional to the irradiance. These sensors can obtain annual accuracies well above 3%. For irradiance measurement by definition is required that the response to "beam" radiation varies with the cosine of the angle of incidence. This means full response when the solar radiation hits the sensor perpendicularly (normal to the surface, sun at zenith, 0 degrees angle of incidence), zero response when the sun is at the horizon (90 degrees angle of incidence, 90 degrees zenith angle), and 0.5 at 60 degrees angle of incidence. It follows from the definition that a

(a) (b)

Fig. 12. Irradiance sensors (a) two-axis tracked pyrheliometer for direct normal irradiance measurements (b) with shading ball for diffuse irradiance measurements.

pyranometer should have a so-called “directional response” or “cosine response” that is close to the ideal cosine characteristic.

- To measure the direct normal or beam irradiance, the sensor is mounted inside the end of an absorber tube (this tube keeps the diffuse irradiance away). This so-called pyrheliometer has to be mounted on a two-axis tracker that follows the sun very accurately, Fig. 12(a). If a shading ball, or shading ring, permanently shades a pyranometer, it measures the diffuse irradiance since direct irradiance is kept away, Fig. 12(b).

1.2.3. Solar energy on the Earth

However, the almost constant extraterrestrial radiation is highly variable on the Earth surface due to the attenuation such as reflection, scattering (reflection in many directions) and absorption in the Earth atmosphere, which means that only some part of incident radiation becomes transmitted. A well-known example is ultraviolet part of the solar energy absorbed by ozone in the stratosphere. Furthermore, there is additional attenuation of the clear sky is determined by the length of the atmospheric path traversed by sunlight, which refers to the so-called relative Airmass (AM). The solar radiation is reflected and scattered primarily by clouds (moisture and ice particles), particulate matter (dust, smoke, haze and smog) and various gases. Airmass represents the strength (mass) of the atmosphere, and can be approximated by (1) with the Sun at the angle to overhead, as illustrated in Fig. 10(a).

$$\text{Air Mass} = 1/\cos\varphi \tag{2}$$

Spectrum AM 0 denotes extraterrestrial radiation whereas AM 1.5 approximately represents solar noon near the spring and autumn equinoxes at the 45º latitude with surface of the cell perpendicular to radiation and is used for standard testing (Fig. 13).

With the Sun overhead at noon, the sky appears white because little scattering occurs at the minimum atmospheric path length. At sunrise and sunset, however, the solar disc appears red because of the increased atmospheric path associated with relatively high scattering of the short wavelength blues and greens. As a result, the irradiation falling to the optimally set surface is at a see level at midday amounts of 1000 W/m2 when the sky is cloudless. Of this energy approximately 527 W is infrared, 445 W is visible, and 32 W is ultraviolet part of the spectrum. With altitude, the maximum values of radiation increases due to the decrease of the optical thickness of the atmosphere: for every added 100 m value of radiation in the troposphere

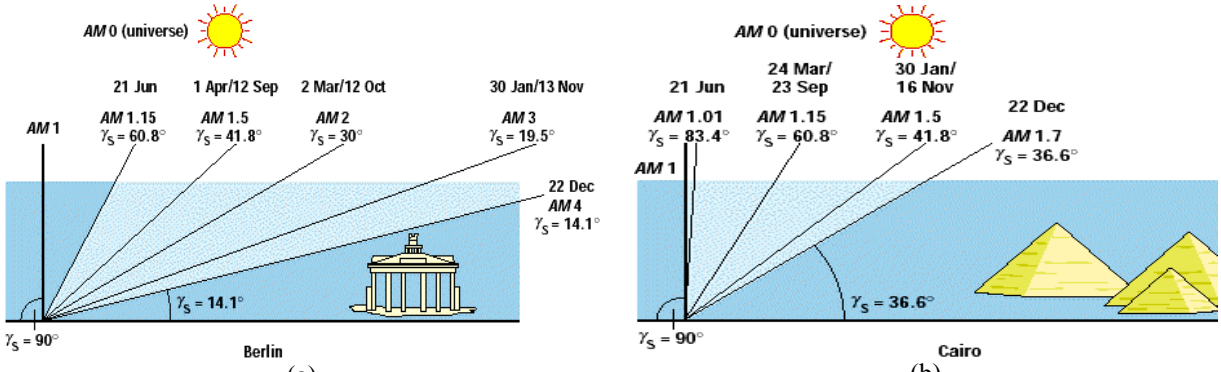
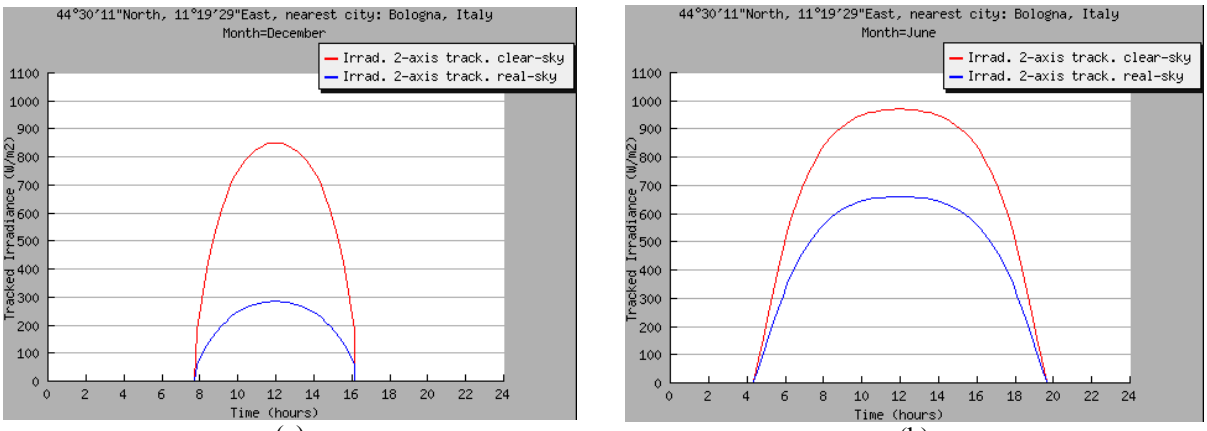


Fig. 13. Position of the sun and airmass values at solar noon for various days in Berlin (52º N) and Cairo (30º N).



(a) (b)

Fig. 14. Daily and seasonal change of the irradiance in Bologna, 45° N latitude: (a) winter, (b) summer diagram.

increases by 0.007-0.014 kW/m^2. Maximum values of radiation recorded in the mountains reach 1190 W/m^2.

There are three major sources of irradiation variability:

- Change in Earth's atmosphere regarding the movement of the clouds, particulate matter (dust, smoke, haze and smog) and various gases. As a consequence, the maximum irradiation is attenuated up to only 150 W/m^2 in an overcast dull day.
- Change of Sun tilt angle due to the Earth rotation. The radiation intensity on the Earth's surface changes continually during a day even if the sky is clear. Less radiation is available early in the morning or late in the afternoon, when the rays make a longer path through the atmosphere and therefore more attenuation than at midday, as illustrated in Fig. 14 for different time of the day.
- Change of the inclination of the Sun's trajectory in the sky (as seen by an observer on Earth's surface) due to the axial tilt of the Earth (often known as the obliquity of the ecliptic), varies over the course of the year (Fig. 13). For the northern hemisphere the minimum values of insolation occur in December, and the maximum at spring when the air contains less condensation products and dust then in summer. Although the difference by comparing Fig. 14(a) and (b) is significant, it can be seen that the difference between seasonal maximum irradiation in temperate latitudes is not so drastic. However, it increases towards the poles where winter irradiation becomes zero.

Surprisingly, the maximum direct irradiance little increase with decreasing of latitude, despite the increase in the height of the Sun. This is because of increasing moisture and dust content in air in southern latitudes. Therefore, at the equator, the maximum values are slightly greater than the maximum in temperate latitudes. As an illustration, the maximum direct irradiance at the following places in W/m^2 is given in Tab. 4 [14]. Experimental results are very prone to the influence of this change. Therefore they should be conducted close to the sun highest position, which is usually around noon in "winter season" (from autumn to spring, no daylight saving time), and around 1 PM in the remaining part of the year (from spring to autumn, daylight saving time). Around this time, the derivative of the cosine function is minimal, so the change of the irradiation is as small as possible. In contrary, in early morning (late afternoon) changes are so quick that on a clear sky almost every few minutes power increase (decrease).

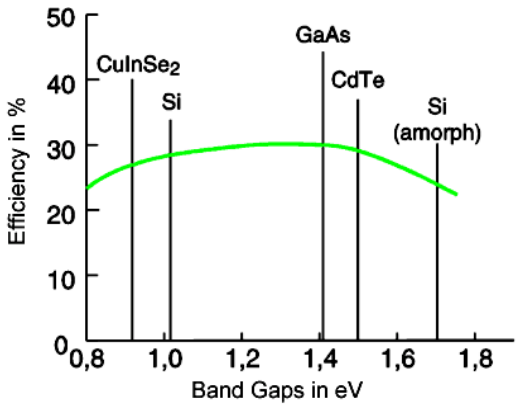
Tab. 4. The maximum direct irradiance for places with the different latitude.

Place	Latitude	Max. irradiance [W/m^2]
Sahara	20º North	1100
Tashkent	40º North	1060
Moscow	55º North	1030
Tiksi	70º North (Polar circle)	910

1.2.4. Photovoltaic cells

Photovoltaic cell provides direct conversion of sunlight to electricity. It is actually a p-n junction, like ordinary diode; however, its construction is adapted to maximum utilization of solar radiation. The principle is based on the interaction between incident photons and silicon (or other element) electrons, which generates an electron-hole pair, if the photon energy is higher than the silicon band gap value. However, much of the solar radiation reaching the Earth is composed of photons with energies greater than the band gap of silicon. These higher energy photons will be absorbed by the solar cell, but the difference in energy between these photons and the silicon band gap is converted into heat via lattice vibrations rather than into usable electrical energy. This specific portion of the radiant energy cannot be used, because the light quanta (photons) do not have enough energy to "activate" the charge carriers. This leads to a theoretical maximum level of efficiency, e.g. approximately 28 % for crystal silicon (Fig. 15).

Numerous efforts were done to determine equivalent circuit applicable to all conditions. A typical circuit is shown in Fig. 16(a), representing the cell as an antiparallel connection of the non-ideal current source and a diode, with additional resistances in series R_s and parallel R_{sh} [12]. For low values of the cell output voltage V (corresponding to lower load resistance) the diode voltage is bellow its threshold and almost all source light-generated current I_L is obtained as the output current I. To a very good approximation, the cell “light” current I_L is directly proportional to the cell irradiance. As the output voltage increases, the diode is surpassing the threshold and conducting bigger portion of the source current, up to the no-load condition when all the current I_L is overtaken by the diode. The I-V characteristic of a typical PV cell is given in Fig. 16(b) between I_{sc} and V_{oc} points. Note that the amounts of current and voltage available from the cell

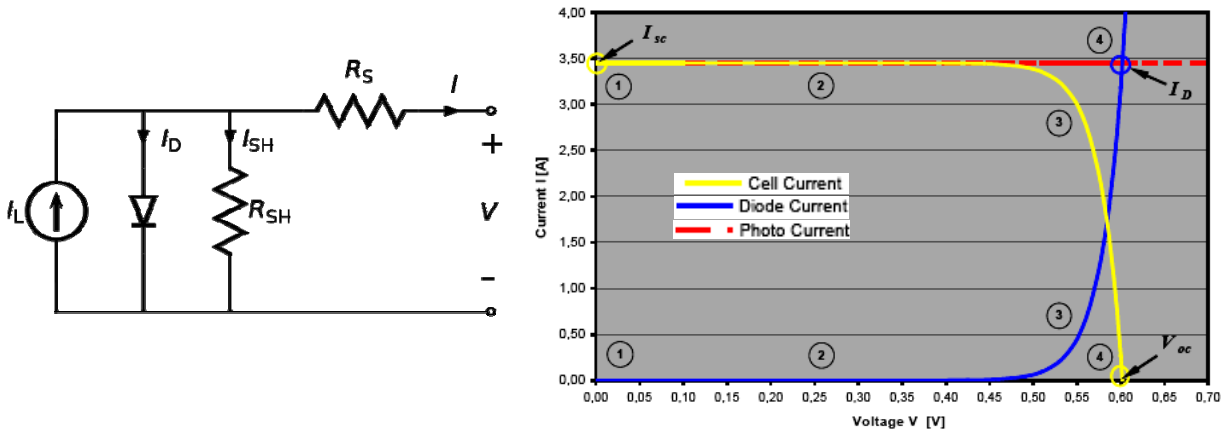


(a)

Material	Conversion efficiency in lab [%]	Conversion efficiency in production [%]
Monocrystalline Silicon	24	14 - 17
Polycrystalline Silicon	18	13 - 15
Amorphous Silicon	13	5 -7

(b)

Fig. 15. Photovoltaic cell efficiency, (a) theoretical maximum at standard conditions, (b) realized values.



(a) (b)

Fig. 16. PV cell (a) equivalent circuit, (b) V-I diagram.

depend upon the cell illumination level. In the ideal case, the I-V characteristic equation is

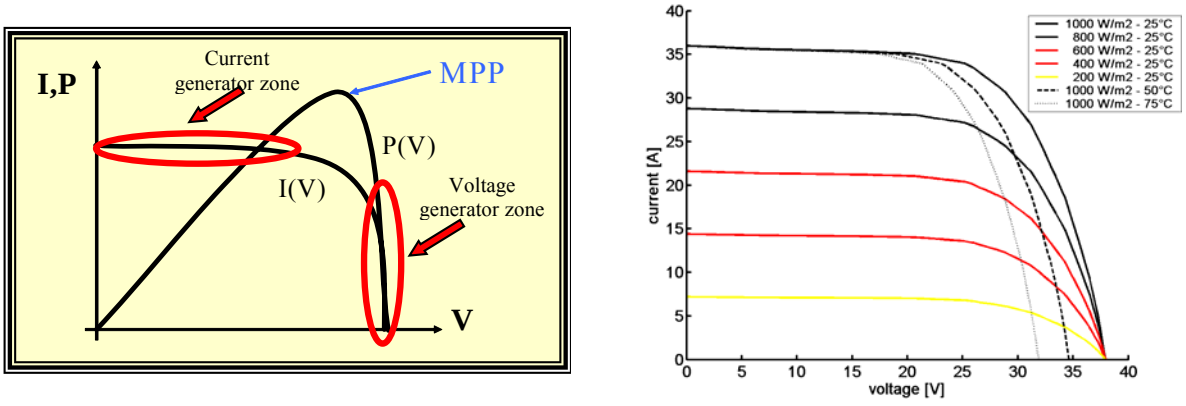
$$I = I_L - I_o(e^{\frac{qV}{kT}} - 1) \tag{3}$$

where I_L is the component of cell current due to photons, q = 1.6x10^{-19} C, k = 1.38·10^{-23} J/K and T is the cell temperature in Kelvin. While the I-V characteristics of actual PV cells differ somewhat from this ideal version, (3) provides a means of determining the ideal performance limits of PV cells. To determine the open circuit voltage of the cell, the cell current is set to zero and (3) is solved for V_{oc}, yielding the result:

$$V_{OC} = \frac{kT}{q}\ln\frac{I_l + I_o}{I_o} \approx \frac{kT}{q}\ln\frac{I_l}{I_o} \tag{4}$$

since normally $I >> I_o$. For example, if the ratio of photocurrent to reverse saturation current is 10^{10}, using a thermal voltage (kT/q) of 26 mV, yields V_{oc} = 0.6 V. Note that the open circuit voltage is only logarithmically dependent on the cell illumination, while the short circuit current is directly proportional to cell illumination.

As a result, there are two different zones, so called "voltage source" and "current source" zone, separated by buffer area conditionally called MPP zone, denoted in Fig. 17(a). Zones are



(a) (b)

Fig. 17. Cell I-V characteristic (a) Two different behaviors of PV cell (panel) separated by MPP zone, (b) irradiation (T = 25°C) for *SP150*.

also called "low impedance" and "high impedance" zone, since dv/di is small in the first one and very high in the second (di/dv→0) (but always negative). Between the two extreme working points with zero output power (short-circuit and no-load), there is a point with the maximum output power, which is often of the outmost interest. The area around that point is highly non-linear, also known as “the knee”. Due to extremely low output voltage, approximately equal to standard diode threshold voltage of 0.6-0.7 V, cells are always connected in series (string) forming a PV module. The data for a different irradiance levels are given for *Shell Solar SP150* module in Fig. 17(b), which will be used for experiments in this work.

1.3. Research objectives and originality of the work

The thesis analyzes a multilevel converter from its structure over modulation up to application in a grid-connected photovoltaic system. The principal objectives of the work were:

1. *To carry out a comprehensive modeling of three-phase multilevel voltage source inverters, with emphasis on cascaded and dual VSIs.*
2. *To investigate characteristics of continuous carrier-based and space vector based pulse width modulators for three-phase dual two-level VSIs, operating in the linear modulation region.*
3. *To examine advantages and shortcomings of both approaches defined above, and establish bi-directional link between carrier-based and space vector pulse width modulators for dual two-level VSIs.*
4. *To develop PWM schemes for dual two-level VSIs (using carrier-based and space vector approach), which are able to produce proper multilevel output voltage applicable to control of three-phase loads and connection to the grid.*
5. *To develop PWM schemes for dual two-level VSIs (using carrier-based and space vector approach), which are able to control the dc-link voltage in accordance with the dual inverter application.*
6. *To explore and develop analytical tools for characterization of the dc-link voltage control methods for dual two-level inverter.*
7. *To design and build dual two-level VSI with accompanying DSP control system for the purpose of experimental verification of results obtained by theoretical and simulation studies.*
8. *To design and build photovoltaic generation system capable of injecting power into the grid and tracking operating point of the maximum power under different environmental conditions.*

By achieving the objectives listed above, a significant body of new knowledge has been produced. This is partially evidenced by the already published research papers that have resulted from the thesis, which can be found within cited references. Chapters four to six contain the original results from the research and therefore represent the main contributions of this work.

1.4. Organization of the thesis

Corresponding to research objectives, the thesis is organized in four major parts that are background, modulation, application and conclusions. More detailed, structure consists of eight chapters, followed by three appendices.

Chapter 1 contains an overview of multilevel power converters. A multilevel topology based on the use of today's mature technology supplied from multiple dc sources is identified as a potentially viable solution for application in the high-power conversion systems. Existing three-phase multilevel power converters are introduced advantages and drawbacks briefly surveyed. Of today's three most exploited configurations, two of them are addressed here, since they are not of the principle interest. A brief introduction of the photovoltaic conversion principles in terrestrial applications is given, with the emphasis on the electrical characteristics of the photovoltaic converter as an electric source. The need for the research conducted within the scope of this thesis is thus established and objectives of the research are finally set forth.

The basic characteristics of the dual two-level inverter VSIs as a multilevel converter of the principle interest are addressed in Chapter 2. First, the configuration is introduced within broader class of cascaded multilevel inverters, showing the performances of the dual inverter with comparison to possible alternatives. The voltage space vectors concept is applied in order to determine the output voltage, with the mapping of switching combinations and the classification of the obtained vectors is given. This foundation is necessary for development of the PWM methods based on the space vector approach. Additionally, modeling aspects of a multi-leg VSI are covered, emphasizing similarities with a three-phase VSI that are used later on for development of the PWM scheme.

The third chapter presents a literature survey in the area of PWM techniques for dual two-level inverter, starting from the basic fundamental frequency methods up to newest space-vector techniques. Due to the differences in dual inverters with double and single dc supply, and having in mind that the emphasis in this thesis is on double-supplied dual inverter, PWM methods applicable to these two configurations are reviewed separately. Additionally, the concept of the power balance of the two sources has been introduced. The chapter also includes a survey of the basic two-level inverter techniques that are the cornerstone for the modulation of dual inverter.

Chapter four deals with development of modulation schemes with power sharing capability for a dual VSI. They use a degree of freedom present at the double-supplied structure to control the two dc powers. Three modulation algorithms are developed based on the utilization of different approaches. It is demonstrated at first that simple extension of well-known principles of a three-phase PWM provides relatively simple yet satisfactorily solution for the dual inverter. Therefore, two CBPWM schemes are introduced, based on the use of discontinuous modulation and composition of the switching periods that are able to generate output voltage without the double simultaneous commutations. Experimental results that are collected from a developed converter prototype show excellent match with predicted theoretical results obtained by means of theoretical analysis and simulations.

A particular dual inverter application as a grid connection converter is treated in Chapter 5. The major issues of such configuration are formulated in the following order: dc-link voltage regulation, current control and synchronization with the grid. Regarding the voltage regulation a two different controllers were proposed. For a current control, a simple proportional controller has been shown as satisfactorily choice with respect to its simplicity. Similarly, a simply yet efficient synchronization solution was implemented. All these aspects were tested separately, provided the possibility to be tuned separately. Finally, a performance of the whole system has been evaluated on the experimental prototype.

The photovoltaic generation application of the dual inverter is presented in Chapter 6. First, a survey on the photovoltaic fields as a source has been presented with practical aspects of their configuration and performance. Another unavoidable aspect of the PV generation is maximum power point tracking that has been briefly surveyed. A new method particularly suitable for the dual inverter configuration has been presented with both the simulation and experimental results obtained. Experimental results are presented, confirming theoretical findings.

Chapter 7 provides conclusions and a summary of the thesis, highlighting the most important findings from each chapter. Guidelines for future research are also given. References are listed at the end of each chapter. The numbered structures (sections, equations, figures, tables, reference) are referred inside the same chapter with ordinal number only (e.g. Fig. 15), and outside its chapter with the leading number of the chapter (e.g. Fig 2.15 denotes Fig. 15 in the second chapter).

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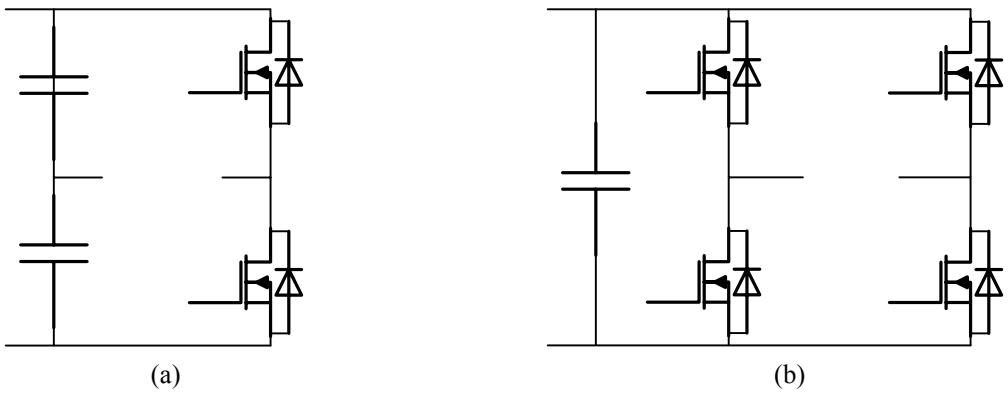
2. Dual inverter configuration

Cascaded converter, together with the described diode clamped and capacitor clamped converters, makes the three most common types of present multilevel topologies [1], [2]. In fact, the series H-bridge design was a forerunner of the whole multilevel family, proposed more than 30 years ago [3]. It still receives large attention among these topologies, due to the simplicity of the power stage not requiring additional components such as diodes and capacitors. As cascaded inverters here is considered broader group of converters having a common "open-end" load connection, i.e. both terminals of the load are connected to the converter. This is illustrated in Fig. 1 by showing single-phase inverters: half-bridge with center tap and full-bridge, both representing the cascaded principle. The main cascaded multilevel inverter configurations are

- cascaded H bridge inverters,
- cascaded three-phase inverters,
- dual two-level inverters,

and they will be described in the following sections with the emphasis on the last one. This chapter mostly discusses the topology issues, whereas the modulation and control topics are to be addressed in the chapters to come.

The complexity of both leg hardware and control algorithm sharply increases with the number of levels, as was presented in the previous chapter. This drawback lead to a development of the cascaded topology, providing the same number of output voltage levels using two yet simpler multilevel inverters instead of one complex inverter with large number of leg levels. Considering two n_2-level inverters connected "in opposition" at two ends of the load, it will be shown that the obtained structure can produce $p_2 = 8n_2\text{-}7$ different phase voltage levels of output voltage. Simultaneously, three-phase inverter consisting of n_1-level legs provides $p_1 = 4n_1\text{-}3$ different phase voltage levels (including zero) for a star-connected load. Therefore, for n_1 less than n_2 the same multilevel output number of levels $p_2 = p_1$ can be reached. Moreover, having two inverters with an appropriated control strategy it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability [4], [5].



(a) (b)

Fig. 1. Cascaded H-bridge cells (a) half-bridge, (b) full-bridge.

2.1. An overview of cascaded multilevel inverters

2.1.1. Cascaded H-bridge

The idea to cascade (connect in series) single-phase full-bridges was the most natural solution and the first proposed one [3]. Indeed, it is a literal realization of the multilevel principle: each switch works inside its on "module" (here H-bridge), contributing to the total output under limited reverse voltage. The principle can be easily understood with reference to Fig. 2(a) where each H-bridge forms a phase leg for a three-level inverter with the levels $+V_{dc}$, 0 and $-V_{dc}$. The number l of "leg" output voltage levels for N such cascaded converters become:

$$l = 2N + 1, \tag{1}$$

from $-NV_{dc}$ to NV_{dc} and including zero voltage. It can be noted that the number of switching levels is always odd (unlike diode-clamped), since inserting additional H-bridge to each phase leg adds two new levels. For a star-connected load it can be shown that these l leg levels will produce p output voltage levels where

$$p = 2 \cdot 2(l-1) + 1 = 4l - 3, \tag{2}$$

An important advantage of the converter is modularity that can be clearly noted comparing Figs. 2(a) and 2(b).

The dc link supply for each full-bridge converter element must be provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer Fig. 3(a). It can be shown that by progressive phase shifting of the three-phase secondary windings significant harmonic cancellation of the transformer input current can be achieved. However, for single-phase rectifiers this task is more complex [6], since they require connection in groups of three. Another possible solution is in photovoltaic applications [7], [8] as

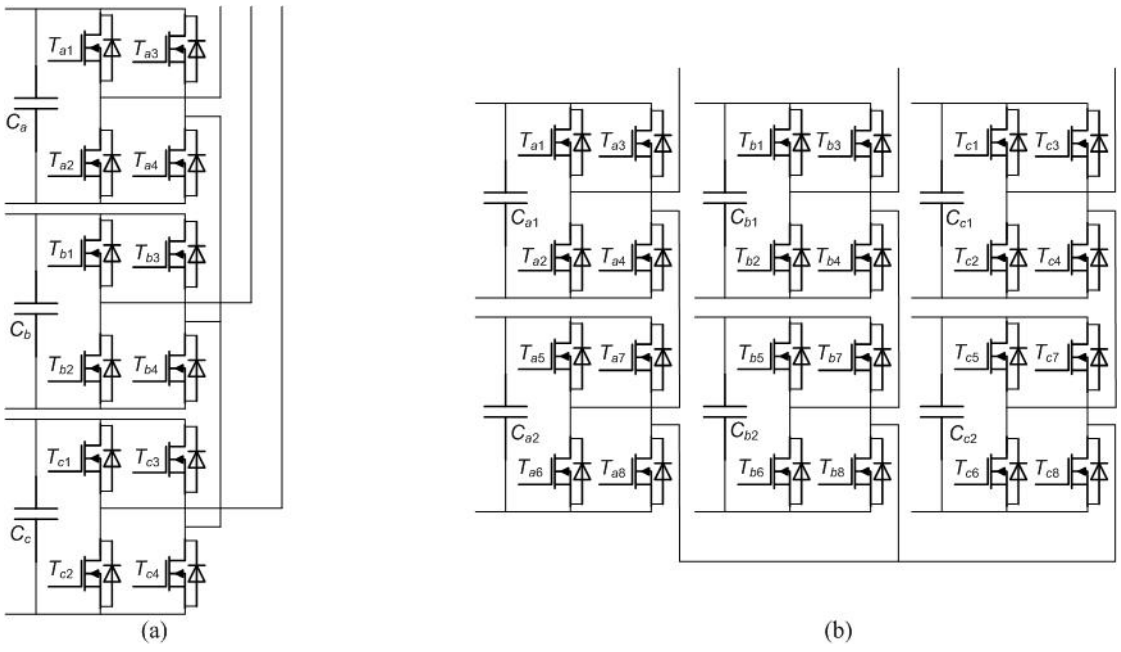
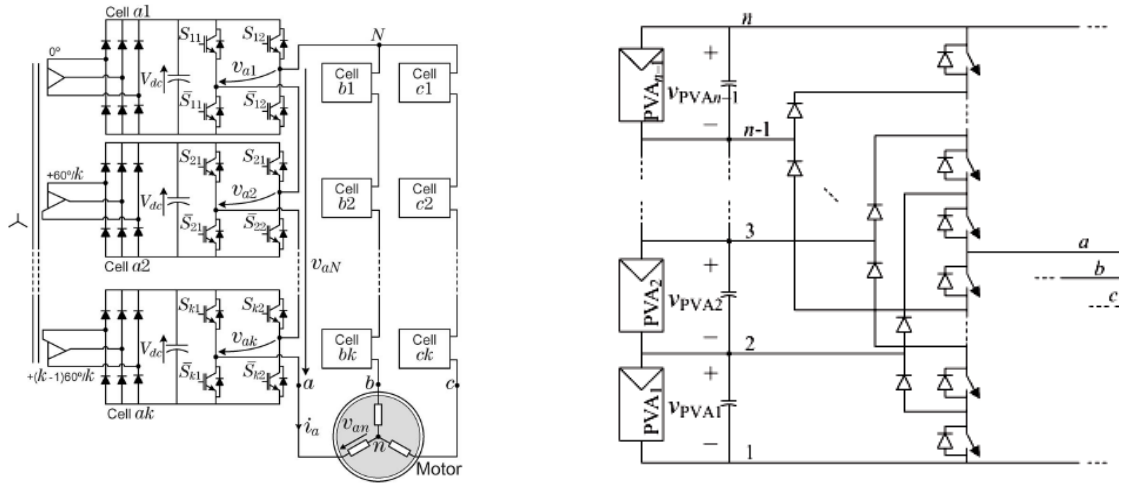


Fig. 2. Three-phase cascaded H-bridge inverter (a) three-level (b) five-level.



(a) (b)

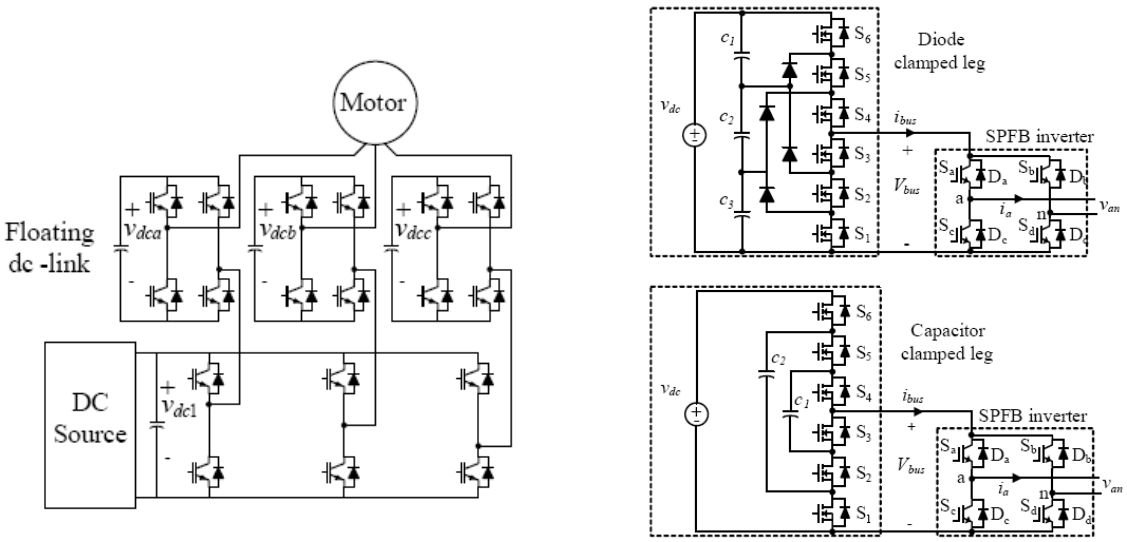
Fig. 3. Power supply for cascaded H-bridge with (a) grid supply, (b) PV supply.

shown in Fig. 3(b); however, it is highly impractical to have such a large number of connection cables. A particularly convenient application is STATCOM and active power filters, where injection of active power is not required, so the dc voltages can be floating and adjusted to the reference by the control strategy.

In contrast to the diode-clamped and flying-capacitor inverters, where individual phase legs must be modulated by a central controller, an advantage of the cascaded structure of the full-bridge inverters is independence of each other, only the synchronization of reference and carrier waveforms for different phase legs is required. This makes for a simpler controller structure than for either of the two previously discussed topologies. On the other hand, the price is paid by higher number and larger values of the capacitors required since the power flow for each source possess a strong oscillatory component due to its single-phase configuration. Additional advantage is a possibility to load equally all switches of the converter, in contrast to previous two configurations described in Chapter 1. Last but not least, an significant difference is an intrinsic balancing of the capacitor voltages done by the each dc source. This is not the case for the diode-clamped or capacitor clamped inverters where dc link capacitors can be over or undercharged depending of the average current [9].

Many of the hybrid multilevel inverters employ H-bridges, as introduced in the paragraph 1.1.3. The topology shown in Fig. 4(a), with a two-level or NPC converter in series with a floating single-phase inverter floating dc-sources [10], offers an optimum tradeoff between output quality, reliability and efficiency. Recently, the use of a multilevel dc-link voltage has been studied in order to increase the number of total output voltage levels using only a few single-phase inverters. The topology is based on a variable dc-link which could have from zero to several voltage levels, then a single-phase full bridge (SPFB) inverter could applies this voltage or its negative [11]. In described configuration, each cascaded inverter cell had the same dc-link voltage value and contributed equally to the total output voltage.

Furthermore, by choosing different dc-link voltages for given number of cells it is possible to increase the number of output voltage levels. This method is called asymmetric cascaded inverter in the literature, and requires binary (power of two) or trinary (power of three) relationship



(a) (b)

Fig. 4. Hybrid cascaded topologies with (a) floating dc-link, (b) variable multilevel dc-link voltage diode/capacitor clamped.

among the dc-link voltages to provide equal steps of output voltage waveform [10]. By sum\difference of binary potentials can be reached all numbers up to next potential since

$$2^{N-1} + 2^{N-2} + \ldots + 1 = 2^N - 1, \tag{3}$$

so all natural numbers are covered even with redundancy (e.g. $2^2 = 2^3 - 2^2$). In analogous manner can be covered all natural number within interval by sum\difference of potentials of three, but there is no redundancy since the sum reaches exactly up to the "complement of the sum":

$$3^{N-1} + 3^{N-2} + \ldots + 1 = \frac{3^N - 1}{2} = 3^N - \frac{3^N + 1}{2} \tag{4}$$

The number of leg voltages levels for N such "binary" inverters will be

$$l = 2 \cdot (2^{N-1} + 2^{N-2} + \ldots + 1) + 1 = 2^{N+1} - 1, \tag{5}$$

since the maximum leg voltage is achieved by the sum of all cell voltages. Analogously

$$p = 2 \cdot (1 + 3 + \ldots + 3^{N-1}) + 1 = 2\frac{3^N - 1}{3 - 1} + 1 = 3^N, \tag{6}$$

It can be easily seen that for n higher than three geometrical progressions n^N increase too fast and cannot be "reached" by the sum of its previous members.

2.1.2. Cascaded two-level inverter

Instead of cascading H-bridges, it is possible to apply similar idea to two-level inverters, as was proposed in [12]. The obtained structure is depicted in Fig. 5(a), consisting of one standard two-level inverter (ABC) and another slightly modified (DEF, positive dc busbar removed). The structure provides three-level output by simple switching of upper, middle and lower switches, as stated in Tab. 1. The simple and scalable structure for arbitrary number of levels is the main advantage of the proposed topology. The biggest drawback of the scheme is that the lowest switches (T_{a4}, T_{b4}, and T_{c4} in Fig. 5(a), belonging to the inverter with non-standard layout) have

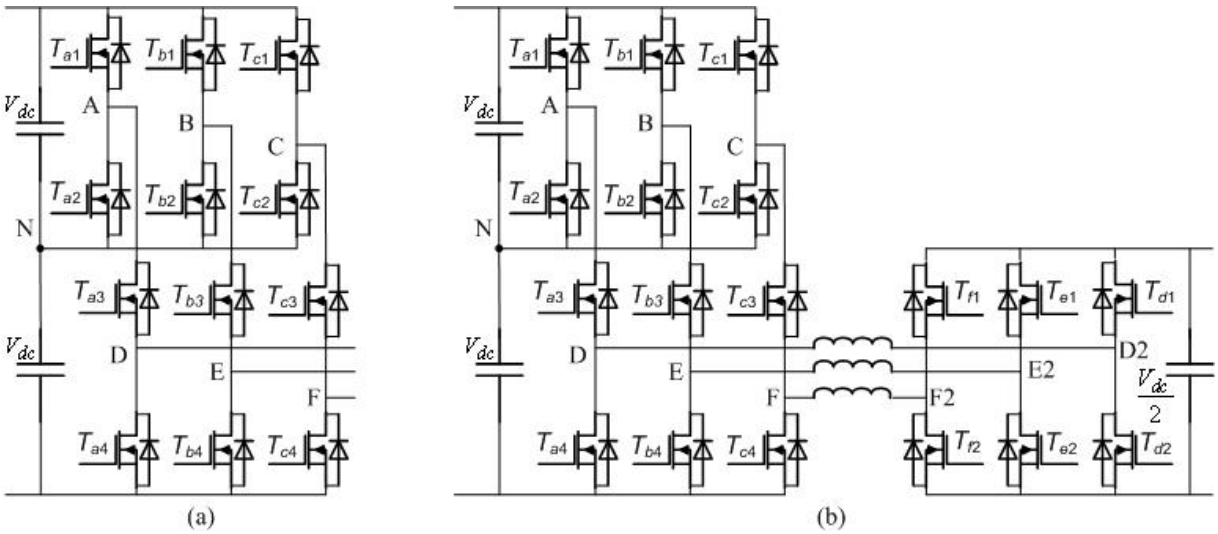


Fig. 5. Cascaded three-phase three-level inverter: (a) converter, (b) five-level application.

to withstand the whole dc voltage (i.e. $2V_{dc}$). Another drawback common for clamped inverters is the asymmetry of the inner and outer switches conducting currents.

The Authors [13] applied cascaded two-level inverter in a more complex topology presented in Fig. 5(b). In order to be distinguished from cascaded inverters this kind of structure with two converters connected "in opposition" between an open-winding load will be further called dual inverter. The open winding load is standard three-phase load with six available terminals, in contrast to usual delta and star connections with three (eventually four) output terminals. In this case, the dual inverter is both hybrid and asymmetrical: not only are that two inverters with different number of levels, but also with different dc voltages in ratio 4:1. This is in concordance with the analysis in Subsection 1, since three level inverter provides 4:2 ratio, therefore all steps from V_{dc} to $5V_{dc}$ are obtainable. As a result, the dual inverter is equivalent to six-level converter, therefore increasing the number of leg voltages more than a simple sum 3+2.

Tab. 1. Switching states and leg output voltages for three-level cascaded inverter.

	State of the switches				3-level
Value	T_{a1}	T_{a2}	T_{a3}	T_{a4}	Leg voltage
	1	0	1	0	V_{dc}
	0	1	1	0	*0*
	0	0	0	1	$-V_{dc}$

2.1.3. Dual inverter structure

Considering dual inverter formed by two identical inverters with *l* leg voltage levels and using (2) gives the number of the different output voltage levels *d* (including zero level):

$$d = 2(4n-3)-1 = 8n-7\,. \tag{7}$$

The two inverters are connected "in opposition" at two ends of the load in order to obtain output voltage as a difference of inverter's leg potentials as shown in Fig. 5(b). The result, when compared to (2) shows that in order to reach given number of output voltage levels it is more convenient to apply two simpler *n*-level inverters in dual configuration that one large *l*-level

inverter since the complexity of both the leg hardware and modulation/control algorithms sharply increases with the number of levels. Comparing (7) with (2) gives

$$l = 2n - 1 >> n \,. \tag{8}$$

which is significant reduction compared to n.

A particularly convenient case is obtained for n equal two, which gives multilevel output equivalent to three-level inverter by using standard readily available two-level inverters, avoiding multilevel structure. A possible development path for this solution is illustrated in Fig. 6, starting from the simplest cascaded H-bridge (a), over "double inverter" (b) towards dual two-level inverters with common (c) and isolated (d) dc-supplies. It means that the converter can be considered as derived from the cascaded H-bridge from a structural point of view.

Historically, dual inverter was proposed twenty years ago for high-power drive application [14]. Curiously, the authors did not entered into details of the new topology, paying more attention to the direct-torque control being a pioneering technique at the time. Few years later, a first open-loop modulation technique was presented, and the equivalence with the three-level inverters output was established [15]. However, a whole decade passed before a comprehensive analysis of dual inverter and its counterparts came out [16]. It is worth nothing that no immediate terminology agreement has been set: the inventors called it "dual three-phase inverter", whereas [16] and [17] diverted from this terminology by using term "cascaded", which actually corresponds to others topologies as previously explained.

A. Comparison between dual and standard two-level

The first justification of the dual inverter topology comes in comparison with standard two-level inverter [18]. The standard inverter topology (Fig. 7) for a given dc-bus voltage V_{dc} can produce a phase-to-star-point RMS voltage:

$$V = \frac{1}{\sqrt{2}}\left(\frac{\sqrt{3}}{2}\cdot\frac{2}{3}V_{dc}\right) = \frac{V_{dc}}{\sqrt{2}\sqrt{3}} = 0{,}408\,V_{dc}\,. \tag{9}$$

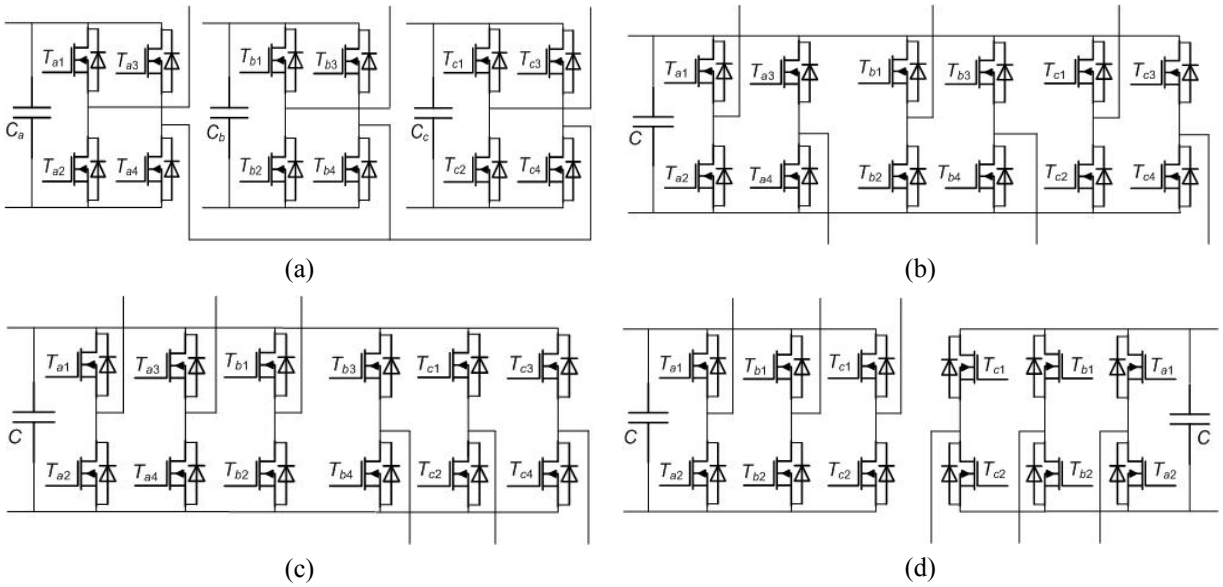


Fig. 6. "Evolution" from cascaded to dual inverter (a) cascaded H-bridge with a star connection and 3 insulated dc supply, (b) cascaded H-bridge with open-end winding and single dc supply, (c) simple redraw equivalent to point b, (d) proposed dual-inverter configuration obtained from point c (or b) by splitting the dc supply.

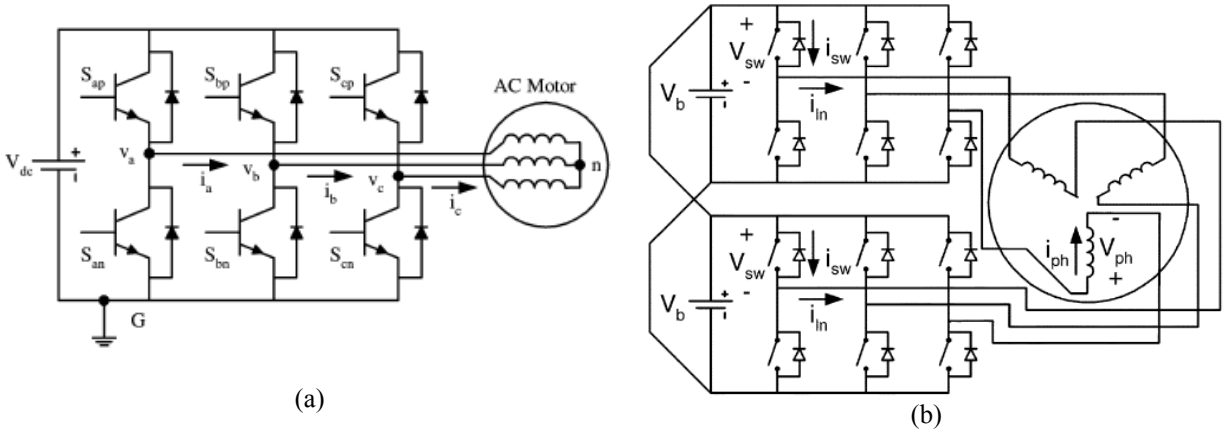


Fig. 7. Inverters comparison (a) standard two-level, (b) dual with a common dc-source.

while the switches rated reverse voltage has to be:

$$V_{sw} = V_{dc}\,. \tag{10}$$

Similarly, if inverter output current is equal to RMS value I, the current rating of the switch should be the peak value:

$$I_{sw} = \sqrt{2}I\,. \tag{11}$$

The cost of the switches for the converter is not determined only by their number, but also by their voltage and current ratings determining the power level. Switch utility ratio [19] is a quantitative factor of converters switches utilization obtained as a ratio between converter output power S_c and sum of switches power:

$$SUR = \frac{S_c}{N \cdot V_{sw} I_{sw}} = \frac{3VI}{6V_{sw} I_{sw}} = \frac{3 \cdot 0.408 V_{dc} \cdot I}{6V_{dc} \cdot \sqrt{2} I_{ph}} = 0.144. \tag{12}$$

A similar switching factor is defined in [20]. Here should be noted that switches peak current cannot be provided continuously, therefore the proper factor should take into account continuous current rating:

$$SUR = \frac{S_c}{N \cdot V_{sw} I_{sw}} = \frac{3VI}{6V_{sw} I_{sw}} = \frac{3 \cdot 0.408 V_{dc} \cdot I}{6V_{dc} I} = 0.204. \tag{13}$$

However, the difference is only in absolute values, the relations remain the same as if peak current would be considered. Moreover, due to the physical reasons switches peak and continuous current ratings are usually proportional.

In case of dual inverter feed by two sources with equal voltage V_{dc} each, the calculations made analogously manner show:

$$SUR = \frac{S_c}{N \cdot V_{sw} I_{sw}} = \frac{3VI}{12V_{sw} \cdot I_{sw}} = \frac{3 \cdot 0.408 \cdot 2V_{dc} \cdot I}{12V_{dc} \cdot I} = 0.204. \tag{14}$$

The same conclusion is obtained by using other indicators in [16] One can observe that dual structure possesses no advantage in comparison to standard inverter in terms of the number of switches. They are just arranged in a different manner: indeed many paralleled mosfets are typically used to achieve required current rating. The benefit of dual inverter arises from the fact that use of components with lower voltage ratings enables bigger efficiency, since the mosfet's

on-state resistance is a strong function of the blocking voltage rating V_{DSS}. This explains why MOSFET is an excellent choice in low-voltage applications (bellow 200 V). The same power rating can be obtained by using single three-phase inverter with parallel switches, but this solution has few disadvantages:

- The output current is doubled, which makes problems with load windings, losses and connections,
- Paralleling switches adds additional problems, such are difficult current protection, different driver circuits, unsymmetrical current sharing.

B. Comparison between diode-clamped and dual three-level inverter

Same number of the transistors, but DCI has additional two diodes per each phase (six in total)

- For the same output voltage DCI requires double input in respect to dual inverter
- For single supply, neutral point of the DCI can be balanced by additional capacitors. Dual inverter does not need that.
- For the same input supply voltage and transistors ratings rated power of the DCI is half of the rated power of the dual inverter

Power supply dualism

- For two separate power supplies NPC does not need voltage balancing of the neutral point, in the same manner that dual inverter doesn't need to eliminate zero-sequence current.
- For single supply, neutral point of the NPC can be balanced by appropriate voltage vectors and capacitors. Similarly, for the dual inverter with a single supply zero-sequence component can be eliminated by choosing appropriate vectors, with the price of lower output voltage.

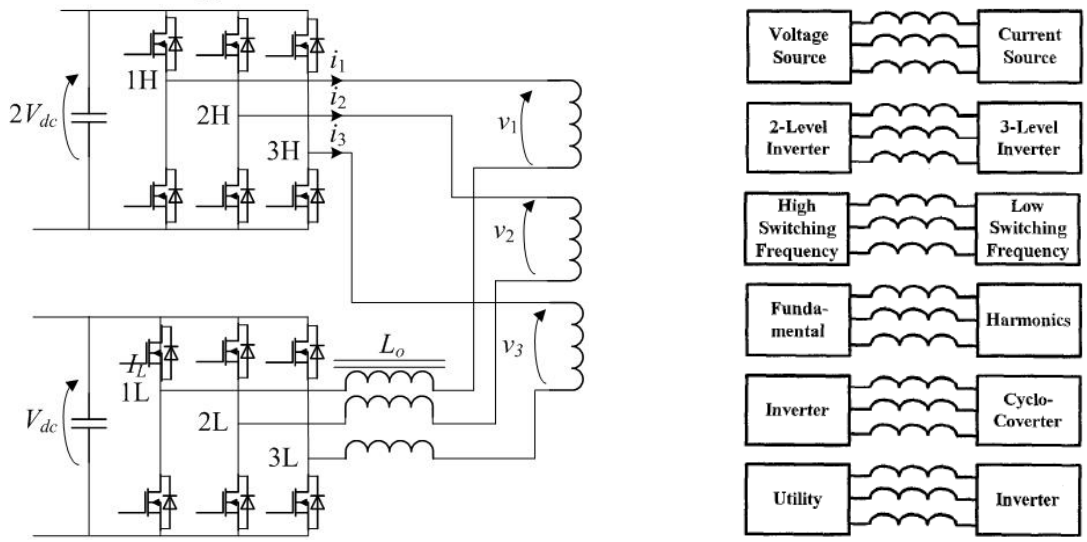
C. Comparison between cascaded and dual three-level inverter

Compared to cascaded multilevel inverters discussed in this chapter, dual inverter

- The cascaded H-bridge configuration Fig. 2 is scalable and easy to realize, but has the disadvantage of multiple insulated dc sources (three for the 3-level version) with oscillating power from each source (each H bridge behaves as single-phase inverter);
- The cascaded three-phase inverter configuration Fig. 5 reduces the number of dc power supplies and avoids the need of galvanic insulation. It is a scalable structure, but the bottom inverter has not a standard connection layout and all its switches must be rated with the full dc voltage;
- The dual inverter configuration Fig. 8(a) consists in the simple connection of two standard 2-level inverters to a three-phase open-winding load, and performs as a 3-level inverter. Although it is not scalable to get more voltage levels, it represents a viable solution to supply transformers and ac motors, especially when the dc source can be easily split in two insulated parts, as for batteries and PV panels. This is the structure considered in the following.

D. Asymmetrical dual inverters

As already noted two inverters forming the dual converter in general do not have to be necessary equal [21]. There can be different combinations of the two inverters, as illustrated Fig.



(a) (b)

Fig. 8. Dual multilevel inverter (a) with two equal two-level inverters, (b) with two different inverters.

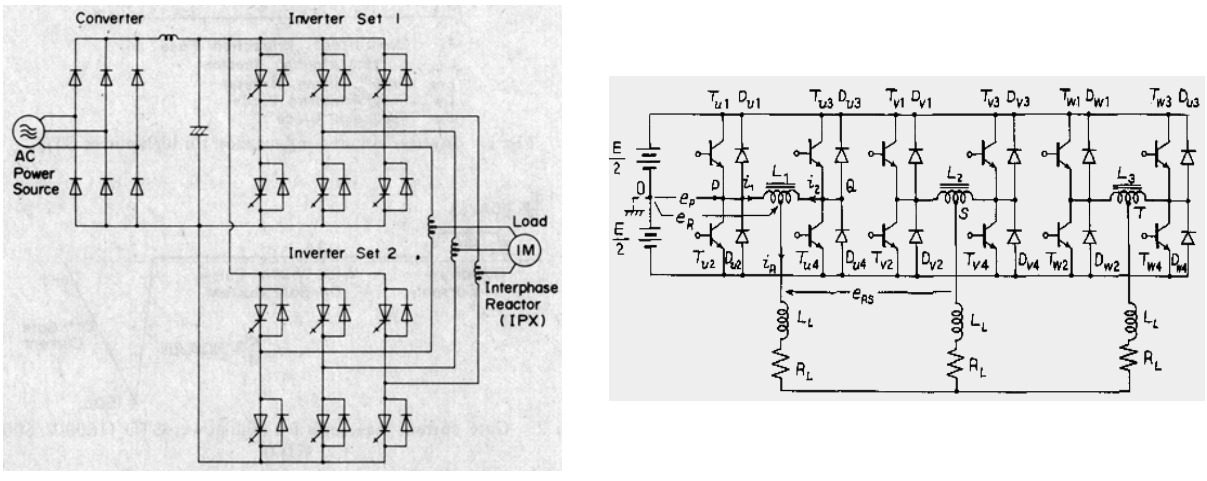
8(b), satisfying a minimal limitation such is that two current source inverters cannot form dual inverter.

E. Fault tolerance

The use of dual inverter can be considered in applications where fault tolerance is required. It has the smallest cost penalty factor compared to standard configurations, and provides fault tolerance to open phase faults [22]. With the addition of triac switch in each phase, this system is fault tolerant to single switch open, short faults, and single-phase open-circuits.

2.1.4. Parallel inverters

Parallel inverters are sometimes considered as multilevel inverters due to the some misunderstandings present in the literature. For this reason, although not a multilevel inverter, this topology will be briefly analyzed here. Another important motive is to illustrate different approach in high power converter design: augmenting current instead of voltage capability. Originally, it was proposed in order to avoid the problems with parallel connection of gate-



(a) (b)

Fig. 9. Parallel inverters connection realized with (a) thyristors, (b) transistors.

thyristor off (GTO) switches [23], introducing benefits regarding their current and voltage snubber circuits. The quite simple idea is depicted in Fig. 9(a), with two standard two-level inverters connected in parallel by additional inductances called “inter-phase reactors”. The inter-phase reactors have large losses and high acoustic noise, and in addition they are bulky and expensive [21].

With parallel connection of inverter through inter-phase reactors, the semiconductors must block the entire voltage, but share the load current. However much later Authors [24] claimed that the voltage output has multilevel waveform equivalent to three-level inverter, which is false. Shortly after the similar statement has been published in [25], depicted in shown in Fig. 9(b), and erroneously cited in [26]. If true, it would mean that converter gains both voltage and current, which is not possible by use of only two two-level inverters. The brief calculation in the next section will show that the output is identical as two-level inverter.

2.2. Calculation of the output voltage

For standard two-level three-phase inverter with star-connected load the relation between the phase voltages and leg states can be obtained using:

$$\begin{aligned} v_{AS} &= v_{AN} + v_{NS}, \\ v_{BS} &= v_{BN} + v_{NS}, \\ v_{CS} &= v_{CN} + v_{NS}, \end{aligned} \tag{15}$$

where "N" is negative pole of the dc link and "S" is the star point of the load, as shown in Fig. 10 for the two-level inverter. Note that voltage v_{AN}, v_{BN}, v_{CN} can take either value V_{DC} or 0. Presuming balanced load and isolated star point yields that there is no zero-sequence component of load voltage:

$$v_{AS} + v_{BS} + v_{CS} = 0. \tag{16}$$

In contrast to this case, unbalanced load inherently contains zero-sequence voltage component independently from the connection of the star point. Equation (16) provides a temporary result:

$$v_{SN} = (v_{AN} + v_{BN} + v_{CN})/3, \tag{17}$$

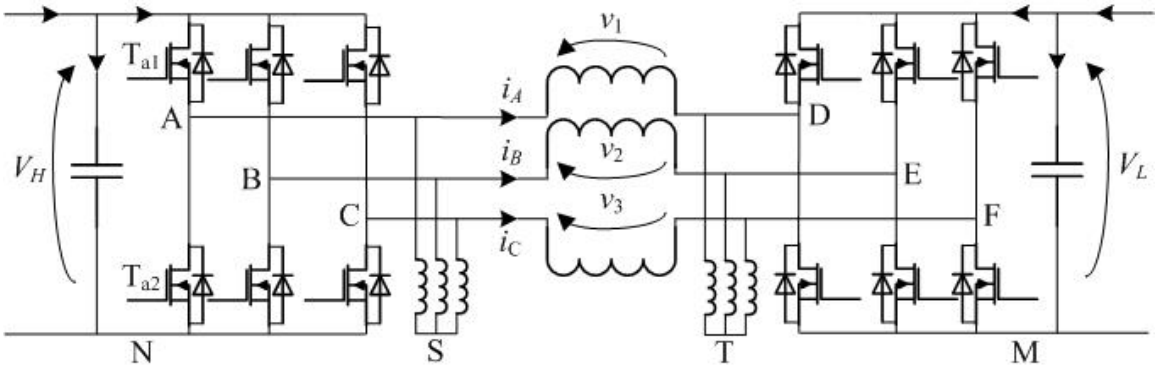


Fig. 10. Dual two-level inverter with artificial star points.

that gives output voltage expression:

$$\begin{aligned} v_{AS} &= (2v_{AN} - v_{BN} - v_{CN})/3 = V_{dc}(2S_A - S_B - S_C)/3, \\ v_{BS} &= (-v_{AN} + 2v_{BN} - v_{CN})/3 = V_{dc}(-S_A + 2S_B - S_C)/3, \\ v_{CS} &= (-v_{AN} - v_{BN} + 2v_{CN})/3 = V_{dc}(-S_A - S_B + 2S_C)/3, \end{aligned} \tag{18}$$

where $S_X \in \{0, 1\}$ are switching states of "leg voltages. Note that

$$v_{AS} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \end{bmatrix} \begin{bmatrix} v_{AN} & v_{BN} & v_{CN} \end{bmatrix}^t = v_\alpha, \tag{19}$$

is α-component of Clarke transform of leg voltages.

Applying analogous calculation for the dual inverter output voltages:

$$\begin{aligned} v_{AD} &= v_{AN} - v_{DM} + v_{NM}, \\ v_{BE} &= v_{BN} - v_{EM} + v_{NM}, \\ v_{CF} &= v_{CN} - v_{FM} + v_{NM}, \end{aligned} \tag{20}$$

with denotations in Fig. 10. With the presumption of no zero-sequence component:

$$v_{AD} + v_{BE} + v_{CF} = 0, \tag{21}$$

an intermediate result can be obtained:

$$v_{MN} = (v_{AN} + v_{BN} + v_{CN})/3 - (v_{DM} + v_{EM} + v_{FM})/3, \tag{22}$$

leading to the final result for output voltage [16]:

$$\begin{aligned} v_{AD} &= (2(v_{AN} - v_{DM}) - (v_{BN} - v_{EM}) - (v_{CN} - v_{FM}))/3, \\ v_{BE} &= (-(v_{AN} - v_{DM}) + 2(v_{BN} - v_{EM}) - (v_{CN} - v_{FM}))/3, \\ v_{CF} &= (-(v_{AN} - v_{DM}) - (v_{BN} - v_{EM}) + 2(v_{CN} - v_{FM}))/3. \end{aligned} \tag{23}$$

There can be two interpretations of (23) how dual inverter output voltage can be treated, also depicted in Fig. 11(a):

- As three single-phase choppers, based on similarity with (18):

$$\begin{aligned} v_{AD} &= (2v_{1S} - v_{2S} - v_{3S})/3, \\ v_{BE} &= (-v_{1S} + 2v_{2S} - v_{3S})/3, \\ v_{CF} &= (-v_{1S} - v_{2S} + 2v_{3S})/3. \end{aligned} \tag{24}$$

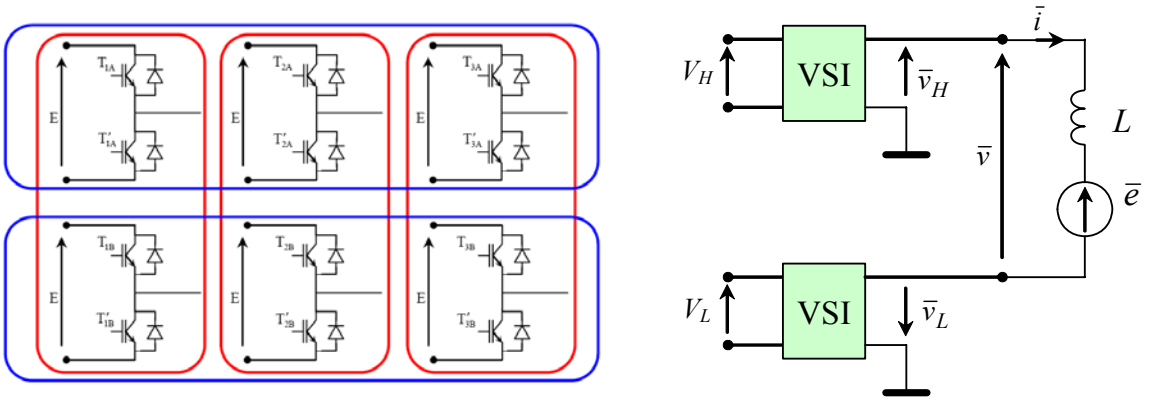
where

$$\begin{aligned} v_{1S} &= v_{AN} - v_{DM}, \\ v_{2S} &= v_{BN} - v_{EM}, \\ v_{3S} &= v_{CN} - v_{FM}. \end{aligned} \tag{25}$$

are composite duty cycles obtained as a difference of two duty cycles (“S” stays for imaginary common star point). This approach makes dual inverter analogue to standard three-phase case, the only difference are composite duty cycles. Typical example is level-shifted carrier-based modulation discussed in the next chapter.

- As two three-phase inverters, since (23) can be regrouped as:

$$\begin{aligned} v_{AD} &= (2v_{AN} - v_{BN} - v_{CN})/3 - (2v_{DM} - v_{EM} - v_{FM})/3, \\ v_{BE} &= (-v_{AN} + 2v_{BN} - v_{CN})/3 - (-v_{DM} + 2v_{BN} - v_{EM})/3, \\ v_{CF} &= (-v_{AN} - v_{BN} + 2v_{CN})/3 - (-v_{DM} - v_{EM} + 2v_{FM}))/3. \end{aligned} \tag{26}$$



(a) (b)

Fig. 11. Dual inverter (a) equivalent scheme (b) illustration of two different approaches the three H-bridges (vertical lines) or the two three-phase inverters (horizontal lines).

where v_{AS}, v_{BS}, v_{CS}, and v_{AT}, v_{BT}, v_{CT} are phase-to-star point voltages of inverters H and L respectively, according analogy with (18),

$$\begin{aligned} v_{AD} &= v_{AS} - v_{DT}\,, \\ v_{BE} &= v_{BS} - v_{ET}\,, \\ v_{CF} &= v_{CS} - v_{FT}\,. \end{aligned} \tag{27}$$

and these star points are imaginary, virtual. As a possible interpretation, it can be stated that since sum of output currents is zero, each inverter creates "virtual star point" for the other one.

This result is very important - dual inverter, which is inherently complex, is referred to case of two independent single inverters in Fig. 11(b), for whom many developed methods exist. Nevertheless, it should be noted that the conclusions are only formal, not related to any real physical star point, neither the star points of their star loads are equipotential. Once more, it should be emphasized careful that this is not stated for single v_{AN}, v_{DM} voltages i.e.

$$v_{AD} \neq v_{AN} - v_{DM}\,. \tag{28}$$

2.2.1. Output voltages in the terms of inverters line-to-line voltages

Since phase-to-neutral voltages are not available in contrast to line-to-line voltages v_{AB}, v_{BC}, v_{DE}, v_{EF} of single inverters it is more practical to use them to calculate output (load) voltage

$$\begin{aligned} v_{AD} + v_{DE} &= v_{AB} + v_{BE}\,, \\ v_{BE} + v_{EF} &= v_{BC} + v_{CF} \end{aligned} \tag{29}$$

Expressing voltages of interest:

$$\begin{aligned} v_{AD} - v_{BE} &= v_{AB} - v_{DE}\,, \\ v_{BE} - v_{CF} &= v_{BC} - v_{EF} \end{aligned} \tag{30}$$

Subtracting two equations and supposing the presumption (21) gives:

$$\begin{aligned} v_{AD} - 2v_{BE} + v_{CF} &= -3v_{BE} = v_{AB} - v_{DE} - v_{BC} + v_{EF}\,, \\ v_{BE} &= ((v_{BC} - v_{EF}) - (v_{AB} - v_{DE}))/3 \end{aligned} \tag{31}$$

Analogously can be the complete result:

$$\begin{aligned} v_{AD} &= ((v_{AB} - v_{DE}) - (v_{CA} - v_{FD}))/3, \\ v_{BE} &= ((v_{BC} - v_{EF}) - (v_{AB} - v_{DE}))/3 \\ v_{CF} &= ((v_{CA} - v_{FD}) - (v_{BC} - v_{EF}))/3 \end{aligned} \tag{32}$$

This method can be preferred way for output voltage measurement since it avoids electromagnetic interferences, as will be explained later. However, it is quite impractical since requires measurement and arithmetical operation with four voltages simultaneous, which is a demanding task.

2.2.2. Dead time effect

Dead time is a necessary blanking interval (pause) between the turn-on signals for two legs switches in voltage source inverter (T_{a1} and T_{a2} in Fig. 10), due to their serial connection. Therefore, deadtime T_b is introduced at each commutation (change of the leg output as the switch previously on is turning off and vice versa). Although is often neglected in the global analysis of inverters output, it significant influences output voltage due to a parasitic effect of this interval which makes nonlinear and distorted [27]. Huge efforts have been exerted to resolve this problem [28], [29]. A consequence of the deadtime is delay of the leading edge of the pulse (i.e. positive slope), whereas the trailing edge remains unchanged. Only in the two boundary cases when duty cycles are 100 % and 0 % the deadtime interval does not exist since there is no need for commutation.

Behavior of the command signals is illustrated in Fig. 12(a) where trace 2 (upper) shows commanded duration of pulse at switching period T_s = 50 μs, T_d = 1.28 μs for duty cycle d = 4% (t_d^* = 2 μs). The leading edge is delayed for value of T_d whereas the trailing edge is unaffected. The same can be seen on Fig. 12(b), for d = 96% (t_d^* = 48 μs). It may look that command signal is simply delayed for T_d, and pulse can be compensated for this amount at the trailing edge. However, this is not the case since antiparallel diodes are also commutating during the deadtime interval but in an uncontrollable manner. The state of the two diodes depends on the leg current sense [27]. Therefore, the loss of the duty cycle shown in Fig. 12 requires compensation that is more complex, instead of a simple extension of the trailing edge it has to take into account also sense of the current.

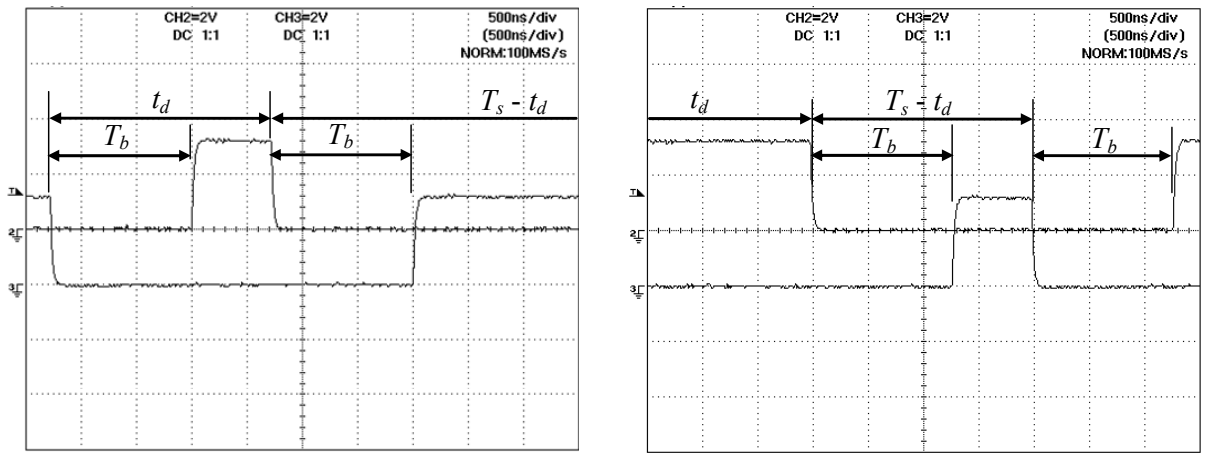
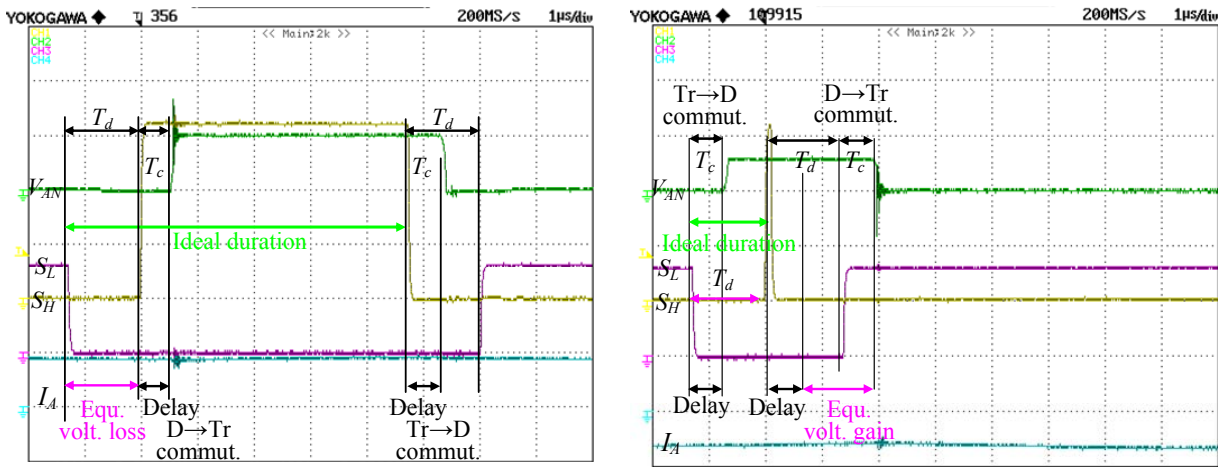


Fig. 12. Dead time effect (T_d = 1.28 μs, T_s = 50 μs) on duty cycle duration (a) 4 % (t_d = 2 μs), (b) 96 % (t_d = 48 μs).



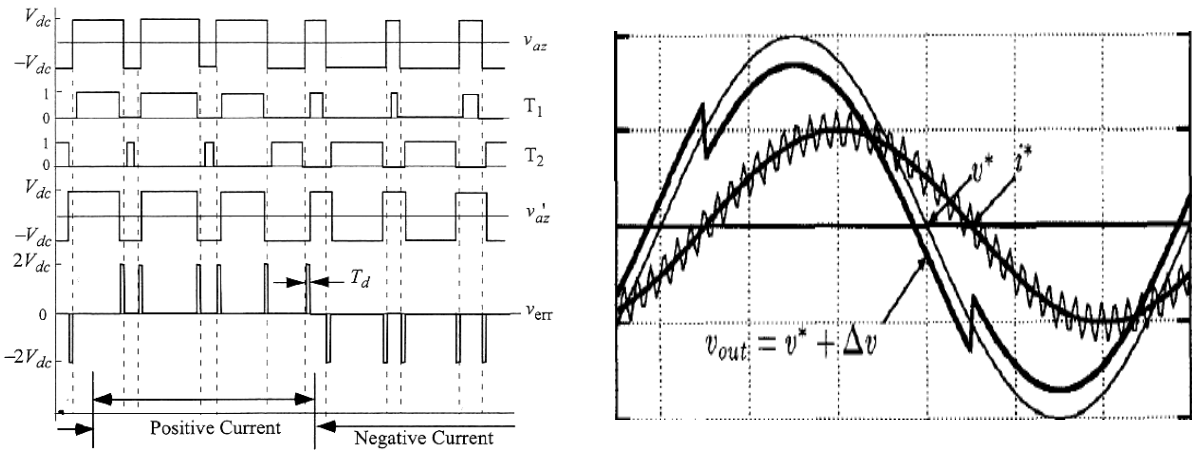
(a) (b)

Fig. 13. Consequences of the dead time effect depending on the leg current (a) positive and (b) negative sense.

The total deadtime effect is voltage loss or gain, depending on the sense of the current, as illustrated in Fig. 13. For the positive current leading edge loss remains uncompensated by trailing edge diode conduction, whereas for negative sense trailing edge becomes "overcompensated". The two cases are

- Positive current: When lower switch turns off there is a dead time (1.28 µs) which does not affect output voltage. It can be seen that the turn-on time of mosfet and the turn-off time of the mosfet plus turn-on time of the diode are approximately equal.
- Negative current: When lower switch turns off there is a dead time (1.28 µs) which affects output voltage significantly. First, there is a delay due to upper diode turn-on time. Since it is less than deadtime there is a voltage gain. Then, after the upper mosfet finishes its duty and turns off, upper diode remains on for deadtime and lower mosfet turn-on time.

The overall effect to the voltage pulses is illustrated in Fig. 14(a), and to the voltage fundamental harmonic in Fig. 14(b). When the commutation between two voltage vectors is performed by one leg commutation only, the inverter applies the outgoing or the incoming voltage vectors depending on the sign of the output current in the commutating leg. Thus, the voltage vector applied to the load during the dead time is one of the expected adjacent vectors, if



(a) (b)

Fig. 14. Effect of dead time on single inverter and dual inverter (b) fundamental output voltage result

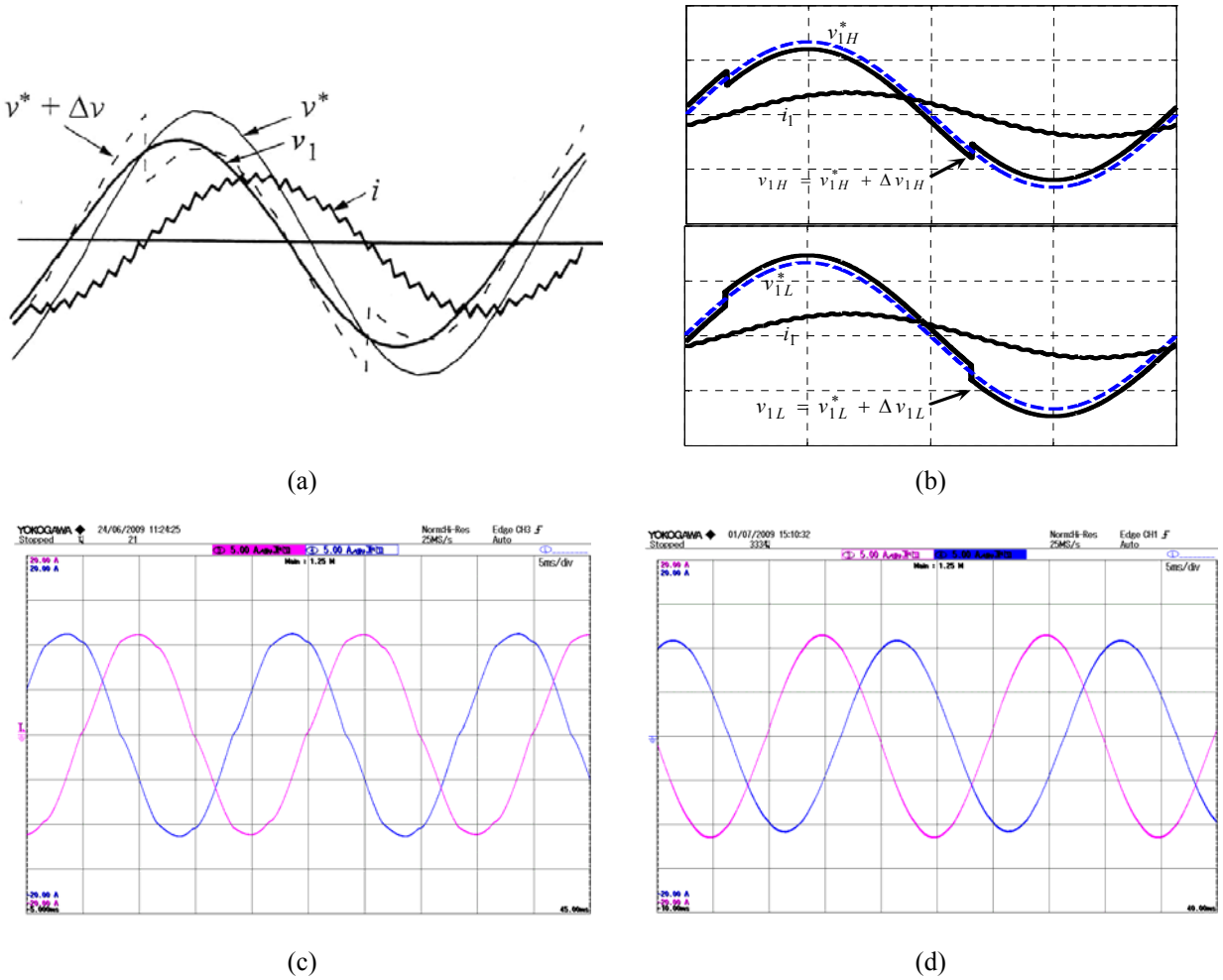


Fig. 15. Comparison of the dead time effect for dual inverter (a), (c) two-level and (b), (d) dual inverter open-loop current output.

there is no another commutation during the period affected by deadtime effect. On the contrary, when the commutation between two voltage vectors is obtained by two simultaneous commutations, the voltage vector could be different from proper adjacent vectors during the dead time, leading to a spurious voltage pulse.

In the case of the dual inverter, if the two single inverter references $\bar{v}_H^*$ and $\bar{v}_L^*$ are chosen to be collinear (the reason will be comprehensively treated in the next chapter), dead time effect of the two inverters is canceling itself, having for $\bar{v}_H^* = \bar{v}_L^*$ almost undistorted output. This is the averaged effect, instantaneous discrete vectors of the single inverters are still affected by dead time. The reason for the cancellation is illustrated on Fig. 15(a) and experimentally proved in Fig. 15(a), where is shown average effect of the dead time. If the references $\bar{v}_H^*$ and $\bar{v}_L^*$ are opposite, as it is usually case in order to provide symmetry among two inverters the average value of the errors are opposite. On the other side, the corresponding leg currents for inverters H and L have opposite senses (Fig. 10), giving in total equal errors that are canceling each other due to (27). This characteristic represents additional benefit of the dual inverter structure that can be important in some applications.

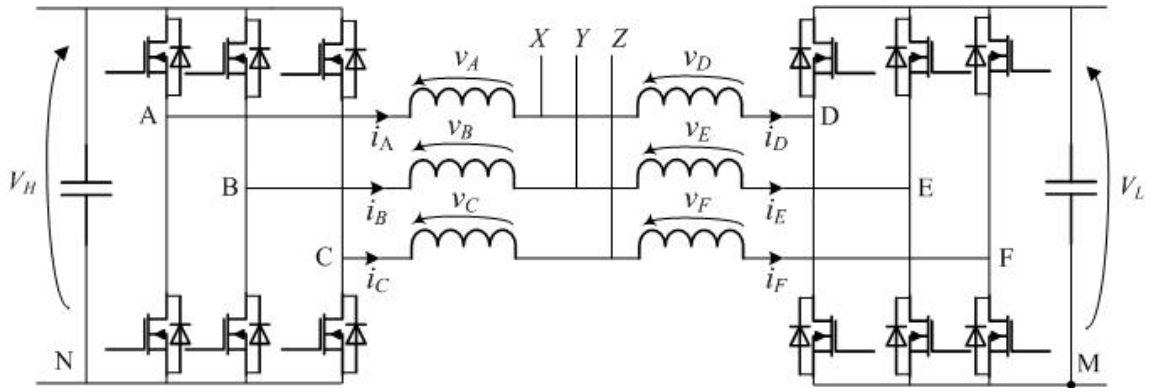


Fig. 16. Comparison of the dead time effect for two-level and dual inverter open-loop current output

2.2.3. Output voltages for parallel inverters

In order to calculate the output voltage for the parallel inverters (Fig. 16) the previous approach can be applied

$$v_{XY} = -v_{1H} + v_{AN} + v_{2H} - v_{BN} = -(v_1 - v_2)/2 + v_{AB} = -(v_{AB} - v_{DE})/2 + v_{AB}\,, \tag{33}$$

obtaining the final result

$$\begin{aligned} v_{XY} &= (v_{AB} - v_{DE})/2\,, \\ v_{YZ} &= (v_{BC} - v_{EF})/2\,, \\ v_{ZX} &= (v_{CA} - v_{FD})/2\,. \end{aligned} \tag{34}$$

The result (34) clearly proves that the output line-to-line voltage of the parallel inverter has equal amplitude as the output of single two-level inverter. The obtained result also was expected since the parallel connection in general increases the current capacity preserving the same voltage.

2.3. Space vector representation

The combination of the eight switching configuration for each three-phase inverter of dual inverter (as represented in Fig. 10) yields total 8x8 = 64 switching states. Based on the result (27) the output voltage is contributed by the two inverters in a following manner:

$$\bar{v} = \bar{v}_H + \bar{v}_L\,, \tag{35}$$

where

$$\begin{aligned} \bar{v}_H &= (2/3)V_H(S_{1H} + S_{2H}\, e^{j(2/3)\pi} + S_{3H}\, e^{j(4/3\pi)})\,, \\ \bar{v}_L &= -(2/3)V_L\,(S_{1L} + S_{2L}\, e^{j(2/3\pi} + S_{3L}\, e^{j(4/3)\pi}) \end{aligned} \tag{36}$$

are vectors corresponding to the load voltages for a standard case with balanced star-connected load with isolated star-point (neutral). Due to (35), switch states for $\bar{v}_L$ are opposite to the corresponding switch states of $\bar{v}_H$, as depicted in space vector representation on Fig. 17. Note that these conditions require that there will be no zero-sequence currents flow. Each of 64 switching states will be designated as a two-digit number consisting from digits 0-7 (format of designation "$d\bar{d}$"), with the meaning of digits explained in Fig. 17.

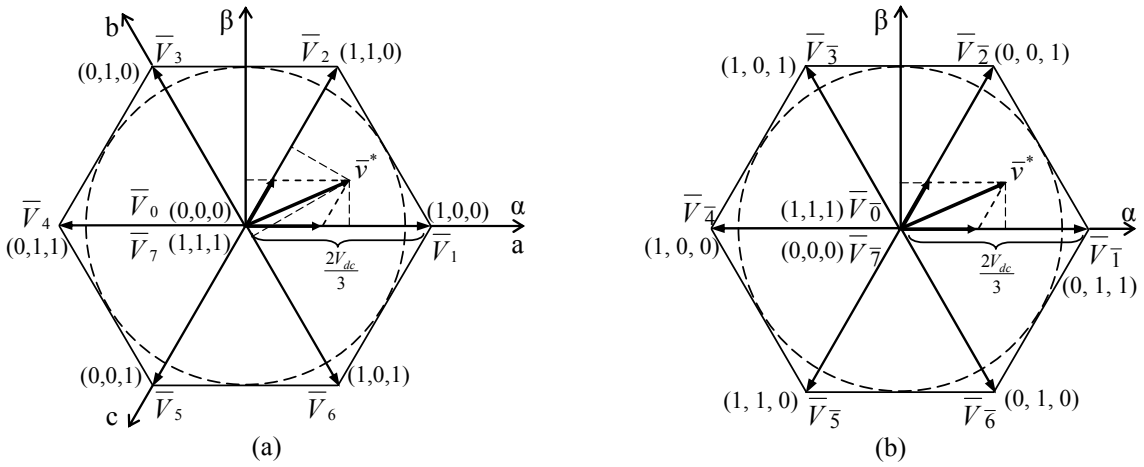


Fig. 17. Space vector representation for two inverters forming dual inverter (a) inverter H, (b) inverter L.

The derivation of the space vector representation for the dual inverter can be easily understand from Fig. 18, where "the development" is shown starting from the single two-level inverter case. Due to (35), the vector loci of the dual inverter will be grouped around the loci of the inverter H, as shown in Fig. 18(b)-(d). Since a single inverter has seven different vectors, a maximum number from two inverters would be 7x7 = 49 different output vectors, as shown in Fig. 18(b). An intermediate possibility is $V_H = 2V_L$, when 37 vectors are obtained, Fig. 18(c). In the case of $V_H = V_L = V_{dc}$, which will be analyzed first and most thoroughly, these switching states correspond to 19 different output voltage vectors, including zero vector, depicted in Fig. 18(d) and with all combinations in Fig. 19(a).

There are four types of vectors, as on Fig. 19(b):

- Zero vectors: there are ten combinations to obtain zero vector, and they can be divided in two subgroups
    1. Both vectors in combination are original zero vectors, so the result vector of dual inverter is zero, since there is no return path for the current Each single inverter has two zero vector combinations giving 2x2 = 4 such vectors in total:

$$0\overline{0},\ 0\overline{1},\ 1\overline{0},\ 1\overline{1}. \tag{37}$$

    2. Both vectors in combination have equal switching state, making the load symmetrical with respect to two sources and the currents will not flow. Since there are six active vectors of single inverter it gives six more zero vectors as a result:

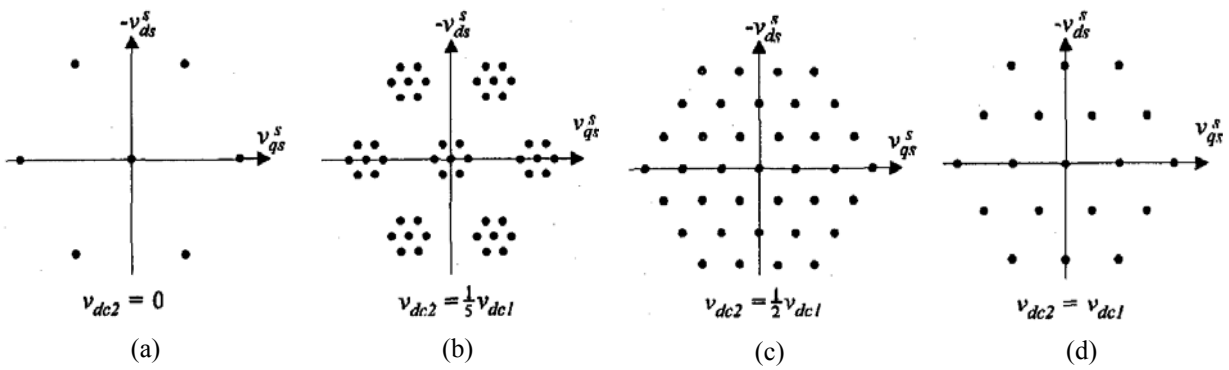


Fig. 18. Space vector plot of the dual inverter (a) starting point - single two-level inverter, (b) $V_{dc2} = (1/5)V_{dc1}$, (c) $V_{dc2} = (1/2)V_{dc1}$, (d) $V_{dc2} = V_{dc1}$.

$$1\bar{4},\ 2\bar{5},\ 3\bar{6},\ 4\bar{1},\ 5\bar{2},\ 6\bar{3}. \tag{38}$$

- Small vectors: Their amplitude is equal to the amplitude of active vector from a single inverter, and they can be divided in two subgroups.

1. If one of the inverters does not contributes to the amplitude of the output voltage, it forms the combination of zero vector from one inverter, and active vector from another, giving 2x2x6 = 24 such combinations:

$$\begin{aligned} &1\bar{0},\ 2\bar{0},\ 3\bar{0},\ 4\bar{0},\ 5\bar{0},\ 6\bar{0},\ 1\bar{7},\ 2\bar{7},\ 3\bar{7},\ 4\bar{7},\ 5\bar{7},\ 6\bar{7}, \\ &0\bar{1},\ 0\bar{2},\ 0\bar{3},\ 0\bar{4},\ 0\bar{5},\ 0\bar{6},\ 7\bar{1},\ 7\bar{2},\ 7\bar{3},\ 7\bar{4},\ 7\bar{5},\ 7\bar{6}. \end{aligned} \tag{39}$$

2. If one of the inverters "contributes" in the "next-to-opposite" direction, as a result they form another active vector of a single inverter (not completely opposite because it would lead to zero vector which is already discussed). An example of these are vector 1 of the inverter are $\bar{2}$ and $\bar{6}$ of the second inverter. For each active vector there are two "non-opposite" vectors giving 6x2 = 12 combinations in total:

$$1\bar{3},\ 31,\ 2\bar{4},\ 4\bar{2},\ 3\bar{5},\ 5\bar{3},\ 4\bar{6},\ 6\bar{4},\ 5\bar{1},\ 1\bar{5},\ 6\bar{2},\ 2\bar{6}. \tag{40}$$

- Submaximal vectors are obtained by the combination of active vectors from both inverters but in the "next-to-collinear" direction. For each active vector there are two such vectors forming 2x6 = 12 total vectors

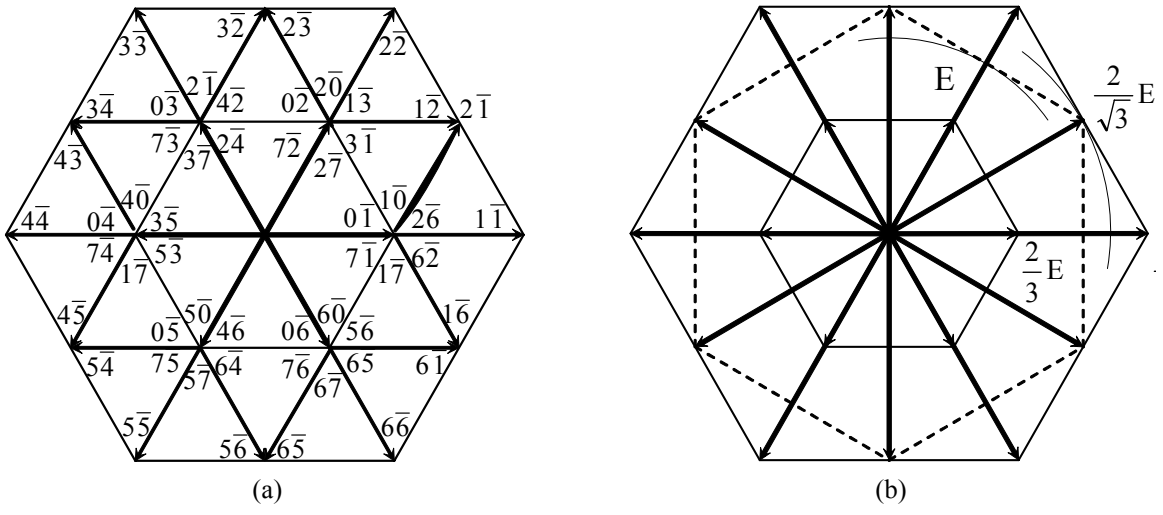
$$1\bar{2},\ 21,\ 2\bar{3},\ 3\bar{2},\ 3\bar{4},\ 4\bar{3},\ 4\bar{5},\ 5\bar{4},\ 5\bar{6},\ 6\bar{5},\ 6\bar{1},\ 1\bar{6}. \tag{41}$$

The amplitude of these type of vector is $\sqrt{3}$ times bigger than active vectors of a single inverter.

- Maximal vectors are formed by using both active and collinear vectors, so there can be only six such combinations:

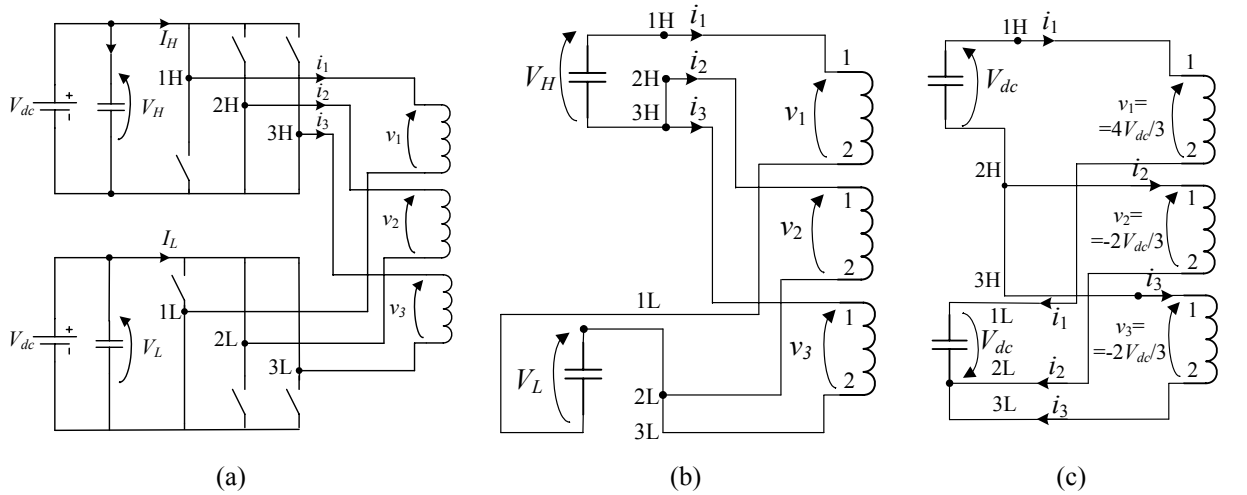
$$1\bar{1},\ 2\bar{2},\ 3\bar{3},\ 4\bar{4},\ 5\bar{5},\ 6\bar{6}. \tag{42}$$

The amplitude of these vectors is obviously the double of the single active vector. For an illustration, the switching state for one of these combinations $1\bar{1}$ is shown in Fig. 20. After simple transformations, it can be seen that three load windings are again connected in such a way that two of them are connected in parallel, and their connection is then in series with the third winding, same as for the single two-level inverter with a star load.



(a) (b)

Fig. 19. Dual inerter vector plot (a) switching combinations (b) four different vector amplitudes.



(a) (b) (c)

Fig. 20. Dual inverter configuration for switching combination $1\,\bar{1}$ (a) original (b) equivalent, (c) final result.

It can be seen that output voltage vectors are equivalent as of three-level inverter. Further comparison of its equivalency can be made regarding the redundancy of the switching combinations. Evidently, maximal vectors (maximum and minimum magnitude) are unique in both cases, but the other three types of vectors have different redundancy. First, it has only 3x3 = 27 combinations compared to previous 64. Among these, three-level inverter has no redundancy for submaximal vectors (dual has two), and only two combinations for small vectors (dual has six for each). At the end, there are only three (000_3, 111_3, 222_3) combinations for zero vectors, instead of ten of dual inverter. From the provided analysis, it can be concluded that dual inverter has redundancy much higher than three-level inverter. The redundancy of switching states corresponds to a degree of freedom useful to develop different modulation strategies, as will be discussed in Chapter 4.

In particular, the output voltage waveform of the converter has up to nine output levels of phase voltage. It represents a viable solution when the three-phase output can be connected in the open-winding configuration, as for transformers and ac motors, and especially when the dc source can be easily split in two insulated supplies, as for batteries and photovoltaic panels. Note that the presented analysis was made for the case of two insulated dc sources preventing the circulation of zero-sequence currents. In the case of the common source, the analysis is quite different, as will be shown in the next section.

2.4. Single and double supply

Generally, dual inverter can be supplied from single (common) or double (insulated) dc supply. These two cases differ significantly on many aspects and need to be analyzed separately. Historically, the first proposed dual inverter application was single-supplied [14]. The main reason for more interest in single supply was the converters application in grid-supplied high-power variable-speed drives. Single supply saves additional transformer and rectifier, it also simplifies practical issues such are relays and fuses [18]. However, significant problem is an elimination of zero-sequence currents flowing between two inverter modules.

2.4.1. Single supply

The first case to be analyzed is the simplest: a single supply with presence of the zero-sequence currents. This topology is very similar to single inverter with delta-connected load, as can be seen from Fig. 21(a). Indeed, for given dc supply voltage V_{dc} the output (load) voltage can have only one of three values: $-V_{dc}$, 0 and V_{dc}, with vectors graphical representation shown in Fig. 21(b). A delta connection of two-level inverter provides higher voltage output with given dc supply voltage V_{dc} at a price of lower current rating since switching current is not equal to load current:

$$V^{\Delta}_{\max} = \sqrt{3}V^{Y}_{\max}, \quad I^{\Delta}_{\max} = I^{Y}_{\max} / \sqrt{3} \tag{43}$$

and only three load voltage levels compared to five of star connection. This is a particular drawback for low-power drives (small leakage inductance leads to high current and subsequently torque ripple). Dual inverter with single supply has the same voltage output levels as single delta-connected inverter (therefore no multilevel), but with an advantage of having leg and load currents equal, yielding ratio of the rated power

$$S_{dual} = \sqrt{3}S_1, \tag{44}$$

where S_1 is single inverter rated current.

Although standard inverter with delta-connected load also produces phase voltages

$$\{V_{dc}, 0, -V_{dc}\}. \tag{45}$$

there is a significant difference that voltages cannot be chosen independently. For delta load, the sum of voltages is always zero, which here is not the case:

$$v_1 + v_2 + v_3 \neq 0. \tag{46}$$

It should be emphasized that as a consequence the diagram shown in Fig. 21(b) represents only αβ-plane, and furthermore

$$v_a \neq v_\alpha. \tag{47}$$

The same result can be obtained in a different manner: from total $3^3 = 27$ combinations in

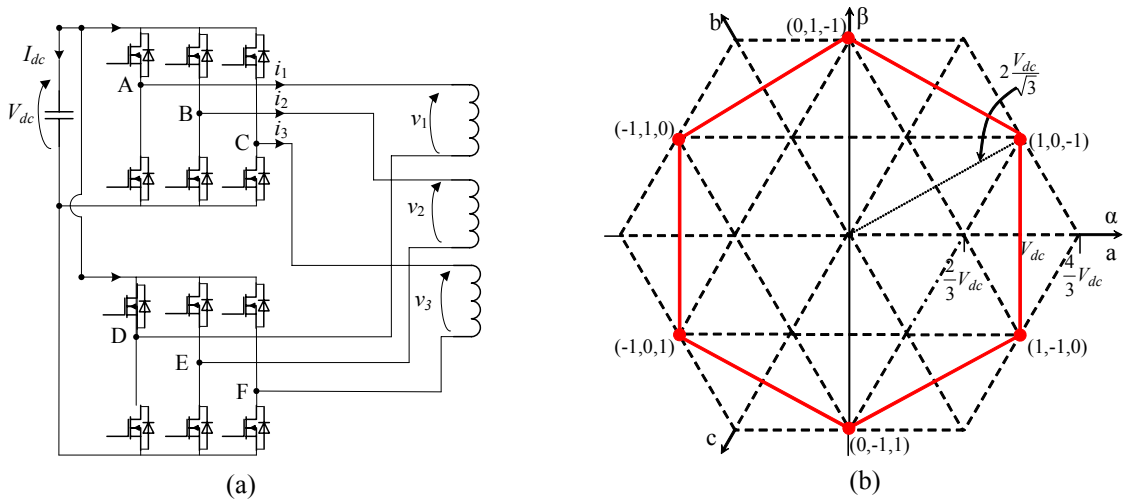


Fig. 21. Single-supply dual inverter (no zero-sequence filter) (a) topology with zero-sequence filter (b) space vector representation.

dual inverter there are only 8 (six submaximal and two zero vectors) that satisfy zero-sum criteria, and they match with the corresponding from the standard inverter delta-connected case. Since the amplitude of the submaximal vector is $\sqrt{3}$ times bigger than the intermediate vector, Fig. 19(b), the ratio determined by (44) is valid. This obtained voltage output vectors are depicted in Fig. 22(a). It is interesting to apply (12) to this case:

$$SUR = \frac{S_c}{N \cdot V_{sw} I_{sw}} = \frac{3VI}{12 V_{sw} \cdot I_{sw}} = \frac{3 \cdot 0.707 V_{dc} \cdot I}{12 V_{dc} \cdot I} = 0.177. \tag{48}$$

In the case of only one available source, maximum available voltage is lower, in order to cancel zero sequence current: Consequently SUR is lower than for two-level or dual inverter with two supplies:

$$SUR = \frac{SUR_1}{SUR_2} = \frac{0.177}{0.204} = 1.15. \tag{49}$$

Therefore this converter would cost 15 % more for the switches.

Now presume that zero-sequence current is eliminated giving for balanced load:

$$v_1 + v_2 + v_3 = 0, \tag{50}$$

Considering there 27 different vectors in αβ-plane, some of them can coincide forming a redundancy, e.g. completely different switching combinations $\bar{v}$ = (V_{dc}, 0, V_{dc}) and $\bar{v}'$ = (0, -V_{dc}, 0) give the same output vector. For two vectors $\bar{v}$ and $\bar{v}'$ obtained by different switching combinations the condition of coincidence is:

$$\begin{aligned} v_\alpha &= v'_\alpha, \\ v_\beta &= v'_\beta, \end{aligned} \tag{51}$$

Note that (50) does not mean that switching states need to satisfy, i.e.

$$v_{AD} + v_{BE} + v_{CF} \neq 0, \tag{52}$$

since there is voltage drop on the filter L_o. Condition (51) gives

$$\frac{2}{3}(v_1 - \frac{1}{2}v_2 - \frac{1}{2}v_3) = \frac{2}{3}(v'_1 - \frac{1}{2}v'_2 - \frac{1}{2}v'_3), \tag{53}$$

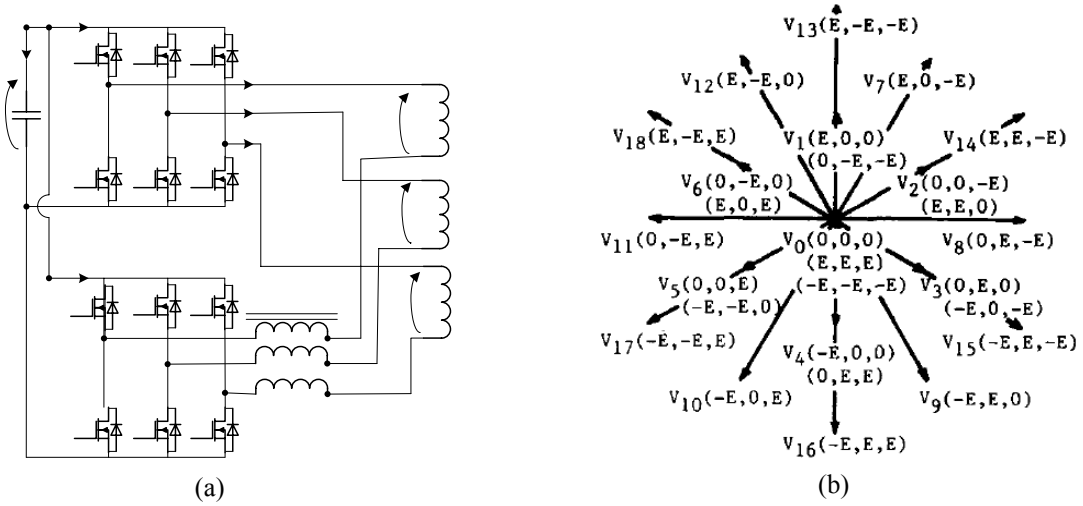


Fig. 22. Single-supply dual inverter with zero-sequence filter (a) topology, (b) space vector representation.

$$\frac{2}{3}(\frac{\sqrt{3}}{2}v_2 - \frac{\sqrt{3}}{2}v_3) = \frac{2}{3}(\frac{\sqrt{3}}{2}v_2' - \frac{\sqrt{3}}{2}v_3'), \tag{54}$$

yielding:

$$\begin{aligned} v_1 - v_2 &= v_1' - v_2', \\ v_1 - v_2 &= v_1' - v_2', \end{aligned} \tag{55}$$

Depending on the value of the difference $d = v_1 - v_2$ from (55) three cases can be distinguished:

$$d \in \{V_{dc,} 0, -V\}. \tag{56}$$

The first case gives pairs (V_{dc}, 0) and (0, -V_{dc}) as (v_1, v_2). Now considering second condition in (55) there can be same three cases regarding the difference $e = v_1 - v_3$:

- $e = 0$ gives (V_{dc}, V_{dc}) in pair with (0, 0) → in total (V_{dc}, 0, V_{dc}) = (0, -V_{dc}, 0) i.e. one pair,
- $e = V_{dc}$ gives (V_{dc}, 0) in pair with (0, -V_{dc}) → in total (V_{dc}, 0, 0) = (0, -V_{dc}, -V_{dc}), i.e. one pair,
- e = -V_{dc} cannot give anything since it would mean $v_3 = 2V_{dc}$.

Similarly the second case gives (-V_{dc}, -V_{dc}) in pair with (0, 0) and (V_{dc}, V_{dc}). Considering second condition (55) the second group gives four pairs (v_1, v_3):

- (V_{dc}, V_{dc}) in pair with (0, 0) and (-V_{dc}, -V_{dc}) → in total (-V_{dc}, -V_{dc}, V_{dc}) = (0, -V_{dc}, 0) = (0, -V_{dc}, 0), i.e. two pairs
- (V_{dc}, 0) in pair with (0, -V_{dc}) → in total (V_{dc}, 0, 0) = (0, -V_{dc}, -V_{dc}), i.e. two vectors
- (V_{dc}, -V_{dc}) cannot be paired since its maximum possible difference.

The third case gives (-V_{dc}, 0) in pair with (0, V_{dc}). Considering second condition (55) the second group gives four pairs (v_1, v_3):

- (-V_{dc}, -V_{dc}) in pair with (0, 0) → in total (-V_{dc}, 0, -V_{dc}) = (0, V_{dc}, 0), i.e. one pair,
- (-V_{dc}, 0) in pair with (0, V_{dc}) → in total (-V_{dc}, 0, 0) = (0, V_{dc}, V_{dc}), i.e. one pair,
- (V_{dc}, -V_{dc}) cannot be paired since its maximum possible difference. In total

$$27 - (2+4+2) = 19, \tag{57}$$

different vectors, result already obtained in previous section for dual inverter with double supply.

2.4.2. Double supply

For two isolated dc supplies configuration there are two main differences with respect to the single supply dual inverter:

- Lack of zero-sequence path,
- Different potentials between two inverters ($v_{NM} \neq 0$!), i.e. existence of the common mode voltage that will be addressed in the following chapter.

However, in some applications there is no significant complexity to provide two isolated supplies instead of one with the double current capability. For example batteries are modular (consisting of cells), and any power battery is assembled of more cells in series/parallel. Similarly, in photovoltaic applications power array consists of number of modules, so the partition in two isolated arrays can be easily achieved.

2.5. Summary

In this chapter, a dual two-level inverter is introduced as a part of the larger class of cascaded inverters. It has been shown that this structure is not limited to symmetrical topologies only, but represents a more general solution to obtain multilevel output voltage avoiding the complexity of the common three-phase multilevel inverters. Compared to similar solutions, such are cascaded H-bridge, cascaded three-phase and parallel standard inverters dual inverter possesses some favorable features.

The expression for the output voltage is shown to be a compound from the output voltages of the two single inverters. Based on this result modulation techniques will be developed with the reference to the standard two-level inverter, which significantly simplifies also the control, when compared to other multilevel competitors. Another beneficial feature of the dual inverter is inherent immunity to the deadtime effect, which is a rare feature among voltage source inverters.

The dual structure of the inverter introduces a degree of freedom regarding the choice of the supply: single or double dc supply. Although the single supply seems decisively simpler, it has a significant disadvantage of zero-sequence component filter feature, since the performance of the original converter is quite unattractive. Furthermore, with the penetration of the dual inverter from the grid-supply towards other applications the availability of two isolated supplies represents no problem anymore.

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3. Modulation strategies for dual inverter: state of the art

The main modulation task is to achieve control of the system by switching converter power components, i.e. determining which discrete vectors should be applied and for how long within a switching period. A typical modulation provides average voltage value equal to the voltage reference, thus making a direct dc-ac conversion. There is also another, yet less common control approach, called direct (or modulation control), where discrete voltages are chosen directly from the state of the control variable. The examples of the second concept are direct torque control in the area of drives and direct power control for grid-connected applications [1]. For both approaches, the demands for a modulation can be classified in two priority levels, which may vary depending on the application. Typically the higher priority tasks are:

- Wide range of linear operation,
- Minimal number of commutations to minimize the losses,
- Minimal harmonic content in the voltage and consequently current, elimination of low-frequency harmonics

Whereas the additional demands can be:

- Simplicity of the modulator - it is one of the most demanding parts of the control algorithm
- Acoustic noise reduction
- Common-mode voltage reduction
- Operation in overmodulation region including square wave

It should be noted that most of the demands are conflicting, for example lower number of commutations or simplicity of the algorithm usually lead to higher harmonic content.

The switching frequency criteria can further subdivide multilevel modulations into three classes: fundamental, mixed and high switching frequency, as shown in Fig. 1.

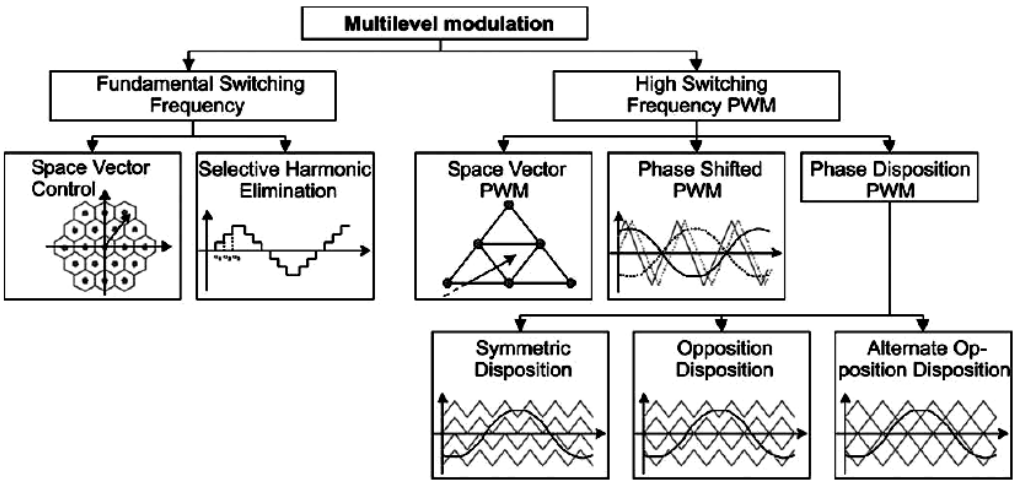


Fig. 1. Multilevel modulation classification.

3.1. Fundamental frequency switching

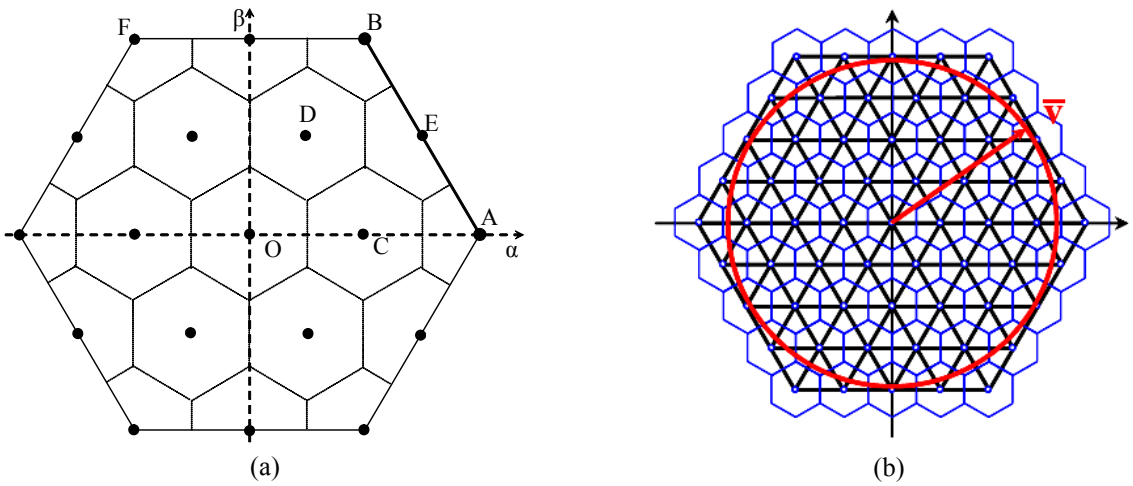
Fundamental switching, also known as a "selective harmonic elimination" or "programmed modulation" is a particular type of modulation developed for multilevel converters. Its application is dedicated to the top power range of converters, where switching frequency is in order of hundreds of Hz [2].

A common feature of the programmed modulation strategies is that the optimization computation is done off-line on a more powerful computer. The result of the calculation is a set of the switching angles in function of the modulation index *m*, to be stored in memory (ROM, EPROM) of the PWM controller. However, as the output frequency decreases a number of pulses also must decrease in order to keep switching frequency low.

3.1.1. Space vector control

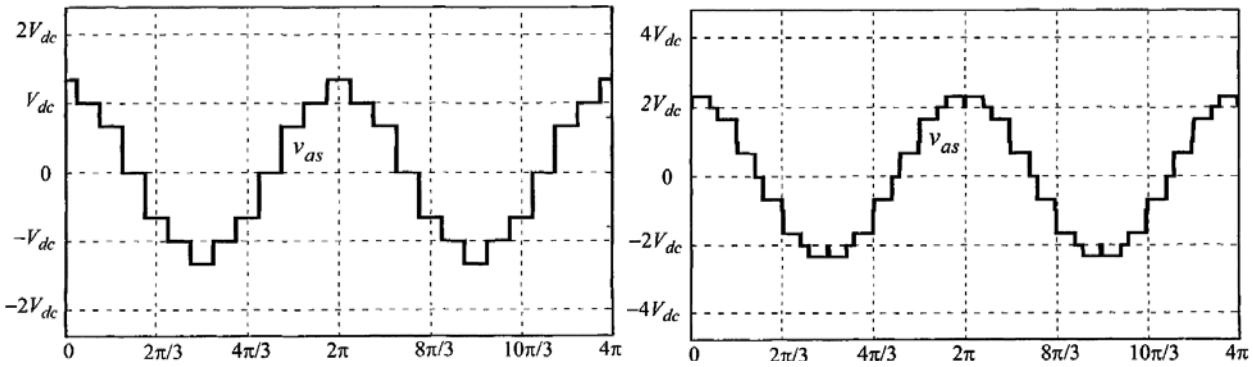
Instead of classical modulation applied for two-level inverter, multilevel inverters can satisfy with fixed discrete vectors within switching period. However, this would mean that voltage reference and average value will not be equal, creating an error that remains uncompensated. The graphical representation of the space vector control (SVC) is given in Fig. 2, showing zones nearest to one of the vertices defined by the medians. These medians of all grid triangles create hexagonal mesh centered in each vertex and determine the sets of points closest to each generable vector. Therefore, the aim of the modulation is to choose among all the generable vectors the one that minimizes the error. If the reference vector is rotating at a constant angular speed, the output voltage will have a symmetrical staircase waveform and switches will commutate at the fundamental (low) frequency.

This kind of modulation is particularly suited for multilevel converter with a high number of levels because the error made is getting smaller as number of level increases [3]. Then it becomes a viable solution since modulation and hardware complexity sharply increases with the number of the levels. Moreover, the switching frequency of each switch is equal to the



(a) (b)

Fig. 2. Space vector control (a) dual two-level inverter and (b) five-level inverter.



(a) (b)

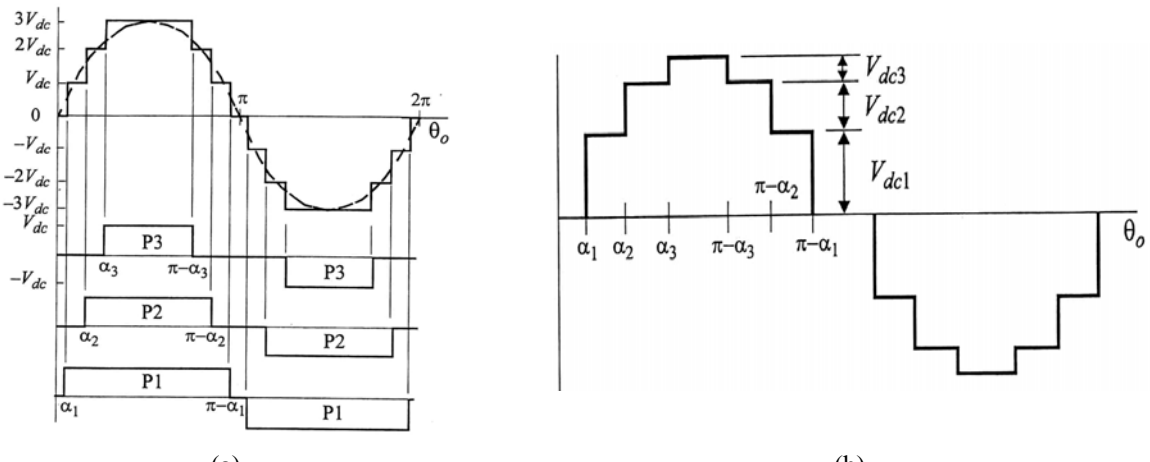
Fig. 3. Voltage waveform for space vector control and minimum THD (a) dual inverter, and (b) five-level inverter.

fundamental, meaning reduced commutation losses and the possibility to apply this modulation even to slow devices like GTO for high power applications. A comparison of three- and five-level inverter SVC performances is given in Fig. 2 (space domain) and Fig. 3 (time domain). Evidently, SVC is definitely unreliable when it applied to a three-level inverter because the ripple on the output voltage becomes unacceptable. Therefore, it will not be considered further.

3.1.2. Selective harmonic elimination

In applications where the output voltage amplitude and frequency are relatively fixed, PWM need not be used to synthesize the output voltage since a sufficiently small harmonic distortion can be obtained by simple fundamental frequency. Furthermore, the dc voltage level magnitudes can be adjusted in order to minimize additionally harmonic distortion. The principle of the selective harmonic elimination (programmed modulation) is shown in Fig. 4, switching levels in order to form step-shaped waveform close as possible to sinusoidal, using only one pulse of each switch within whole output voltage period. For a *l*-level inverter the Fourier coefficients are given by:

$$v_{AN}^{(n)} = \frac{4}{n\pi}\left(\frac{V_{dc}}{2} + \sum_{k=1}^{l/2-1} V_{dc}\cos n\alpha_k\right),\ v_{AN}^{(n)} = \frac{4}{n\pi}\sum_{k=1}^{(l-1)/2} V_{dc}\cos n\alpha_k \tag{1}$$



(a) (b)

Fig. 4. Switching pattern for selective harmonic elimination (a) equal, and (b) different voltage levels.

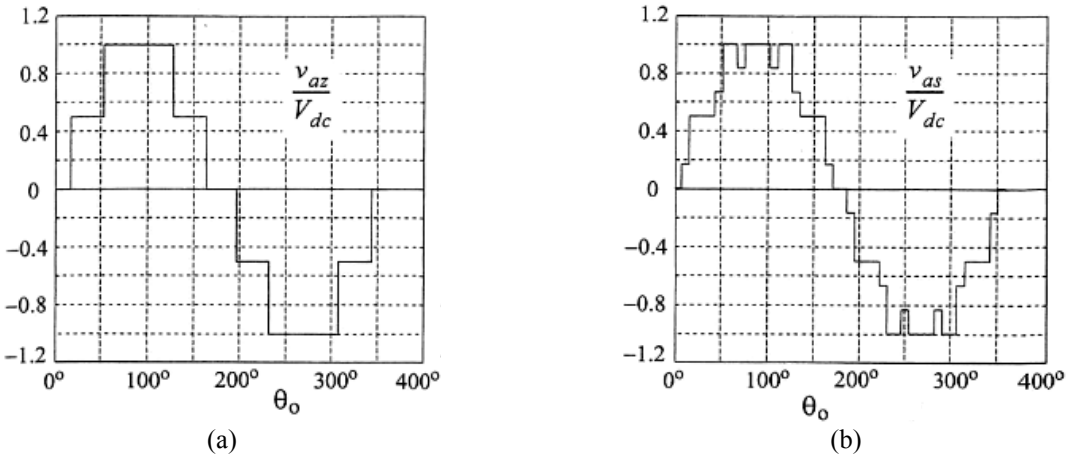


Fig. 5. Voltage waveforms for five-level inverter eliminating the 5th harmonic for modulation index *M= 1.0:* (a) line-to-DC midpoint voltage *Vaz,* (b) line to load-neutral voltage v_{as}.

depending whether *l* is even or odd respectively. Further approaches are:

- The DC voltages remain equal: The switching angles are adjusted to adjust the fundamental voltage component and minimize the harmonic distortion.
- The voltage and angles are both adjusted to minimize the harmonic distortion.

For example if $l = 7$ maximum three harmonics can be eliminated, resulting of determined modulation index *m*. Optimum solutions are presented in Fig. 5. Normally *m* is determined by control algorithm, so the switching angles can be determined in order to eliminate two harmonics (fifth and seventh).

However, to achieve acceptable performance with such limited resource the dc voltage level magnitudes need to be adjusted as desired. This can be achieved in multilevel converters, e.g. diode-clamped and cascaded inverters; however, it imposes additional problems [2]. To conclude, a major problem is a poor performance with lower values of the modulation index, shown in Fig. 6. After certain m_{min} there is no solution. Therefore, the method is suitable for applications where the output voltage amplitude and frequency are relatively fixed, so PWM need not be used to synthesize the output voltage since a sufficiently small distortion can be obtained by simple fundamental frequency switching.

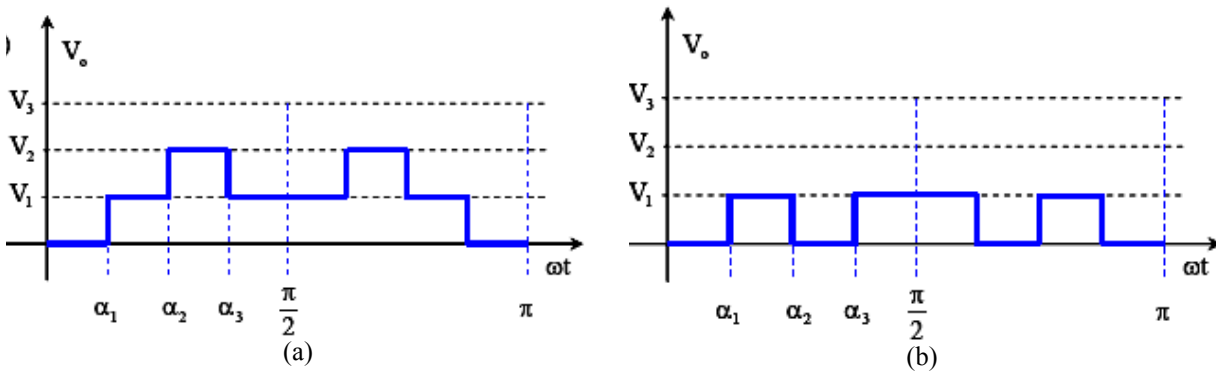


Fig. 6. Poor performance of selective harmonic elimination in a seven level converter for (a) medium, b) low modulation index.

3.2. Modulation techniques for two-level voltage source inverters

A brief retrospection of modulation principles and classic techniques for three-phase two-level inverter is given, as an introduction for the treatment of dual two-level inverter. This simplest three-phase inverter with only eight switching states possess many fundamental characteristics (vector application times, redundancy, modulation continuity/discontinuity), and concepts (carrier-based, space vector etc.), so the Author find it useful to present the methods on a simpler converter before to enter in a more complex topology. In this section under "two-level inverter" term will be assumed well-known standard inverter with star-connected load as shown in Fig. 7(a).

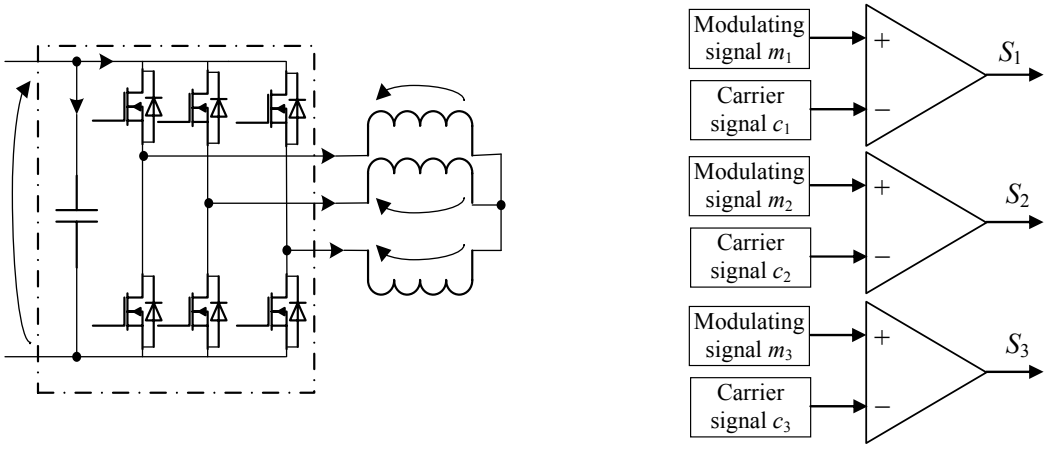
3.2.1. Carrier-based PWM

Carrier-based PWM is a class of methods characterized by the three modulation signals generated separately and compared with so-called carrier signals, schematically represented in Fig. 7(b). To simplify the calculations carrier signals are usually of a very simple and constant form while modulation signals directly depend on the reference voltage. The concept was also historically the first one implemented in power electronics back in 1964, particularly with the algorithm today known as "sinusoidal modulation" [4]. It was based on the comparison of low-frequency modulating signal with high-frequency triangular (or sawtooth) carrier signal and realized in the analog technique. The method is depicted in Fig. 8(a), suggesting that average voltage within a switching period is equal to the reference voltage. In geometrical terms it would mean

$$\frac{|AB|}{|BF|} = \frac{|AD|}{|AH|}, \tag{2}$$

due to the half-symmetry of the switching period. The proof starts from the evident similarity of the triangles ΔABD~ΔFBI then using proportionality of its laterals:

$$|AB| : |BF| = |AD| : |FI|, \tag{3}$$



(a) (b)

Fig. 7. Two-level inverter with delta connected load (a) topology and (b) space vector representation.

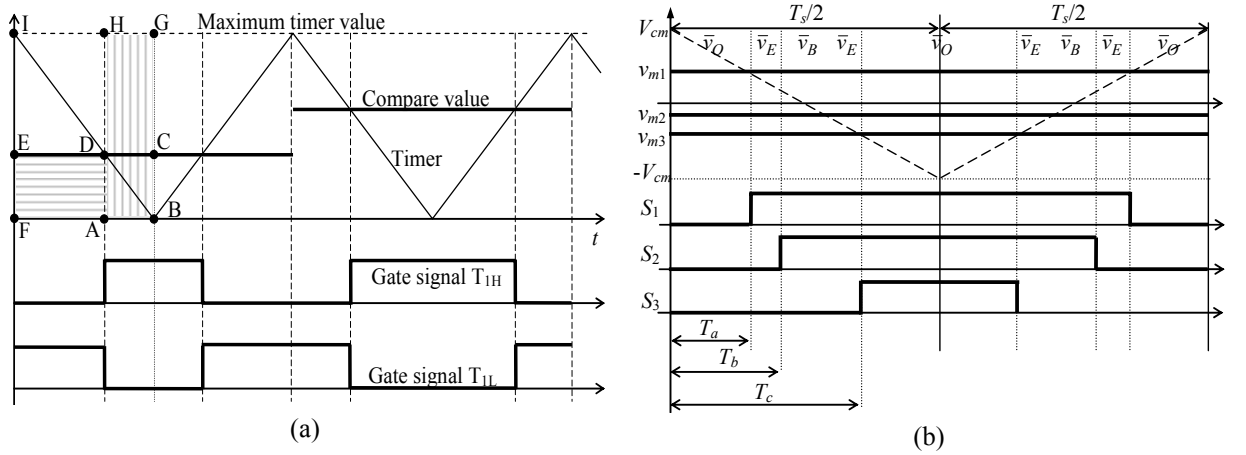


Fig. 8. Two-level inverter modulation principle: (a) single phase ("dc chopper") and (b) three-phase.

and taking into account

$$|FI| = |AH|, \tag{4}$$

However, the same conclusion that modulation signal proportional to the reference voltage provides average value equal to the reference cannot be directly extended to a three-phase case since output voltages are affected by all three switching states (2.18). Setting the modulation signals v_{m1}, v_{m2}, and v_{m3} proportional to reference voltages v_1*, v_2*, and v_3* and considering Fig. 8(b) yields:

$$T_a = \frac{V_{cm} - v_{m1}}{V_{cm}} \frac{T_s}{4},\ T_b = \frac{V_{cm} - v_{m2}}{V_{cm}} \frac{T_s}{4},\ T_c = \frac{V_{cm} - v_{m3}}{V_{cm}} \frac{T_s}{4}. \tag{5}$$

The calculation of the output voltage is based on the equations (2.18):

$$\begin{aligned} v_{AS} &= (2v_{AN} - v_{BN} - v_{CN})/3, \\ v_{BS} &= (-v_{AN} + 2v_{BN} - v_{CN})/3, \\ v_{CS} &= (-v_{AN} - v_{BN} + 2v_{CN})/3, \end{aligned} \tag{6}$$

Calculating the average value of output voltage v_{as}:

$$v_{as} = \frac{2}{T}\left(\frac{2}{3} V_{dc}(T_b - T_a) + \frac{1}{3} V_{dc}(T_c - T_b)\right), \tag{7}$$

Introducing (5) in (6)

$$v_{as} = \frac{V_{dc}}{3V_{cm}}(2((V_{cm} - v_{m2}) - (V_{cm} - v_{m1})) + ((V_{cm} - v_{m3}) - (V_{cm} - v_{m2}))), \tag{8}$$

and finally

$$v_{as} = \frac{V_{dc}}{3V_{cm}}(2v_{m1} - v_{m2} - v_{m3}), \tag{9}$$

showing that simple modulating signals proportional to the reference will lead to proper average voltage. It should be noted that the popular name "sinusoidal PWM" is misleading, as it denotes a particular (yet often at the time) case of sinusoidal modulating signals for sinusoidal reference. Therefore, a more proper name could be "proportional modulator", because for other methods that will be presented modulating signals are not proportional to the reference, i.e. for sinusoidal references modulating signals contain harmonics.

The carrier voltage amplitude V_{cm} is determined by the maximum output phase voltage that can be achieved. For given sinusoidal voltage references with still unknown amplitude V_m

$$\begin{aligned} v_{m1} &= V_m \cos\theta, \\ v_{m2} &= V_m \cos(\theta - 2\pi/3), \\ v_{m3} &= V_m \cos(\theta + 2\pi/3), \end{aligned} \tag{10}$$

the maximum output voltage in phase "1" is reached with the conditions

$$v_{m1} = V_m,\ v_{m2} = -V_m/2,\ v_{m3} = -V_m/2. \tag{11}$$

On the other side linear range is defined as the amplitude of the modulation signal V_m equal to the carrier signal amplitude V_{cm}:

$$V_m = V_{cm}, \tag{12}$$

from (5) yields

$$T_a = 0,\ T_b = 3\frac{T_s}{8},\ T_c = 3\frac{T_s}{8}, \tag{13}$$

which introduced in (6) gives the average voltage

$$v_{as} = \frac{2}{T}((T_b - T_a)\frac{2V_{dc}}{3} + (T_c - T_b)\frac{V_{dc}}{3}) = \frac{V_{dc}}{2} = V_{cm}. \tag{14}$$

It can be concluded that both maximum average value in the linear range and carrier signal amplitude are equal to $0.5V_{dc}$. This is a principal drawback of this carrier-based method, a direct consequence of neglecting that in three-phase system output in one phase depends on states of the other two phases. For this reason "proportional modulator" was superseded by the other methods (including carrier-based) are able to provide 15.5 % higher voltage output. Another possible drawback of the method is the requirement for the modulation signals in *abc*-domain, which are quite rarely used in control algorithms.

3.2.2. Space vector PWM

Space vector PWM algorithm generates simultaneously all three duty cycles from the calculations based on geometrical representation of vectors. Its major advantage is clearer insight, making it today's most popular modulation method, although it turns into a drawback when comes to harmonic analysis of the results. The method is based on the fact that there are only few available switching states of the inverter, i.e. $2^3 = 8$, denoted $\{\overline{V}_0, \overline{V}_1, .., \overline{V}_7\}$ in Fig. 9(a), since leg voltages can produce only two levels. For a balanced star load with isolated star point, it gives only five possible output voltages:

$$u_{as}, u_{bs}, u_{cs} \in \left\{0, \frac{2}{3}V_{dc}, \frac{1}{3}V_{dc}, -\frac{1}{3}V_{dc}, -\frac{2}{3}V_{dc}\right\}, \tag{15}$$

From the fact that voltage zero-sequence component is always zero a space-vector representation in αβ-plane corresponds to the *abc*-plane representation, as shown in Fig. 9. The amplitude of the maximum output voltage in linear region is the radius of the inscribed circle with magnitude:

$$V_{\max} = \frac{V_{dc}}{\sqrt{3}} = \frac{2}{\sqrt{3}}0.5V_{dc} = 1.155(0.5V_{dc}). \tag{16}$$

Compared to "sinusoidal modulation", it gives 15.5 % higher fundamental and therefore superior performance. Sometimes this result is compared with fundamental harmonic in six-step (square, fundamental switching) mode:

$$V_{\max} = \frac{V_{dc}}{\sqrt{3}} = \frac{\pi}{2\sqrt{3}}(2/\pi)V_{dc} = 0.907\,(2V_{dc}/\pi), \tag{17}$$

that is not entirely correct since the quality is completely different - square mode has highly distorted output.

A. Calculation of the application times

The SVM principle decomposes reference $\overline{V}^*$ as a sum of the nearest three vectors (NTV) $\overline{V}_a^*$, $\overline{V}_b^*$, and $\overline{V}_o^*$. Due to the hexagon symmetry, the analysis can be restricted to one of the six big sectors, such is one with the vector $\overline{V}^*$ in Fig. 9(a). In the absolute units, the application times T_a and T_b, of active vectors $\overline{V}_a^*$, $\overline{V}_b^*$ can be calculated as geometrical projections from Fig. 9(b):

$$\begin{aligned} T_b &= \frac{V_b}{V_2}T_s = \frac{(2/\sqrt{3})V_\beta^*}{(2/3)V_{dc}}T_s, \\ T_a &= \frac{V_a}{V_1}T_s = \frac{V_\alpha^*}{(2/3)V_{dc}}T_s - \frac{T_b}{2}, \end{aligned} \tag{18}$$

being $\overline{V}^* = \overline{V}_\alpha^* + j\overline{V}_\beta^*$, and T_S the switching period. The application times of null vectors are given by

$$T_o = T_s - T_a - T_b, \tag{19}$$

In order to calculate the application times in relative units t_a, t_b, t_c the vectors magnitudes V_a, V_b, V_o has to be scaled to the magnitudes of new vectors V_a', V_b', V_o' in the same ratio as original size $2V_{dc}/3$ to $V_{dc}/\sqrt{3}$. The reason is that application time is calculated comparing original vectors to $2V_{dc}/3$, however relative vectors are expressed with respect to base voltage $V_{dc}/\sqrt{3}$.

Further, only relative unit vector reference $\overline{v}^* = \overline{v}_\alpha^* + j\overline{v}_\beta^*$ will be used. The obtained

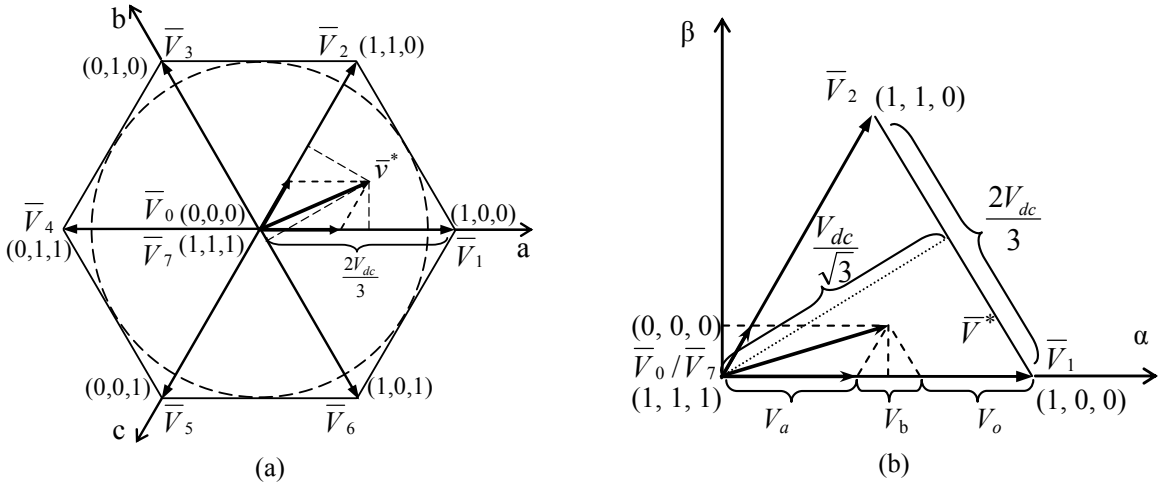


Fig. 9. Space-vector switching representation for two-level star-connected load inverter (a) abc- and (b) αβ-domain.

application times in relative units with respect to T_S are:

$$t_a = \frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*, \quad t_b = v_\beta^*, \; t_o = 1 - \frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^* \text{ [pu]} \tag{20}$$

Taking into account symmetry of switching pattern for the minimization of harmonic and ripple content [2], SVM algorithm theoretically would finish here, since true SVPWM unit in DSP would require the application times as input data[1]. However, a more general case is carrier-based modulation unit that requires duty cycles, which still need to be calculated. Due to the redundancy of zero vector there is a degree of freedom to choose in following steps:

1. Determine the "minimum duty cycle" d_{min},
2. Add t_b to d_{min} in order to obtain "middle duty cycle" d_{mid},
3. Add t_a to d_{mid} in order to obtain "maximum duty cycle" d_{max},

because all three duty cycle values will be compared to the same carrier. Due to the degree of freedom, there are countless possibilities among which the most applied patterns are:

- Continuous symmetrical zero placement commutation, with all three phases having one pulse in each switching period and equal $\bar{v}_o$ duration at the beginning/end and in the middle of the half-switching period:

$$\begin{aligned} d_{\min} &= \frac{t_o}{2} = \frac{1}{2} - \frac{\sqrt{3}}{4} v_\alpha^* - \frac{1}{4} v_\beta^*, \\ d_{mid} &= d_{\min} + t_b = \left(\frac{1}{2} - \frac{\sqrt{3}}{4} v_\alpha^* - \frac{1}{4} v_\beta^*\right) + v_\beta^* = \frac{1}{2} - \frac{\sqrt{3}}{4} v_\alpha^* + \frac{3}{4} v_\beta^*, \\ d_{\max} &= d_{mid} + t_a = \frac{1}{2} - \frac{\sqrt{3}}{4} v_\alpha^* + \frac{3}{4} v_\beta^* + \left(\frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*\right) = \frac{1}{2} + \frac{\sqrt{3}}{4} v_\alpha^* + \frac{1}{4} v_\beta^*. \end{aligned} \tag{21}$$

Particularly it can be noted that for

$$\bar{v}^* = 0, \tag{22}$$

duty cycles are not zero but

$$d_{min} = d_{mid} = d_{max} = 0.5, \tag{23}$$

therefore disproportional to the modulation signal.

The same expression (21) can be obtained by setting equal $\bar{v}_o$ application times in both the beginning/end and middle of the switching period:

$$1 - d_{\max} = d_{\min}, \tag{24}$$

Applying the algorithm gives

$$1 - (d_{\min} + t_b + t_a) = d_{\min}, \rightarrow d_{\min} = (1 - t_b - t_a)/2 \tag{25}$$

and finally

$$\begin{aligned} d_{\min} &= t_o/2, \\ d_{mid} &= (1 - t_b + t_a)/2, \\ d_{\max} &= (1 + t_b + t_a)/2 \end{aligned} \tag{26}$$

[1] There are such SVM units which require application time, e.g. *F2812* DSP with registers ACTRx and CMPRx.

- discontinuous modulation with the maximum duty cycle equal to one

$$d_{max} = 1, \tag{27}$$

and $\bar{v}_o$ only in the middle of the switching period:

$$\begin{aligned} d_{\min} &= t_o = 1 - \frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*, \\ d_{mid} &= d_{\min} + t_b = (1 - \frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*) + v_\beta^* = 1 - \frac{\sqrt{3}}{2} v_\alpha^* + \frac{1}{2} v_\beta^*, \\ d_{\max} &= d_{mid} + t_a = 1 - \frac{\sqrt{3}}{2} v_\alpha^* + \frac{1}{2} v_\beta^* + (\frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*) = 1 \text{ [pu]} \end{aligned} \tag{28}$$

- discontinuous modulation with the minimum duty cycle always off

$$d_{min} = 0, \tag{29}$$

and $\bar{v}_o$ only at the beginning/end of the switching period.

$$\begin{aligned} d_{\min} &= 0, \\ d_{mid} &= d_{\min} + t_b = 0 + v_\beta^* = v_\beta^*, \\ d_{\max} &= d_{mid} + t_a = v_\beta^* + (\frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^*) = \frac{\sqrt{3}}{2} v_\alpha^* + \frac{1}{2} v_\beta^* \text{ [pu]} \end{aligned} \tag{30}$$

- Discontinuous symmetrical modulation with 60º fixed switch period. It is a middle solution between previous two, and the duty cycles are obtained as a combination of (28) and (30). Each of these two equations is applied for central 60º within 120º where they were applied solely. Therefore, zero vectors are present either in the beginning/end or in the middle of the switching period.

The obtained PWM patterns are presented in Fig. 10, together with pattern from the proportional (sinusoidal) modulation given for a comparison.

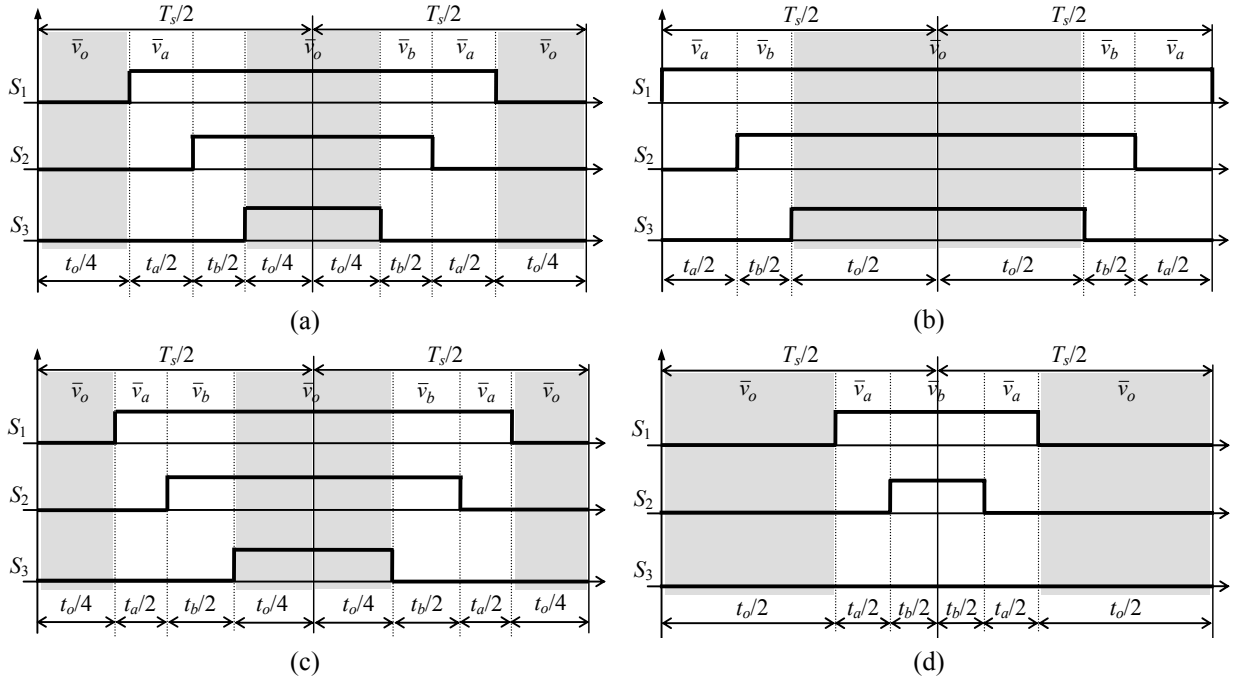


Fig. 10. Switching patterns for some modulation types (a) proportional, (b) discontinuous $d_{max} = 1$, (c) continuous symmetrical, (d) discontinuous $d_{min} = 0$.

B. Determination of the sector

Angle θ^* between reference vector $\overline{V}^* = \overline{V}_\alpha^* + j\overline{V}_\beta^*$ and α-axis:

$$\theta^* = \arctan(\overline{V}_\beta^* / \overline{V}_\alpha^*), \tag{31}$$

can be used to determine sector s of the hexagon:

$$(s-1)(2\pi/3) \le \theta^* < s(2\pi/3), \tag{32}$$

This is the simplest way to determine the sector; however, with slower processors it was important to avoid usage of function *arctangent* as time-consumptive. Another solution is determination based on the component signs and tangent of the angle, like:

$$(u_\alpha \ge 0) \text{ and } (u_\beta > 0) \text{ and } (\sqrt{3}u_\beta < u_\alpha), \tag{33}$$

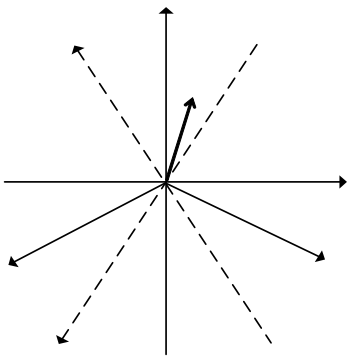
which are simple, but repetitive and therefore require more program memory. The optimal solution is to introduce 2→3 transformation denoted $\mathbf{S_c}$, to obtain six sectors instead of four quadrants inherent for αβ-coordinate system, [5].

$$\begin{bmatrix} v_x \\ v_y \\ v_z \end{bmatrix} = \mathbf{S_c}^{-1}\mathbf{U}_{\alpha\beta} = \begin{bmatrix} 0 & 1 \\ \sqrt{3}/2 & -1/2 \\ -\sqrt{3}/2 & -1/2 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}, \tag{34}$$

In the transform α- and β-axe are swapped compared to the inverse Clarke transform matrix **C**:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{U}_{abc} = \mathbf{C}^{-1}\mathbf{U}_{\alpha\beta} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix}^{-1} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}, \tag{35}$$

as depicted in Fig. 11(a). The method is based on the well-known characteristic that projection to the axis of the vector is equivalent to the sum of the projections of its vector components. Using introduced coordinate system each sector is uniquely determined by the signs of the x-, y- and z-projection, as stated in Fig. 11(b). Furthermore, introducing "code" 1 for $v_x > 0$ and "code" 0 for $v_x < 0$, and different numbering of the sectors they can be coded with binary numbers, since there are $2^3 = 8$ combinations and (0, 0, 0) and (1, 1, 1) are impossible. Regarding the other sectors, it is possible to calculate all the cases referred to the first sector, and to reassign calculated duty cycles in the transposed manner.



(a)

		Sector number					
		1	2	3 (1+2)	4	5(1+4)	6(2+4)
Quantity	V_x	**>0**	<0	>0	<0	>0	<0
	V_y	<0	**>0**	>0	<0	<0	>0
	V_z	<0	<0	<0	**>0**	>0	>0

(b)

Fig. 11. Space representation in αβ and introduced xyz coordinate systems (a) Illustration of the projection vector components and (b) New numeration (Arabic) and original (Roman numbers).

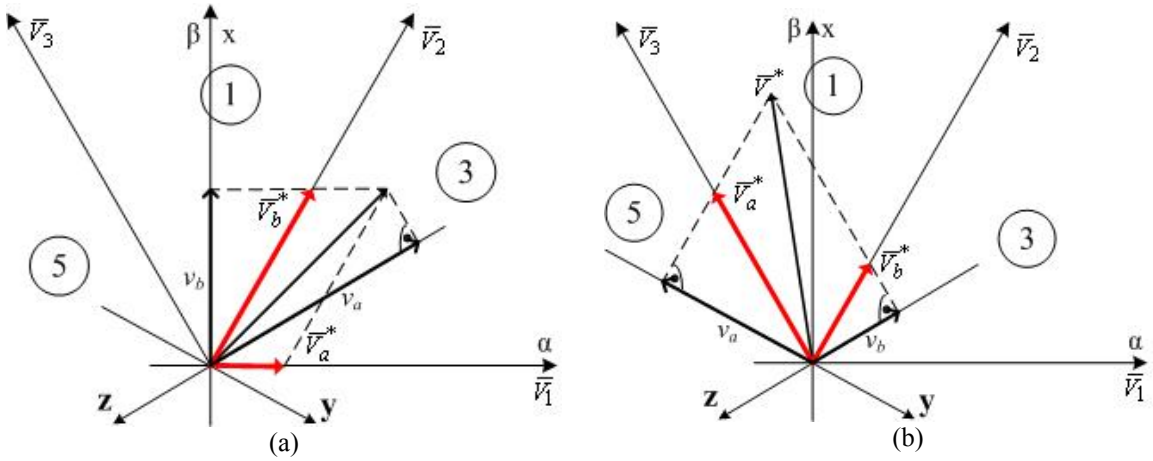


Fig. 12. Calculation of the relative application times in xyz-axes for sectors (a) "3" (sector I) and (b) "1" (sector II).

However relative application times for reference in sector different from sector I can be calculated directly. To calculate relative application time it should be calculated *xyz*-axis projection of the vector. E.g. to calculate t_b simply note that vector v_b becomes projected with 90° to the axis x. From the Fig. 9 and Fig. 12 values v_x, v_y, v_z can be used for the calculation of the relative application times since they are making 30° angle with the *abc*-system same as $2V_{dc}/3$ with respect to base voltage $V_{BS} = V_{dc}/\sqrt{3}$

$$\begin{aligned} v_x &= v_\beta = t_b, \\ v_y &= \frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^* = t_a, \\ v_z &= -\frac{\sqrt{3}}{2} v_\alpha^* - \frac{1}{2} v_\beta^* = -t_a - t_b \end{aligned} \tag{36}$$

and applied to the duty cycles calculation and their assignment:

$$\begin{aligned} d_{\min} &= \frac{t_o}{2} = \frac{1 - t_a - t_b}{2} = \frac{1 - v_x - v_y}{2} = d_c, \\ d_{mid} &= d_{\min} + t_b = d_{\min} + v_x = d_b, \\ d_{\max} &= d_{mid} + t_a = d_{mid} + v_y = d_a \end{aligned} \tag{37}$$

Finally, it should be noted that the fact that depending whether the sector is even or odd application vectors denoted as $\bar{v}_a$ and $\bar{v}_b$ alternatively swap places within the switching sequence. In the sector I the switching sequence having one commutation at a time is (000)-(100)-(110)-(111), corresponding to counterclockwise sense whereas for the sector II must be (000)-(010)-(110)-(111) corresponding to clockwise sense, with the reference to Fig. 9(a).

3.2.3. Unified modulation

A unified modulation can be interpreted as a "middle way" between carrier-based and space-vector modulation [6]. From the Fig. 13(a) it can be seen that times T_a, T_b, T_c are determined by carried-based modulation. A degree of freedom is denoted as a offset T_{off} and it is in range denoted as $[T_{off}^{(\min)}, T_{off}^{(\max)}]$:

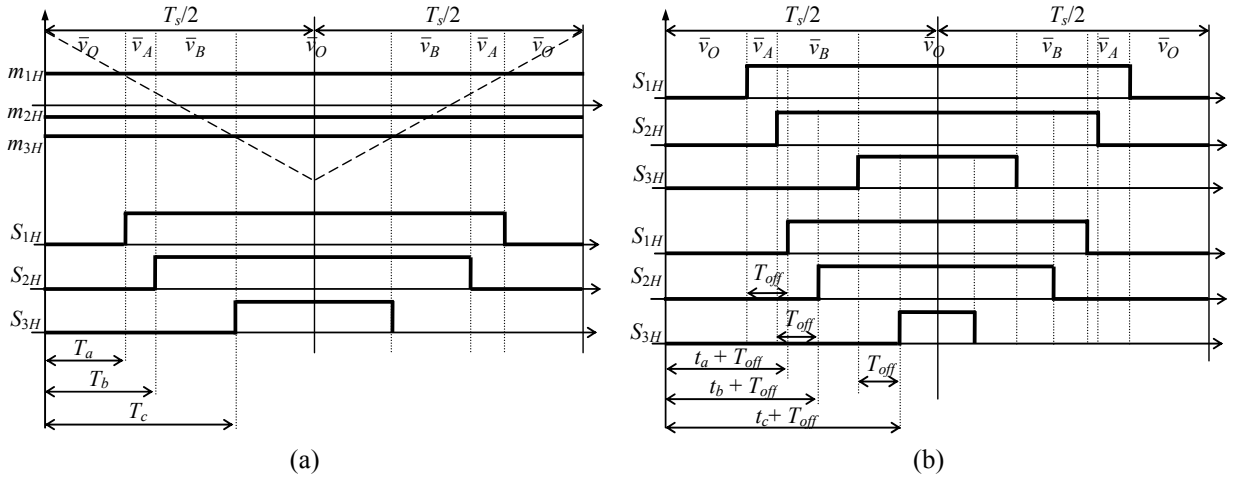


Fig. 13. Unified modulation principle: (a) duty cycles and (b) introduction of offset time.

$$-T_{\min} \le T_{off} \le T_s - T_{\max}, \tag{38}$$

where

$$T_{\min} = \min\{T_a, T_b, T_c\}, \quad T_{\max} = \max\{T_a, T_b, T_c\} \tag{39}$$

For example choosing

$$T_{off} = T_s / 2, \tag{40}$$

gives so-called sinusoidal modulation, because (38) limits reference to $V_{dc}/2$. Similarly

$$T_{off} = (T_s - T_{\max} - T_{\min}) / 2, \tag{41}$$

gives popular modulation with symmetrical distribution of zero vectors. Another example is

$$T_{off} = T_s - T_{\max}, \quad T_{off} = -T_{\min} \tag{42}$$

gives discontinuous modulation, as can be easily seen from Fig. 13(b).

3.3. PWM control methods

A nonlinear coordinate transformation with bang-bang self-control, suitable for switching on/off operation of semiconductor power devices is another approach to the control, commonly referred as direct torque control (DTC). All the modulations described above can work without knowing the nature of the system that is it is not necessary to know the property of the load: when the reference is determined, the modulation algorithm can apply it. In DTC the reference to be applied is directly calculated from the equation of the load, typically an induction or permanent magnet synchronous motor. It is possible to write voltage equation (43), where $\bar{\varphi}_s$ is the stator flux, $\bar{v}_s$, $\bar{i}_s$ and R_s are the stator voltage, current and resistance respectively [7]

$$\frac{d\bar{\varphi}_s}{dt} = \bar{v}_s - R_s \bar{i}_s, \tag{43}$$

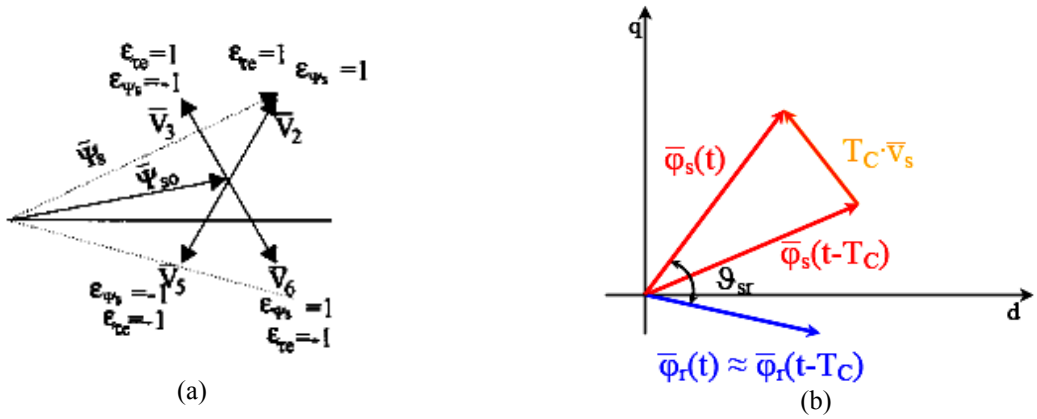


Fig. 14. Basic principle of the DTC (a) choice of the voltage vector, (b) motor control application.

Ignoring the contribution of the ohmic drop, which can be considered small in the respect of the stator voltage, the variation of stator flux can be ascribed all to the voltage applied. So, a proportional relationship between flux variation and voltage in a given period T can be found by discretizing (43).

$$\Delta\overline{\varphi}_S = T\overline{v}_S\,, \tag{44}$$

In drive applications, the stator and rotor fluxes are connected with the output torque, so it is possible to control the motor by applying discrete vectors as represented in Fig. 14(a). It is based on the low pass filter relationship between stator and rotor fluxes that assumes a fast variation of the stator flux angular speed reflecting in an increment of the angle θ_{sr}, as Fig. 14(b) schematically shows. By imposing a stator voltage value, it is possible to control either the stator flux amplitude or the torque.

The only yet published dual inverter DTC drive [8] used standard described control principle additionally applying redundancy of the available switching states in order to minimize common-mode voltage and subsequently the current. In Fig. 15 are given control tables for torque τ and flux φ hysteresis controllers required in DTC application.

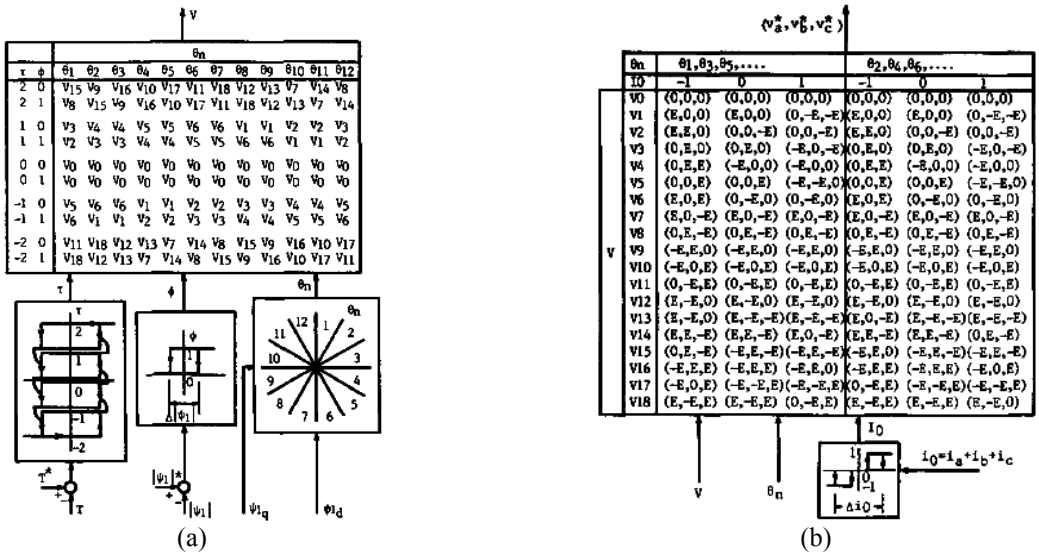


Fig. 15. DTC control tables for the dual inverter.

3.4. PWM methods carrier based

Carrier based methods are simplest for the realization, yet not always straightforward to understand. The switching state of the inverter leg is determined by comparison of the modulating signal providing information on the voltage reference, and carrier signal providing information of the switching period. As dual inverter stands between the simplest two-level and multilevel inverters that are more complex, the carrier-based modulation methods can be adopted both by extending two-level methods or applying true multilevel methods, such are level-shifted and phase shifted modulations.

3.4.1. Independent modulation

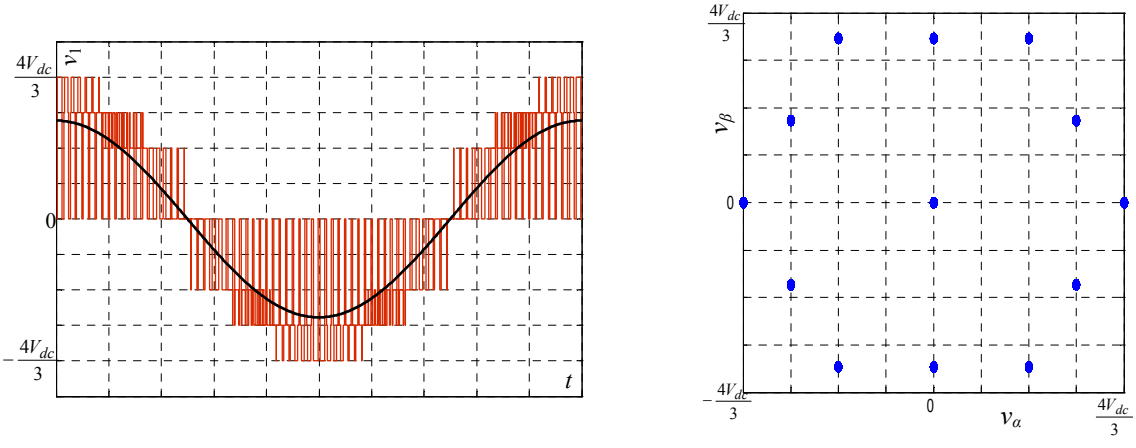
This modulation is a direct extension from single two-level method. Using (2.27) from Section 2.2, the approach as two three-phase inverters can be used to define total voltage reference *v** divided in two equal halves for inverters H and L:

$$\bar{v}_H^* = \bar{v}^*/2\,,\quad \bar{v}_L^* = -\bar{v}^*/2 \tag{45}$$

The chosen method for single inverters is the popular sinusoidal modulation with third harmonic injection, with modified references v_a^*, v_b^*, v_c^*:

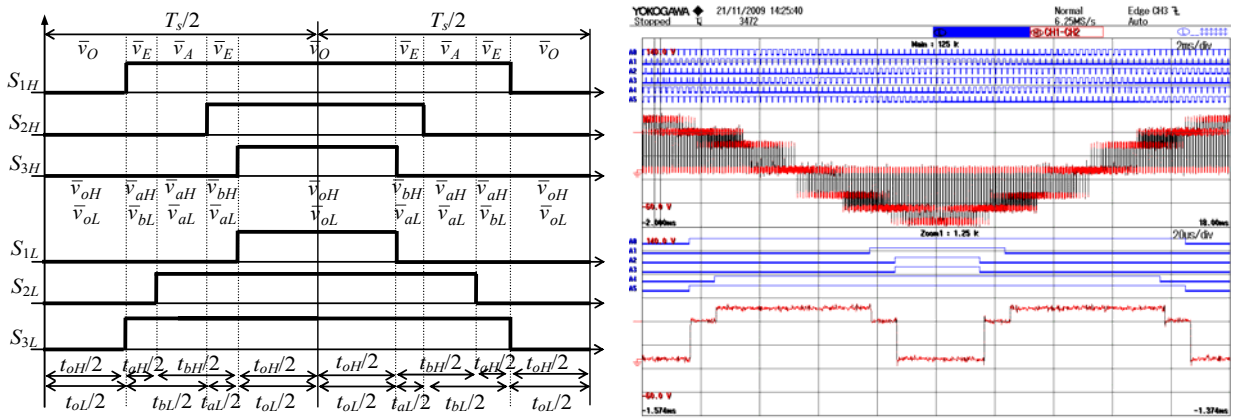
$$\begin{aligned} v_a^* &= v_A^* - (\max\{v_A, v_B, v_C\} + \min\{v_A, v_B, v_C\})/2\,,\\ v_b^* &= v_A^* - (\max\{v_A, v_B, v_C\} + \min\{v_A, v_B, v_C\})/2\\ v_c^* &= v_C^* - (\max\{v_A, v_B, v_C\} + \min\{v_A, v_B, v_C\})/2 \end{aligned} \tag{46}$$

due to its excellent performances for single inverter. However, the result is improper multilevel waveform shown in Fig. 16(a), showing large voltage excursion from maximal to minimal voltage levels. The vectors $\bar{v}_{oH}$ and $\bar{v}_{oL}$ overlap in at the beginning and the end of the switching period, as already seen in Fig. 10(c), thus forming the total zero vector $\bar{v}_O$ even for a relatively large modulating index value. For this reason, the space vector plot in Fig. 16(b) shows only



(a) (b)

Fig. 16. Independent modulation m = 0.75 (a) output voltages and (b) space vector plot.



(a) (b)

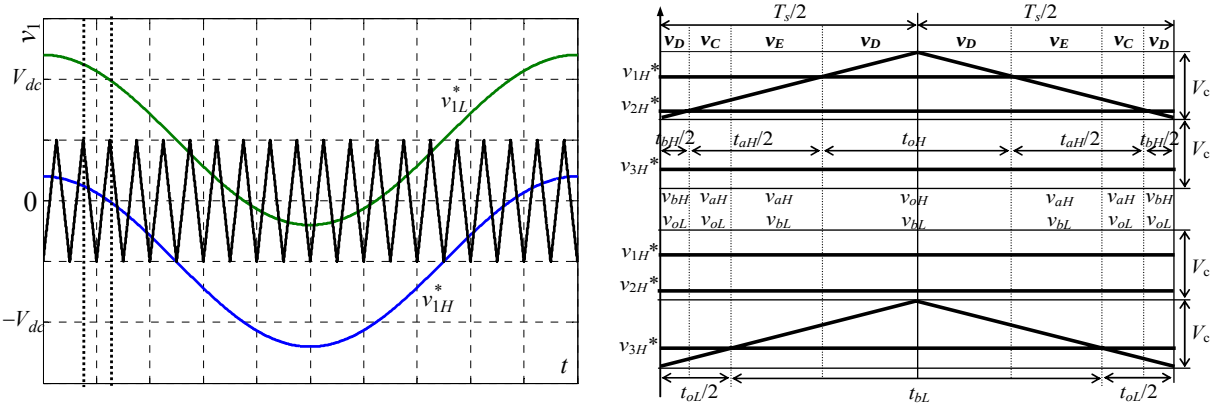
Fig. 17. Independent modulation voltage v_1 for in outer triangle ACE (a) switching pattern, (b) experimental results with zoomed detail in the outer triangle ACE, (m = 0.75, f_s = 2 kHz).

maximal vectors. Similarly, for the applied simplest proportional modulation the output would comprise all available vectors in the plot analogous as in Fig. 16(b) since there is no such distinct overlap between two switching patterns of Fig. 10(a). Both theoretical and experimental switching pattern and waveform are shown in Fig. 17.

Benefits of the method are simple modulation and large degree of freedom. The voltage references can be given independently regarding both amplitude and phase (within available dc voltage limits) [12]. This approach has been proposed for automotive applications [13], [14], setting one inverter to supply only active power whereas the other provides necessary reactive power for the drive. As a benefit, only one supply can be used since inverter providing reactive power does not need dc source.

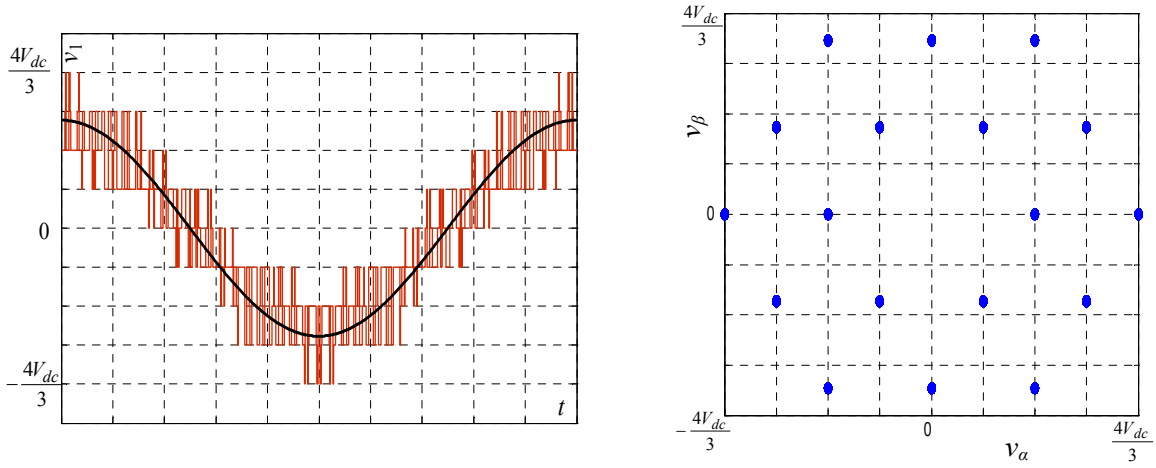
3.4.2. Level-shifted modulation

Level-shifted modulation is a general principle applied to all multilevel converters in general, where for l-levels there are (l-1) carriers shifted by l/(l-1) of the V_{dc}, so each carrier occupies its own "trace". Common modulation signals passes gradually to every carrier and in this way modulates corresponding part of the multilevel inverter, while all "lower" switches are on and "higher" are off.



(a) (b)

Fig. 18. Phase shifted modulation m = 0.75 (a) Modulation signals for the first phase and (b) waveform.



(a) (b)

Fig. 19. Level-shifted modulation $m = 0.75$ (a) output voltages and (b) space vector plot.

In practical implementation (e.g. DSP) it is more convenient to produce level-shifted modulating signals and use common carrier. The second approach described in Section 2.2. to achieve multilevel modulation is to use treatment as three single-phase choppers. However, in order to obtain proper multilevel waveform modulation signals need to be additionally adjusted. With the reference to (2.23), modulating signal v_{1S} for A- and D-leg switches will be determined, taking into account that leg voltage v_{AN} (Fig. 2.10) is always positive

$$v_{AN} \in \{V_H, 0\}, \tag{47}$$

yields that the only way for v_{1S} to take negative value is:

$$v_{AN} = 0, \quad v_{DM} = V_L. \tag{48}$$

Therefore, for given voltage reference the obtained leg voltages need to be:

$$(v_{AN}, v_{DM}) = \begin{cases} (V_H, 0), v_{1S}^* > 0 \\ (0, V_L), v_{1S}^* < 0 \end{cases}. \tag{49}$$

The modulation can be achieved by using common triangular carrier and references

$$\begin{aligned} v_{1H}^* &= mV_{dc}\cos\theta - V_{dc}/2, \\ v_{1L}^* &= mV_{dc}\cos(\theta - \pi) - V_{dc}/2, \end{aligned} \tag{50}$$

as illustrated in Fig. 18(a), taking in account that for the inverter L modulation logic has to be opposite to provide corresponding negative values. A detailed switching period for $\bar{v}^*$ inside OCD triangle is depicted in Fig. 18(b). Due to the symmetry, analogous conclusions will be valid for the remaining modulating signals v_{2S} and v_{3S} of B-E and C-F-leg switches respectively.

The resulting proper multilevel output voltage is depicted in Fig. 19(a), and the space vector plot in Fig. 19(b) shows all applied levels. Note that one of the inverters (H) applies all three NTVs ($\bar{v}_{aH}$, $\bar{v}_{bH}$, $\bar{v}_{oH}$), while the other uses just two of them ($\bar{v}_{bL}$, $\bar{v}_{oL}$). Yields that period-averaged vectors $\bar{v}_H$ and $\bar{v}_L$ cannot be collinear. In Chapter IV will be shown that the omission of the one of the active vector is actually stipulated by the demand of proper multilevel waveform. There are more solutions for this modulation, depending on the chosen modulating signals, carriers, symmetry of carriers for inverters H and L like in Fig. 20 and Fig. 21.

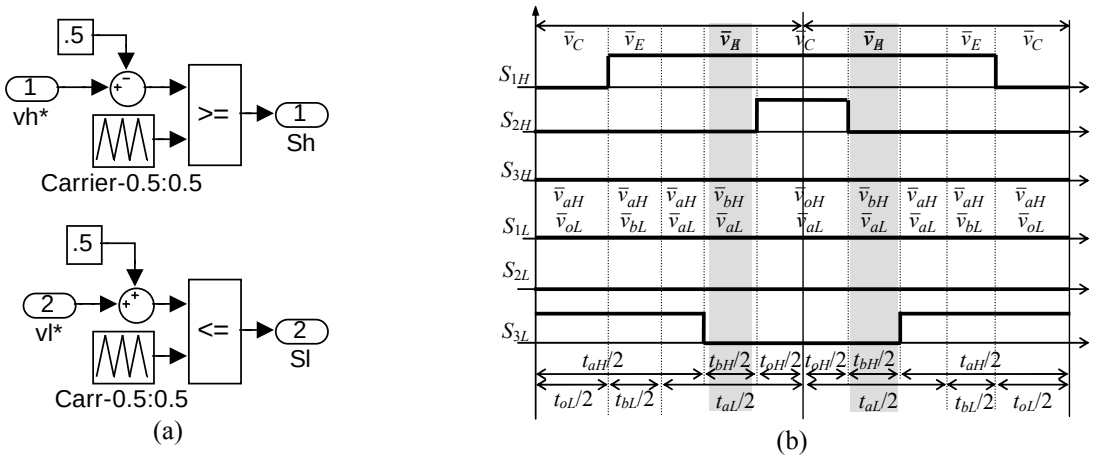


Fig. 20 Level-shifted modulation (a) modulator (b) switching pattern, $m = 0.8$.

3.4.3. Phase-shifted modulation

Phase-shifted modulation is based on the harmonic analysis of PWM signals given in more details in the appendix. The principle of the method is to phase shift carriers by $2\pi/(l\text{-}1)$, where l is the number of the voltage levels by each leg. Using harmonic result for single two-level inverter

$$v(\theta_r,\theta_c)=\frac{E}{2}m\cos\theta_f+\frac{E}{\pi}\sum_{c=1}^{\infty}\frac{1}{c}(\cos c\pi-J_0(c\pi m))\sin c\theta_c+$$
$$+\frac{E}{\pi}\sum_{c=1}^{\infty}\frac{1}{c}\sum_{\substack{f=-\infty\\ f\neq 0}}^{\infty}J_f(c\pi m)\sin(f\frac{\pi}{2}-(c\theta_c+f\theta_f)) \tag{51}$$

and output voltage expressions from Section 2.2, it is possible to set phase shift in order to obtain output voltage free of some harmonics that existed in single inverter cases. For example phase shifting by 180° (phase opposition [15]) cancels sideband harmonics around even c. However, the harmonic analysis is behind the scope of this work, while the major concentration is on the proper multilevel waveform so this method will be not discussed further.

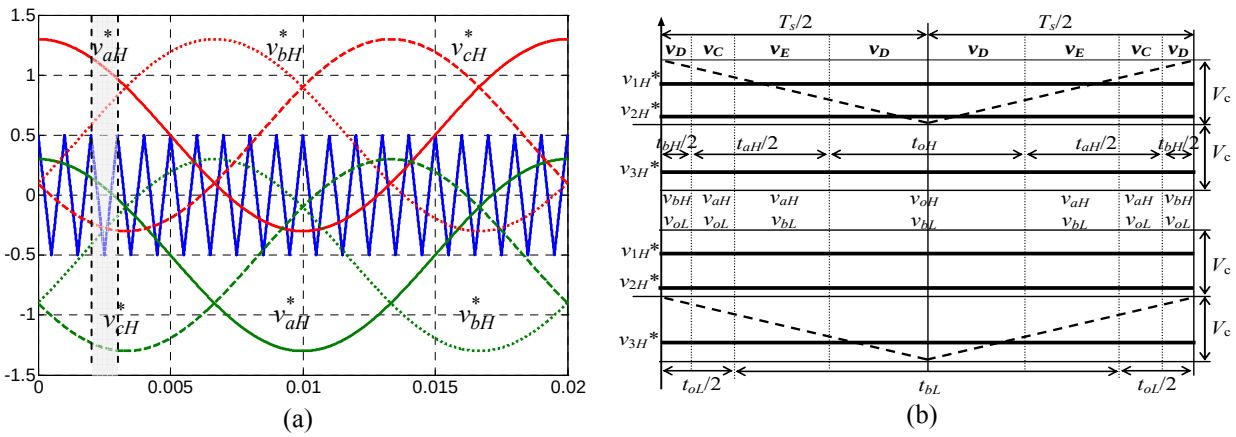


Fig. 21. Phase-shifted modulation (m = 0.75, f_s = 5 kHz) with: (a) modulation signals and carrier, (b) zoomed switching period with the reference vector in the outer triangle ACE.

3.5. PWM methods space vector

The first space vector modulation for dual inverter was proposed almost simultaneously in 2001 for dual inverter [16] and diode-clamped inverter [17]. The method (also called decomposition [18]) has been further varied [19]-[21] and improved [22], [23]. Recently, a different approach was developed, based on "full" space vector modulation of both inverters [24]. In this section, a configuration with two isolated power supplies will be discussed, whereas the single supply is addressed in the next section.

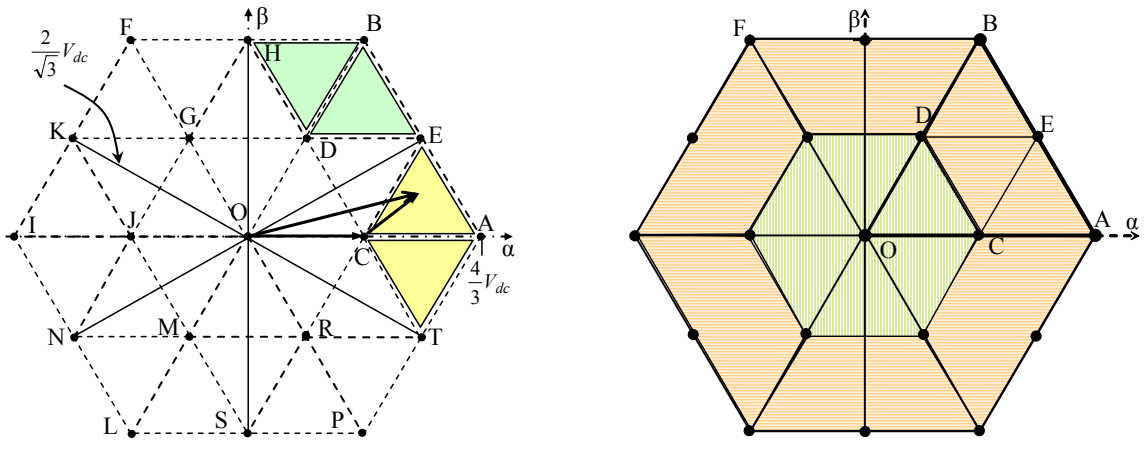
3.5.1. Composition of switching periods

The complexity of dual inverter modulation can be considerably simplified considering the space vector plot as composed of six smaller "hexagons", each one equal as the plot of the single two-level inverter, plus additional such central hexagon, as shown in Fig. 22(a). The centers of these six hexagons (such is AEDORT) are located on the apexes of the very central hexagon CDGJMR. Each two-level hexagon is shifted with respect to the origin of the three-level hexagon by the vector with amplitude equal to $2V_{dc}/3$. A particularly convenient case for the composition method is an asymmetrical dual inverter, with one inverter having much higher power rating than the other. In this configuration the larger inverter can conveniently work in six-step mode (i.e. fundamental switching mode), while the inverter with lower ratings is modulating [25].

The authors [16] had distinguished two general areas: inner and outer, as shown in Fig. 22(b). For example in the triangle OCD inside the inner area the proper switching pattern would be:

$$0\overline{0}\,|\,0\overline{5}\,|\,0\overline{4}\,|\,0\overline{7}\,\|\,0\overline{7}\,|\,1\overline{7}\,|\,2\overline{7}\,|\,7\overline{7}\,\|\,7\overline{7}\,|\,7\overline{4}\,|\,7\overline{5}\,|\,7\overline{0}\,\|\,7\overline{0}\,|\,2\overline{0}\,|\,1\overline{0}\,|\,0\overline{0}\,|\,. \tag{52}$$

The used vector notation is already explained in section 2.3; one vertical line denotes transitions (commutations) between vectors, and two such lines the end of the switching period. The



(a) (b)

Fig. 22. Voltage vector plot: (a) space vector representation of six two-level hexagons with vector composition principle, (b) subdivision to inner and outer sectors.

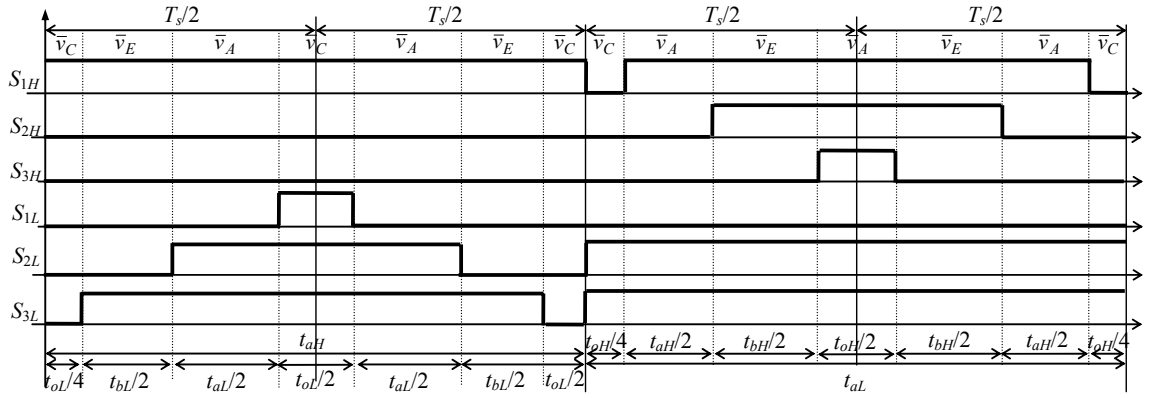


Fig. 23. Composition of switching periods with continuous modulation for intermediate triangle ACE.

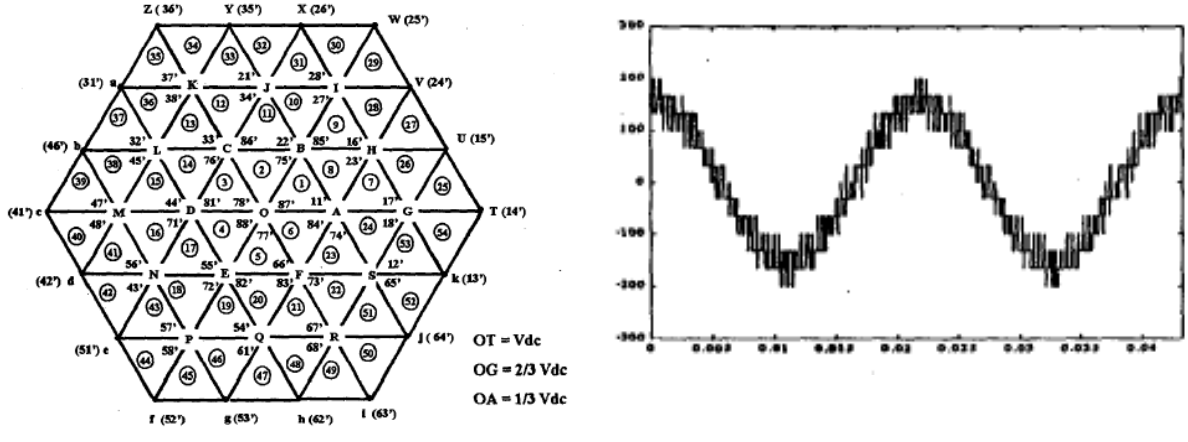
proposed sequence provides both one-leg-switching transition between vectors and symmetrical switching of both single inverters.

However, for triangle in outer area, e.g. CDE, the biggest vectors have lower redundancy, in this case $\bar{v}_E$ can be composed by two combinations only, $1\bar{5}$ and $2\bar{4}$. So these combinations are determining that $\bar{v}_H$ has to be fixed to vectors 1 or 2, and $\bar{v}_L$ to $\bar{4}$ or $\bar{5}$ leading to the sequence:

$$1\bar{0}\,|\,1\bar{5}\,|\,1\bar{6}\,|\,1\bar{7}\,||\,0\bar{4}\,|\,3\bar{4}\,|\,2\bar{4}\,|\,7\bar{4}\,||\,2\bar{7}\,|\,2\bar{4}\,|\,2\bar{3}\,|\,2\bar{0}\,||\,7\bar{5}\,|\,6\bar{5}\,|\,1\bar{5}\,|\,0\bar{5}\,|\,, \tag{53}$$

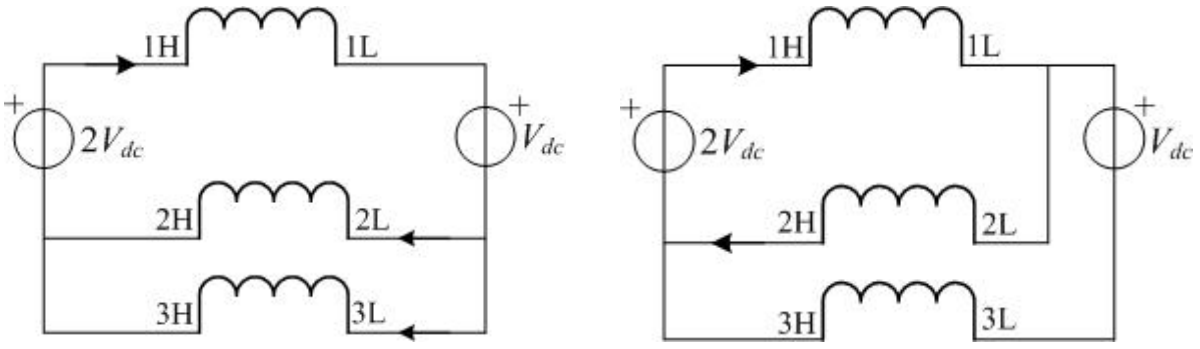
with double simultaneous commutation when one fixed vector replaces another, precisely at transitions: $1\bar{7}$ - $0\bar{4}$, $4\bar{4}$ - $2\bar{7}$ etc. Analogously the same vectors will have to be fixed for the other triangles in outer belt e.g. ACE and BDE leading to the similar vector sequence. As a result, there is a pulse in each of the two switching periods for some phases and multiple simultaneous commutations. Therefore, Authors' claim "*The scheme proposed here makes the individual inverter switching frequency equal to half of the motor phase switching frequency*" is not true, as can be seen from Fig. 23 for signal S_{1H}.

The same modulation principle can be applied to the dual inverter with dc-voltage ratio 2:1 ($2V_{dc}/3$ and $V_{dc}/3$) [19]. The obtained vector plot has same number of levels as a four-level inverter, and can be divided in 54 triangles as shown in Fig. 24, which can be further grouped in inner hexagon (6 triangles), intermediate belt (18 triangles) and outer triangles (30 triangles). These areas correspond to five-level, nine-level and 13-level output, since the configuration adds



(a) (b)

Fig. 24. Dual inverter with dc voltage ratio 2:1 (a) space vector plot for, (b) output voltage waveform.



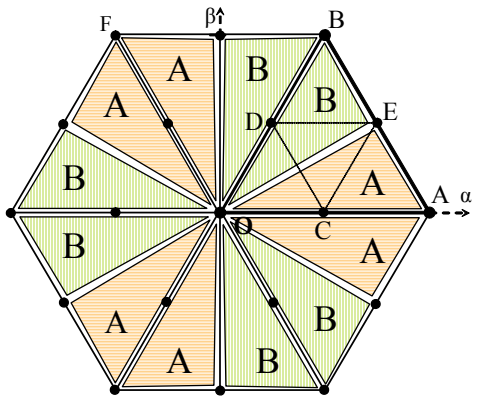
(a) (b)

Fig. 25. Illustration of the two vector switching combinations leading to the asymmetrical load: (a) $1\overline{4}$ charging V_L, (b) $1\overline{5}$ supply only from V_H.

in total four new phase voltage levels (two positive and two negative) compared to dual inverter with equal dc-voltages. All 13 levels correspond to the voltage reference in outer triangles and can work in 18-step mode in overmodulation (analogously to six-step mode for 2-level inverter when each six active vectors are applied for 1/6 of a period). In addition, six-step and 12-step modes can be applied if necessary, although not corresponding to overmodulation [19].

It should be noted that due to inherit asymmetry of the configuration the second dc supply need to be have a regenerative or dynamic breaking, otherwise the higher voltage supply ($2V_{dc}$) could overcharge the dc-link of the lower converter. The reason is that in switching combinations with equal corresponding states (e.g. $1\overline{4}$, $2\overline{5}$ etc.) two sources become connected in parallel, leading to charging of the lower source Fig. 25(a). However these combinations are forming zero vector $\overline{v}_O$ and can be avoided. In combinations with only one leg state equal ($1\overline{5}$, $1\overline{6}$ etc.) lower supply does not contribute with the current Fig. 25(b) creating a possible unbalance.

In order to reduce the problem of the double instantaneous commutations was proposed the division in six areas denoted “A” and “B” [22], as shown in Fig. 26(a). By this dissection, the fixed vector transition between inverters that created simultaneous commutations problem is reduced to only six times within whole output cycle. Each inverter is fixed for one sixth of the output cycle, instead of swapping them after each switching period. Note that only two coordinates are determining the sector, but they are of the same sign, therefore determining the



	Sector number						
Quantity		1	1+2	2	2+4	4	1+4
	V_a	**>0**	>0	<0	**<0**	<0	>0
	V_b	<0	>0	**>0**	>0	<0	**<0**
	V_c	<0	**<0**	<0	>0	**>0**	>0

(a) (b)

Fig. 26. Proposed switching sequences for triangles (a) inner OCD, (b) outer ACE.

Tab. 1. Switching states and leg output voltages for three-level cascaded inverter.

Total vector $\bar{v} = \bar{v}_H + \bar{v}_L$	Inverter H vector $\bar{v}_H$	Inverter L vector $\bar{v}_L$
$\bar{v}_a = \bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_0$
	$\bar{v}_0$	$\bar{v}_\alpha$
$\bar{v}_b = \bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_0$
	$\bar{v}_0$	$\bar{v}_\beta$
$\bar{v}_c = \bar{0}$	$\bar{v}_0$	$\bar{v}_0$

sign of the remaining coordinate (the sum is zero). Introducing "code 1" for v_x positive and "code 0" for v_x negative, sectors can be coded with binary numbers, since there are $2^3 = 8$ combinations and (0, 0, 0) and (1, 1, 1) are impossible. The coding table is given in Fig. 26(b).

The Authors [23] also introduced a concept of "common-mode voltage", developed as an analogy from two-level inverter. This analogy is indirect since there is no single negative pole but two. The common mode voltage is defined as a difference between middle points of the two dc-sources, but in the case of the equal dc-voltages, as here, it is identical as v_{NM}. It was noted that maximum and minimum v_{NM} is achieved with switching contribution combinations" $7\bar{0}$ and $0\bar{7}$ respectively. These combinations can be avoided in proposed modulation as an advantage compared to (52), where these were used extensively. Common-mode voltage will be explained in more details in the Section 6 of this chapter.

3.5.2. Full space vector modulation

In [24] "full" space vector modulation of both inverters was proposed, derived from the popular method of space vector modulation from single two-level inverter. Whole vector plot is divided in six equal triangles like OAB, and further each such triangle is divided in three different region types with representative triangles OCD, CDE and ACE, respectively, depicted in Fig. 26(a). The NTV corresponding to the triangle in case are denoted as $\bar{v}_a$, $\bar{v}_b$, and $\bar{v}_c$, and vectors of the two single triangles are denoted as $\bar{v}_\alpha$, $\bar{v}_\beta$, and $\bar{v}_0$, with mutual correspondence given in Tab. 1.The principle for calculating the relative duty cycles is explained in Fig. 27(a): use of the dot product provides ratio of orthogonal (scalar) projections on the direction of vector $j\bar{v}_\beta^*$:

$$\alpha_H = \frac{|OF|}{|OE|} = \frac{|OH|}{|OG|} = \frac{|OH| \cdot \left| j\bar{v}_\beta^* \right|}{|OG| \cdot \left| j\bar{v}_\beta^* \right|} = \frac{\bar{v}_H^* \cdot j\bar{v}_\beta^*}{\bar{v}_\alpha^* \cdot j\bar{v}_\beta^*}. \tag{54}$$

Similarly can be obtained

$$\beta_H = -\frac{\bar{v}_H^* \cdot j\bar{v}_\alpha^*}{\bar{v}_\alpha^* \cdot j\bar{v}_\beta^*} \tag{55}$$

and simple remaining part for the zero vector:

$$\gamma_H = 1 - \alpha_H - \beta_H \tag{56}$$

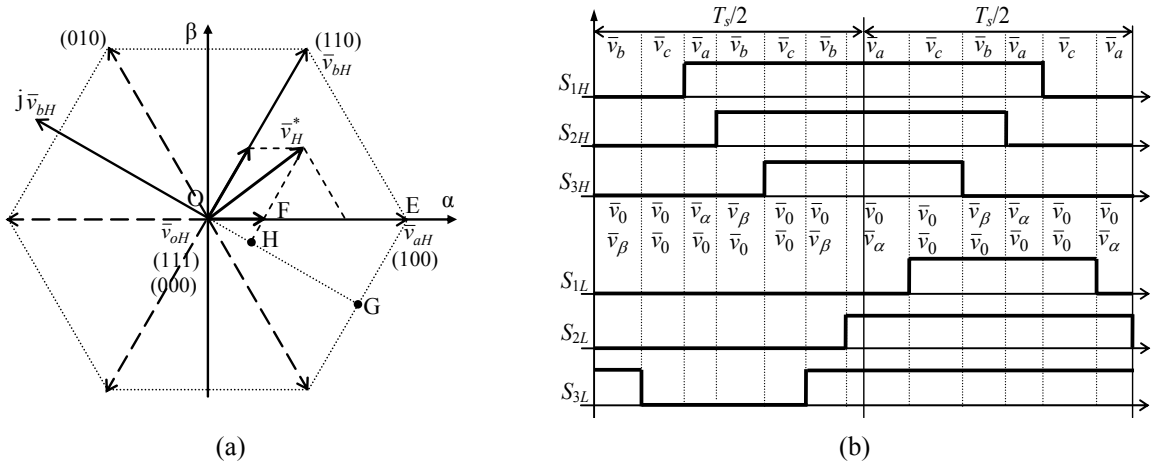


Fig. 27. Space vector modulation (a) duty cycle calculation, (b) proposed switching for inner OCD.

Proposed modulation patterns for different triangle cases are given in Fig. 27(b), Fig. 28(a) and (b), respectively. It can be seen that all pattern provide proper multilevel voltage since they are producing NTV, i.e. vertices of the corresponding triangles.

However, a significant drawback is the asymmetry of the proposed patterns that makes them difficult to be implemented in standard PWM unit of the DSP. Standard DSP unit is usually made for three-phase application and has common carrier for all three phases. This means that it cannot generate arbitrary switching pattern, but only patterns with fixed position of one of the zero output vectors (0, 0, 0)/(1, 1, 1). In this case, patterns are requiring three independent carriers for each single inverter that can be implemented by field programming gate array circuit (FPGA) adding significant complexity to the implementation. Also from the harmonic quality standpoint, the patterns are far from optimal due to strong asymmetry.

3.6. PWM methods for single supply

Modulation techniques for a single supply dual inverter with zero-sequence filter are identical as for separately supplied, as treated in Section 2.4. However, if hardware filter is omitted special

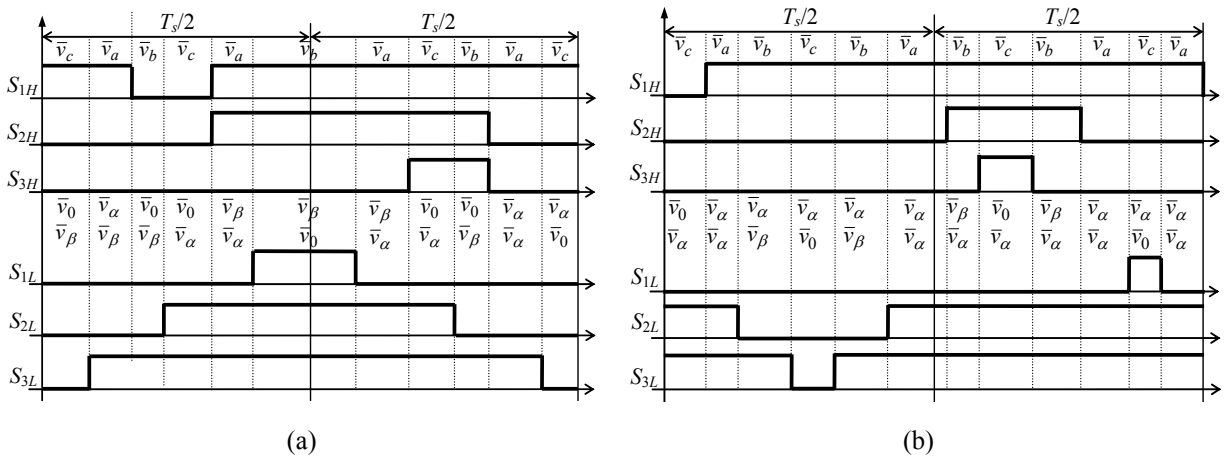


Fig. 28. Proposed switching sequences for triangles (a) intermediate CDE, (b) outer ACE.

modulation techniques need to be applied to suppress the circulation of zero-sequence current. Zero-sequence voltage (called by authors "third harmonic") is defined in a standard manner [26]:

$$v_0 = \frac{v_1 + v_2 + v_3}{3}, \tag{57}$$

All possible values for v_0 are presented in Tab. 2.

3.6.1. Scheme with auxiliary switches

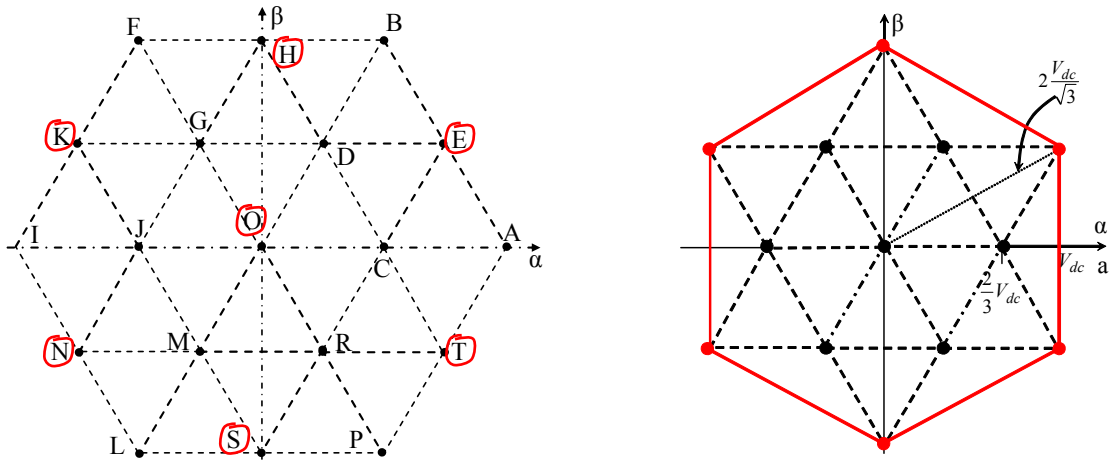
As can be seen from Tab. 2 only seven of total 19 vectors are not contributing to zero-sequence voltage, and they are denoted in Fig. 29(a). First, none of the intermediate vectors v_C, v_D, v_G, v_J, v_M, v_R can be applied, leading to output voltage waveform without multilevel quality. Second, vectors v_A, v_B, v_F, v_I, v_L, v_P with maximum amplitude are not included leading to lower output voltage. It can be noted that the first group of vectors contains zero parts (0, 7, $\overline{0}$, $\overline{7}$) in switching combination, whereas the second does not. To be concluded, application of only zero-sequence-free vectors v_E, v_H, v_K, v_N, v_S, v_T represents a poor solution, as proposed in [27]. Similar modulation has been proposed in [28] with consideration of two single common-mode voltages:

$$v_{0H} = \frac{v_{1H} + v_{2H} + v_{3H}}{3}, \; v_{0L} = \frac{v_{1L} + v_{2L} + v_{3L}}{3} \tag{58}$$

From the total of 20 switching combinations with $v_0 = 0$, only one of them ($0\overline{0}$) has single zero-common voltages $v_{0H} = v_{0L} = 0$. All the other 19 vectors have simply $v_{0H} = v_{0L} \neq 0$, giving as a result:

$$v_0 = v_{0H} - v_{0L} = 0, \tag{59}$$

Although these 19 vectors do not introduce zero-sequence current, they are having common-mode voltage different from zero leading to the known problems of EMI and motor bearings. These common mode voltages do not cause the zero sequence currents in the machine phase windings, as at every instant the common mode voltages generated by the individual inverters are equal and appear at the opposite ends of the windings. However, common mode voltages generated by the single inverters can couple to the stator frame and rotor frame causing undesir-



(a) (b)

Fig. 29. Single supply dual inverter (a) vectors without zero-sequence contribution, (b) obtained output.

Tab. 2. Zero-sequence voltage for all switching combinations of dual inverter with a single supply.

	Zero-sequence voltage v_0						
Switching Combination	$-V_{dc}$	$-2V_{dc}/3$	$-V_{dc}/3$	0	$V_{dc}/3$	$2V_{dc}/3$	V_{dc}
	$0\overline{7}$	$0\overline{1}$	$0\overline{2}$, $0\overline{4}$, $0\overline{6}$	$1\overline{2}$, $1\overline{4}$, $1\overline{6}$	$1\overline{0}$	$2\overline{0}$	$7\overline{0}$
		$0\overline{3}$	$1\overline{1}$, $1\overline{3}$, $1\overline{5}$	$2\overline{2}$, $2\overline{1}$, $2\overline{3}$	$2\overline{1}$, $2\overline{3}$, $2\overline{5}$	$4\overline{0}$	
		$0\overline{5}$	$2\overline{7}$,	$3\overline{2}$, $3\overline{4}$, $3\overline{6}$	$3\overline{0}$	$6\overline{0}$	
		$1\overline{7}$	$3\overline{1}$, $3\overline{3}$, $3\overline{5}$	$4\overline{1}$, $4\overline{3}$, $4\overline{5}$	$4\overline{2}$, $4\overline{4}$, $4\overline{5}$	$7\overline{2}$	
		$3\overline{7}$	$4\overline{7}$,	$5\overline{2}$, $5\overline{4}$, $5\overline{6}$	$5\overline{0}$	$7\overline{4}$	
		$5\overline{7}$	$5\overline{1}$, $5\overline{3}$, $5\overline{5}$	$6\overline{1}$, $6\overline{3}$, $6\overline{5}$	$6\overline{2}$, $6\overline{4}$, $6\overline{6}$	$7\overline{6}$	
			$6\overline{7}$,	$0\overline{0}$, $7\overline{7}$,	$7\overline{1}$, $7\overline{3}$, $7\overline{5}$		

able bearing currents and leakage currents as in the case of the conventional PWM inverters.

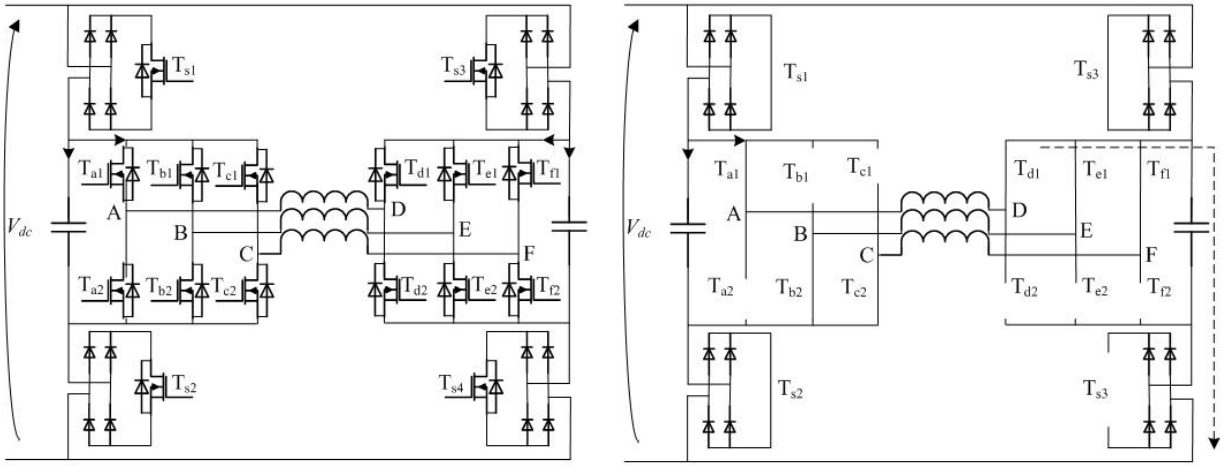
A goal of the proposed PWM scheme is to eliminate these common mode voltages generated by the individual inverters, by obtaining constant v_{0H} and v_{0L}. In this way, the problems related to the common-mode voltage would be minimized since the capacitive couplings are insensitive to the constant common mode voltage. Note that all leg potentials v_{1H}, v_{2H}, v_{3H}, v_{1L}, v_{2L}, v_{3L} have non-negative potential with respect the negative pole O, leading to the classification of 19 vectors in two major groups of nine vectors and additional group with just one vector:

- $v_{0H} = v_{0L} = V_{dc}/6$, with vectors $1\overline{2}$, $1\overline{4}$, $1\overline{6}$, $3\overline{2}$, $3\overline{4}$, $3\overline{6}$, $5\overline{2}$, $5\overline{4}$, $5\overline{6}$, belonging to this group
- $v_{0H} = v_{0L} = V_{dc}/3$, with vectors $2\overline{1}$, $2\overline{3}$, $2\overline{5}$, $4\overline{1}$, $4\overline{3}$, $4\overline{5}$, $6\overline{1}$, $6\overline{3}$, $6\overline{5}$, belonging to this group
- $v_{0H} = v_{0L} = V_{dc}/2$, with vector $7\overline{7}$ belonging to this group

Because of all these methods output voltage amplitude is equal as for a single two-level inverter, as shown in Fig. 29(b), and same waveform as two-level inverter. Furthermore, there are simultaneous commutations.

It may be noted that the state assumed by inverter-L is either lagging or leading that of the state assumed by inverter-H by an angle of 120º. For example, when inverter-H assumes the state '1' i.e. (1, 0, 0), inverter-L assumes either the state '2' (0, 0, 1) as in the first set or the state '4' (1, 1, 0) as in the second set. This explains why the harmonic voltages of the triplen order are eliminated in the phase voltage of the dual inverter scheme when a switching takes place amongst these combinations. A phase difference of 120º between the fundamental components of the individual inverter outputs corresponds to a phase difference of 3n120º, i.e. an integral multiple of 360º, for the triplen harmonics. Thus, the phase voltage of the dual inverter scheme obtained by taking the difference of the pole voltages of the individual inverters does not contain the voltage harmonics of the triplen order.

Using the presence of zero vectors in the first vector group, Authors [26] have proposed a modified hardware structure introducing auxiliary controllable bidirectional switches, as shown in Fig. 30(a) where they are denoted with T_{S1}-T_{S4}. These switched actually provide a configuration with two isolated supplies but in a temporary manner – using capacitors as an auxiliary supply for a short period. All auxiliary switches are normally closed therefore does not



(a) (b)

Fig. 30. Dual inverter with auxiliary switches (a) topology, (b) equivalent state for vector $1\bar{0}$.

affecting the function of the converter. However when one of the intermediate vectors is to be applied the switching combination which includes zero vector is used, and the complementary auxiliary switch is turned off thus preventing zero-sequence current. As an example, when v_C is realized by vector combination $1\bar{0}$ auxiliary switch T_{S4} is simultaneously opened thus disabling zero-sequence current path, as illustrated in Fig. 30(b) with dashed line. This opening is possible since current of the some of the inverter current is zero and that does not affect the capacitor. However, the same principle cannot be applied to six biggest vectors v_A, v_B, v_F, v_I, v_L, v_P since they do not contain zero in their combinations and opening of the switches would affect corresponding capacitor. As a result, obtained voltage amplitude is reduced as shown in figure Fig. 29(b) (7-level output maximum). The applied modulation algorithm wass switching periods composition already presented in [16], and derived in more details in [29]. However, the drawback of multiple simultaneous commutations from [16] remains.

For the second group of vectors, a different switching algorithm was proposed for converter from Fig. 30(a) simply chopping auxiliary switch pairs S_1-S_2 and S_3-S_4 all the time [30]. The switching is fixed at 50 % duty cycle for symmetry, without required control. Any possible zero-sequence current is avoided by introduction of the deadtime for both auxiliary switches of the same leg. In this way, the converter practically becomes with two insulated supplies. The ripple in the voltage across the dc-link capacitors in the present scheme always corresponds to the switching frequency of the auxiliary switches. Authors claim that this does not influence capacitors so much, since frequency of the switching is "high" (500 Hz), which is on the order above the maximum frequency which would discharge dc-link capacitors in a conventional neutral clamped three-level inverter.

3.6.2. Average zero-sequence voltage

Instead of annulling instantaneous values of zero-sequence voltage, as for the previous solution, in [31]-[33] have been proposed a modulation method based on the period composition with average zero-sequence voltage equal to zero (over the switching period). The obtained

voltage can be easy filtered by the load (e.g. motor, inductance) or an addition of small zero-sequence inductance. Application times of the vectors T_a, T_b, and T_o are determined by (18), the only degree of freedom is sharing of T_o between two zero vectors (0, 0, 0) and (1, 1, 1). As an illustration for reference vector in CDE switching sequence determined in the subsection 5.1

$$1\bar{0}\,|\,1\bar{3}\,|\,1\bar{2}\,|\,1\bar{7}\,\|\,0\bar{4}\,|\,3\bar{4}\,|\,2\bar{4}\,|\,7\bar{4}\,\|\,2\bar{7}\,|\,2\bar{4}\,|\,2\bar{3}\,|\,2\bar{0}\,\|\,7\bar{5}\,|\,6\bar{5}\,|\,1\bar{5}\,|\,0\bar{5}\,|\,, \tag{60}$$

Within the first switching period applied vectors $1\bar{0}$, $1\bar{3}$, $1\bar{2}$, $1\bar{7}$ have zero-sequence voltage contributions: $V_{dc}/3$, $-V_{dc}/3$, 0, and $-2V_{dc}/3$ respectively, shown in figure Fig. 31(a). The average zero-sequence voltage will be:

$$v_0 = xT_0(V_{dc}/3) + T_a 0 + T_b(-V_{dc}/3) + (T_0 - xT_0)(-2V_{dc}/3)\,, \tag{61}$$

yielding:

$$v_0 = (xT_0 - (T_b + 2T_0)/3)V_{dc}\,, \tag{62}$$

In order to have zero-sequence average value equal to zero must be:

$$xT_0 = (T_b + 2T_0)/3\,, \tag{63}$$

giving also the limitation of the method:

$$T_b \le T_0\,, \tag{64}$$

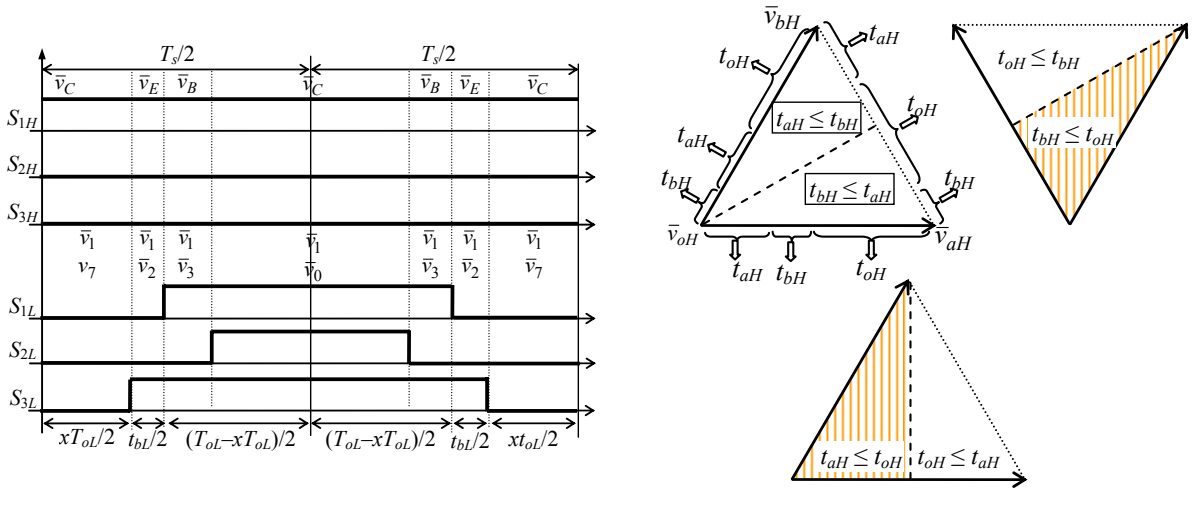
This limits the output voltage to seven-level output excluding the maximum vectors v_A, v_B, v_F, v_I, v_L, v_P. As has been explained in Subsection 2.3, parameter T_{off} can be used here to provide desired average zero-sequence voltage determines. Taking into account that application time of the first zero vector already contains T_{min} the parameter is:

$$T_{off} = (1-x)T_o - T_{\min}\,, \tag{65}$$

which applying (63) gives:

$$T_{off} = T_s/3\,, \tag{66}$$

Similarly, the T_{off} times can be calculated for the OFF sequence in the other sectors also and this works out to be equal to $T_s/3$ irrespective of the sector in which the tip of the reference vector is located. This means that a simple relocation of the effective application time within the



(a) (b)

Fig. 31. Zero-sequence average modulation (a) switching pattern calculation (b) vector areas with time inequalities.

switching period eliminates the zero-sequence voltage in the average sense. However, such a non-centre-spaced PWM results in a higher current ripple and consequently a higher THD [2].
The limitation from (64) can be graphically interpreted in Fig. 31(b). Inside triangle CDE the limitation is (64) which due to the symmetry does not bring the limitation, however inside ACE it gives:

$$T_a \leq T_0, \tag{67}$$

3.7. PWM techniques for double supply

PWM techniques do not generally differ between single supply dual inverter with zero-sequence filter and separate supplied dual inverter. However, separate supply configuration introduces two dc voltages that might need to be balanced. In addition, there is a degree of freedom in how two sources will be treated.

3.7.1. Control strategies

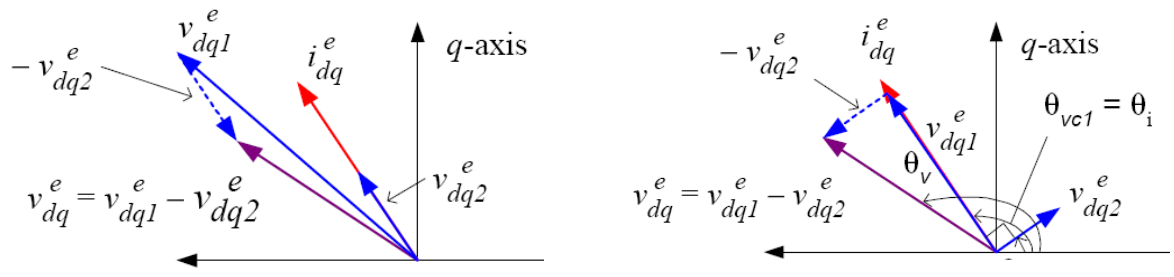
The power balance equation for dual inverter with isolated supplies is simple

$$p = p_H + p_L, \tag{68}$$

where p is the output power of the dual inverter and p_H, p_L are the powers of the single inverters. For a given output power (68) shows that dual inverter possess a degree of freedom between two power sources, enabling different control strategies to be introduced. Only the few most popular strategies will be briefly described.

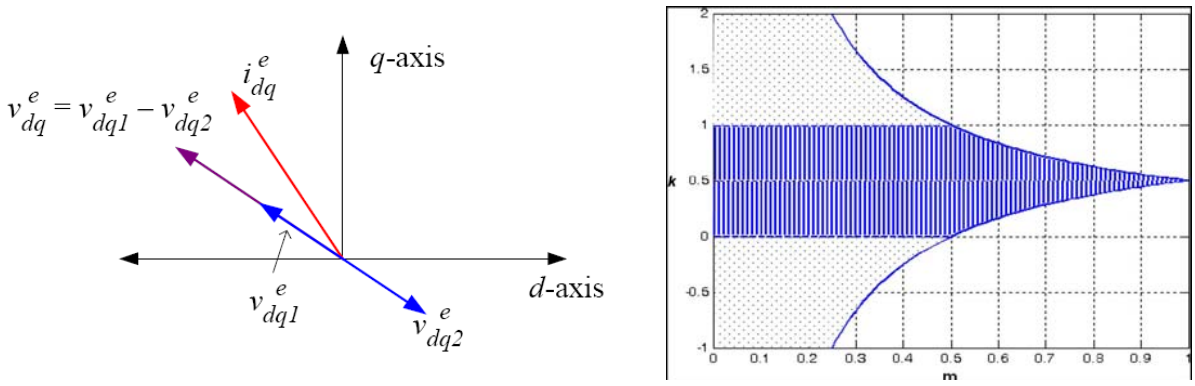
In order to maximize power flow of the one of the sources in [12] was proposed method called "unity power factor control". If one of the sources needs to supply or receive the maximum power, the power factor of the corresponding inverter is kept to one, as illustrated in Fig. 32(a), which shows charging of the second source. Similarly, as reference voltage of the first inverter decreases the state of maximum load (discharge) for the power source can be reached, with voltage and current vectors having the opposite sense.

Another possible strategy is to supply all the power from the first inverter, therefore saving on the second source. However, the second inverter requires dc capacitors as energy storage. This strategy is called "voltage quadrature control" [12], [13] and is depicted in Fig. 32(b).



(a) (b)

Fig. 32. Dual inverter with double supply phasor diagram for (a) secondary source charging, (b) quadrature control.



(a) (b)

Fig. 33. Two-level inverter with delta connected load (a) Phasor diagram with INVR1 and INVR2 producing maximum output and (b) limits of the power sharing coefficient *k* versus the modulation index m.

Nevertheless, the most important quantity to be maximized is the output voltage, with the corresponding "optimum voltage utilization" that will be described in more details. This method required voltages of the two inverters to be collinear Fig. 33(a). After the brief explanation of the principle, all proposed methods in the next Chapter will be based on this strategy.

3.7.2. Separate supplies power balancing

The reference output voltage $\bar{v}^*$ can be synthesized as the sum of the voltages $\bar{v}_H^*, \bar{v}_L^*$ generated by the two inverters, as determined in the Section 2.2. Introducing the voltage ratio *k* and imposing the inverter voltage vectors $\bar{v}_H^*$, $\bar{v}_L^*$ to be in phase with the output voltage vector $\bar{v}^*$, yields

$$\begin{cases} \bar{v}_H^* = k\,\bar{v}^* \\ \bar{v}_L^* = (1-k)\,\bar{v}^* \end{cases}, \tag{69}$$

The condition expressed by (7) allows maximum dc voltage utilization. In addition, being the output current of the two inverters the same, the coefficient *k* also defines the power sharing between the two inverters. In terms of averaged values within the switching period, the output power can be expressed as

$$p = (3/2)\bar{v}^*\bar{i} = p_H + p_L \quad \begin{cases} p_H = (3/2)\bar{v}_H^* \cdot \bar{i} = k\,p \\ p_L = (3/2)\bar{v}_L^* \cdot \bar{i} = (1-k)\,p \end{cases}, \tag{70}$$

The coefficient *k* has a limited variation range depending on the value of the reference output voltage $\bar{v}^*$, as shown in . An estimation of the coefficient *k* can be easily carried out by a simple power balance written assuming $V_H \cong V_L \cong V_{dc}^*$:

$$k = \frac{p_H}{p} = \frac{V_H I_H}{V_L I_L + V_H I_H} \cong \frac{I_H}{I_L + I_H}, \tag{71}$$

As a consequence, by combining (9) and (7) the inverter reference voltages $\bar{v}_H^*$, $\bar{v}_L^*$ can be determined as

$$\begin{cases} \bar{v}_H^* = \dfrac{I_H^*}{I_H^* + I_L^*}\bar{v}^* \\ \bar{v}_L^* = \dfrac{I_L^*}{I_H^* + I_L^*}\bar{v}^* \end{cases}, \tag{72}$$

From (69) it can be easily calculated that sharing factor k cannot be chosen arbitrarily for given modulation index m. For example if maximum output voltage is set (m equal to 1), it means that k has to be equal to 0.5 (balanced regime). It can be easily obtained

$$1-\frac{1}{2m} \le k \le \frac{1}{2m}, \tag{73}$$

with the assumption that two voltages are equal. The inequality is depicted in Fig. 33(b).

3.8. Summary

A comprehensive survey of the existing methods has been presented in this chapter. It gives both state of the art and basis for the further development of the modulations in the next chapter. The introspection has shown that major interest was dedicated to the common-supply inverter, and only lately, an isolated-supply version had received equal attention. The established reference with two-level inverter is exploited reviewing for this reason in a manner useful for the following development of the new dual inverter modulation. Furthermore, three known dual inverter modulation approaches has been established: carrier-based, composition and space vector.

Regarding the double supply, the proper modulation strategy problem has not been solved in general. Major part of the developed modulation methods work with the presumption of the balance between two inverters (two sources). A universal solution is however, the application of the independent modulation, but it has been demonstrated that it gives improper output waveform.

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4. Proposed modulation strategies for dual inverter

For dual inverter the maximum number of the commutations during the switching period is six, which leads to the seven output vectors, whereas some of them are redundant. However, from a practical point of view such modulation pattern would be increasingly complex to handle regarding proper multilevel modulation and simultaneous commutations. On the other hand, the minimum number of the commutations is two, creates three output vectors. Nevertheless, such minimalist pattern is enough to achieve the average voltage reference. If these vectors are set to as NTV the task is solved with the minimum switching losses as well. One such example is given in the previous chapter, where the output is composed within two switching periods by fixing single inverters vector and modulating the other inverter. It should be noted that the same result theoretically could be obtained by modulating only one phase of the each inverter. In any case, it has been shown that although switches does not commutate during the period they often need to commutate simultaneously at the end of the period in order to fix/modulate different vector. At this point can be concluded that the commutation numbers of interest will be starting from two (the minimum), up to four, that is just a step above the standard inverter case.

For all proposed methods, it is useful to introduce space vector approach as a useful insight. Due to the hexagon symmetry, the analysis can be restricted to one of the six big sectors (i.e., OAB in Fig. 3.26), similarly to the case of standard three-phase SVM algorithm. Using SVM principle, references $\bar{v}_H^*$ and $\bar{v}_L^*$ can be generated by selecting adjacent vectors $\bar{v}_{aH}^*$, $\bar{v}_{bH}^*$, $\bar{v}_{oH}^*$ and $\bar{v}_{aL}^*$, $\bar{v}_{bL}^*$, $\bar{v}_{oL}^*$, respectively. The application times of active vectors can be calculated by the expressions (3.18) applied to single voltage references:

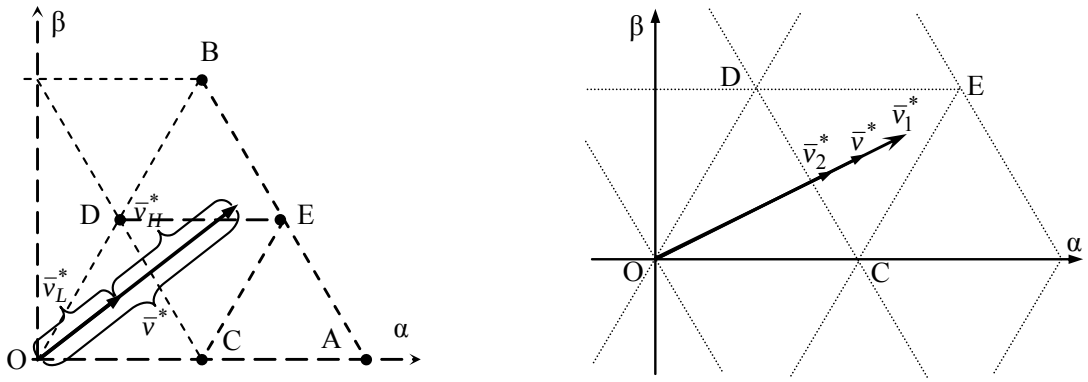
$$\bar{v}_H^* = v_{\alpha H}^* + jv_{\beta H}^*,\ \bar{v}_L^* = v_{\alpha L}^* + jv_{\beta L}^*. \tag{1}$$

The application times of null vectors are given by

$$t_{oH} = T_S - t_{aH} - t_{bH},\ \ t_{oL} = T_S - t_{aL} - t_{bL} \tag{2}$$

where t_{aH}, t_{bH}, t_{oH} and t_{aL}, t_{bL}, t_{oL} are application times for $\bar{v}_{aH}^*$, $\bar{v}_{bH}^*$, $\bar{v}_{oH}^*$, and $\bar{v}_{aL}^*$, $\bar{v}_{bL}^*$, $\bar{v}_{oL}^*$, respectively.

There are four distinctive cases, obtained by the division of the big triangle OAB in four identical equilateral triangles denoted OCD (inner), CDE (intermediate), ACE and BDE (outers), as shown in Fig. 1(a). The voltage reference vector $\bar{v}*$ lays in one of these triangles, leading to the following four relevant cases [1]. The switching configurations corresponding to the selected vectors cannot be applied in an arbitrary sequence if a proper multilevel voltage waveform is desired, i.e., the reference voltage $\bar{v}^*$ should be generated by using the nearest three vectors approach (NTV) [2]. Furthermore, it must be taken into account that the PWM generation unit of industrial DSPs allows up to two commutations within the switching period for each inverter leg, and even further, these commutations cannot be allocated in a arbitrary manner. The chosen



(a) (b)

Fig. 1. Detail of dual inverter voltage vector plot in the case $V_H = V_L = V_{dc}$ with voltage reference vector (a) four typical triangles, (b) switching period composition.

voltage strategy (Section 3.7) is optimum voltage utilization with power sharing capability, and it will be pursued for all methods in this chapter. The proposed methods have been presented from the simplest towards the most complex, with their performance regarding the fixed objectives in the same order.

4.1. Composition of switching periods

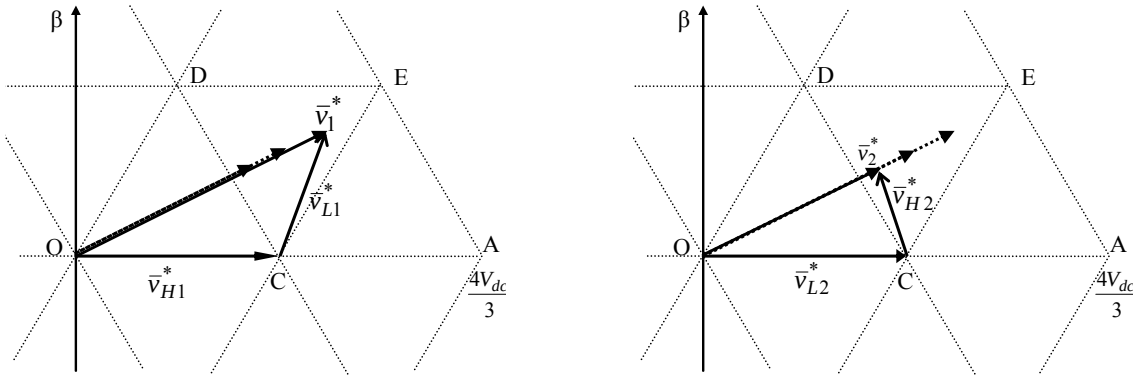
The composition of the switching periods provides a simple and effective method to obtain proper multilevel output. Simultaneously the method should work at switching frequency of each individual inverter equal to half of the output switching frequency (a common demand for all multilevel inverters), or to not more than one pulse within "big switching period" ($2T_S$) consisting of two consecutive switching periods (T_S). However, in section 3.5, it has been shown that developed modulation methods possess significant drawbacks such are increased switching frequency and multiple simultaneous commutations. Furthermore, the methods were not developed for the voltage strategy intended here.

As can be seen from Fig. 3.23 one of the reason for the increased number of the pulses was use of the continuous modulation with symmetrical zero vectors. Another particular problem for the method is "the transition between inverters": due to the duty cycles extended to 100% simultaneous commutations occur at the end of the each switching period when two inverters are swapping their roles. Only for the inner triangle (OCD) the use of zero vector redundancy provides sequence without double instantaneous commutation.

4.1.1. Basic composition of two switching periods

In order to generate the reference vector $\bar{v}*$ the method uses a sum of two collinear vectors denoted as $\bar{v}_1^*$ and $\bar{v}_2^*$ as shown in Fig. 2(a) produced in two consecutive periods T_S:

$$\bar{v}^* = (\bar{v}_1^* + \bar{v}_2^*)/2\,. \tag{3}$$



(a) (b)

Fig. 2. Composition of switching periods for intermediate triangle (a) the first switching period, (b) the second switching period.

Each of these two vectors is composed of one basic inverter vectors and other obtained by modulation, as shown in Fig. 2.

$$\bar{v}_1^* = \bar{v}_{H1}^* + \bar{v}_{L1}^*,\ \bar{v}_2^* = \bar{v}_{H2}^* + \bar{v}_{L2}^*, \tag{4}$$

where $\bar{v}_{H1}^*$ and $\bar{v}_{L2}^*$ are so-called "fixed vectors" from eight possible switching states and further can also be denoted as $\bar{v}_{H1}$ and $\bar{v}_{L2}$. Defining the ratio v_1/v_2 of their magnitudes provides the application of the power sharing capability with the corresponding coefficient (3.69):

$$\frac{|v_1|}{|v_2|} = \frac{1-k}{k}. \tag{5}$$

The analysis for given $\bar{v}*$ gives four typical cases for different triangles:

- Inner triangle OCD is made with

$$\bar{v}_{H1} = \bar{v}_{L2} = \bar{v}_O, \tag{6}$$

  therefore it will be one pulse within big switching period and no simultaneous commutations. As an illustration, a switching pattern is shown in Fig. 3(a).

- For outer triangle ACE

$$\bar{v}_{H1} = \bar{v}_{L2} = \bar{v}_C, \tag{7}$$

  but taking into account that corresponding switching states are

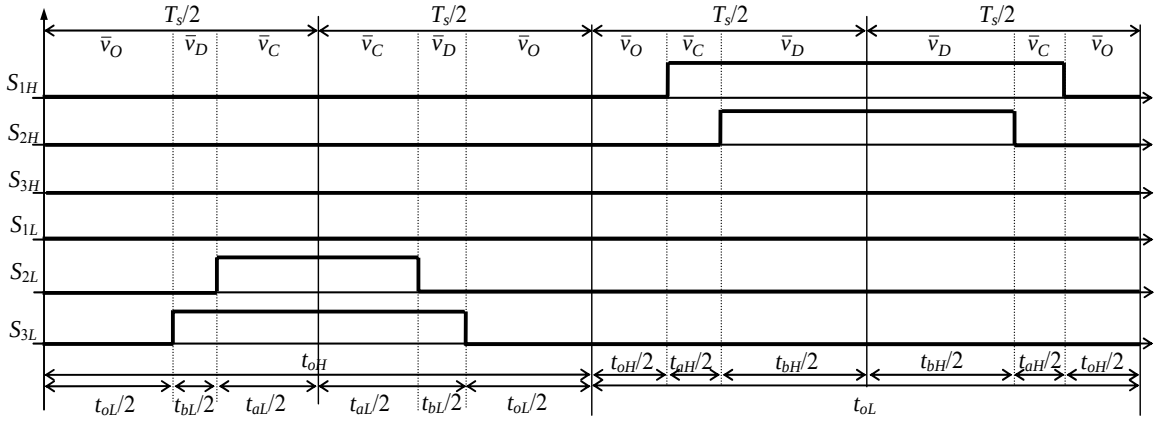


Fig. 3. Switching pattern for decomposition modulation inner triangle OCD.

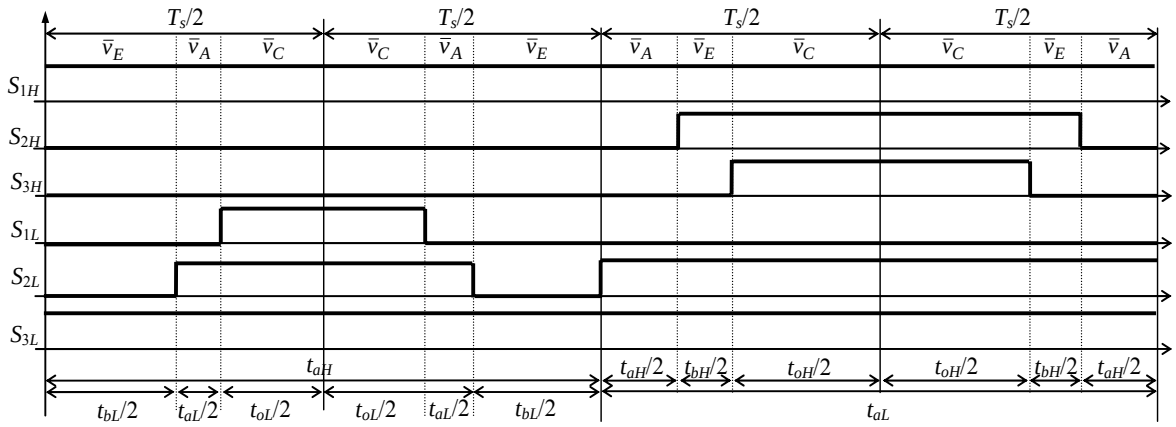


Fig. 4. Switching pattern for decomposition modulation outer triangle ACE.

$$\bar{v}_{H1} = (1,0,0)\,,\quad \bar{v}_{L2} = (0,1,1)\,. \tag{8}$$

To avoid two pulses in S_{1H} within big switching period it has to be fixed high, which is possible since it has the biggest duty cycle. However, the problem cannot be solved in this way for the inverter L where S_{2L}, S_{3L} are fixed high and only S_{3L} can be high during the whole period Fig. 4. A similar problem occurs for outer triangles BDE since needs to be

$$\bar{v}_{H1} = \bar{v}_{L2} = \bar{v}_D\,, \tag{9}$$

but taking into account that corresponding switching states are

$$\bar{v}_{H1} = (1,1,0)\,,\quad \bar{v}_{L2} = (0,0,1)\,. \tag{10}$$

leading to two pulses for S_{2H}.

- For intermediate triangle CDE can be chosen same (7) giving (8). Nevertheless, S_{1H} cannot be fixed high as for the outer triangle, and there will be both two pulses and simultaneous commutation of two inverters Fig. 5. It can be noted that each intermediate triangle there is the second possible choice (9) but it does not represent a better option.

It is more convenient to fix each of the six legs on and off for 1/6th of the output cycle, to avoid evident drawbacks from Fig. 4 and Fig. 5. This solution has already been mentioned in Section 3.5.

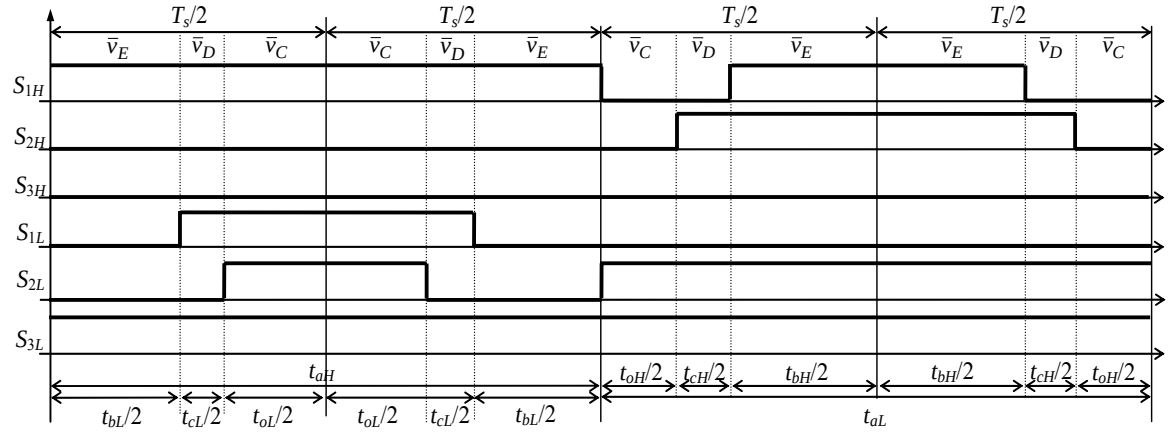


Fig. 5. Switching pattern for basic combination decomposition modulation intermediate triangles (a) CDE

4.1.2. Improved composition of two switching periods

The described drawback in the case of outer and intermediate triangles can be improved by introduction of additional modulation features. For the completeness, all cases inside hexagon AEDORT will be analyzed.

- For outer triangles ACE and ACT S_{1H} has to be fixed high, which is possible as the biggest duty cycle. On the other side, S_{1L} has to be fixed low as a lowest duty cycle. An opposite slope for the inverter L provides only one pulse within big switching period, as shown in Fig. 6. Similar can be shown for outer triangle BDE (hexagon OCEBHG), where S_{3H} has to be fixed low, which is possible since it is the lowest duty cycle. Analogously S_{3L} has to be fixed high as the biggest duty cycle.
- For intermediate triangle CDE a degree of freedom (choice between $\bar{v}_C$ and $\bar{v}_D$) can be used for the improved combination of the two periods T_s. instead of basic combination shown in Fig. 7(a) will be used improved combination Fig. 7(b) exploiting the degree of freedom and fixing

$$\bar{v}_{L2} = \bar{v}_D, \tag{11}$$

Then S_{1H} can be fixed to high state, and simultaneously solve the problem for inverter L where S_{3L} can be fixed high, see Fig. 8. However, the resulting average vectors differ for two inverters in this way, as shown in Fig. 7(b). Therefore, in the adjacent big cycle two inverters will "swap" roles, as also depicted in Fig. 9.

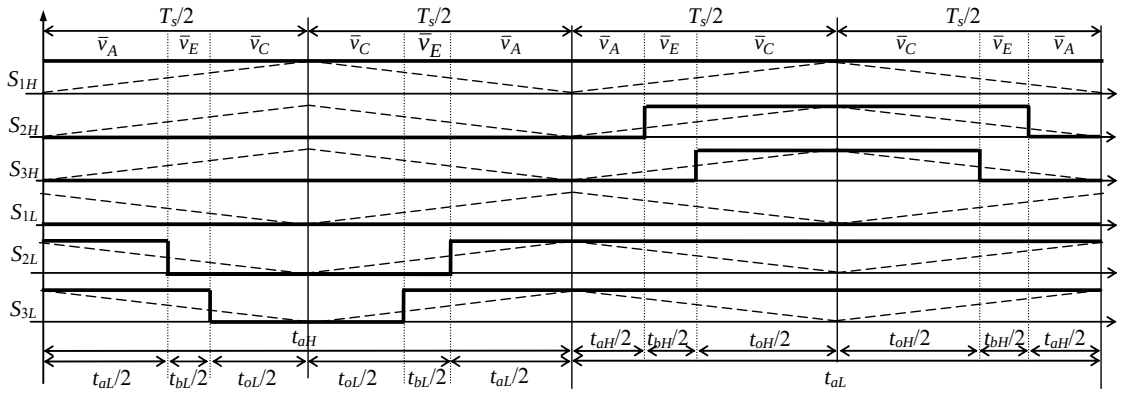


Fig. 6. The switching pattern decomposition modulation improved for outer triangle ACE.

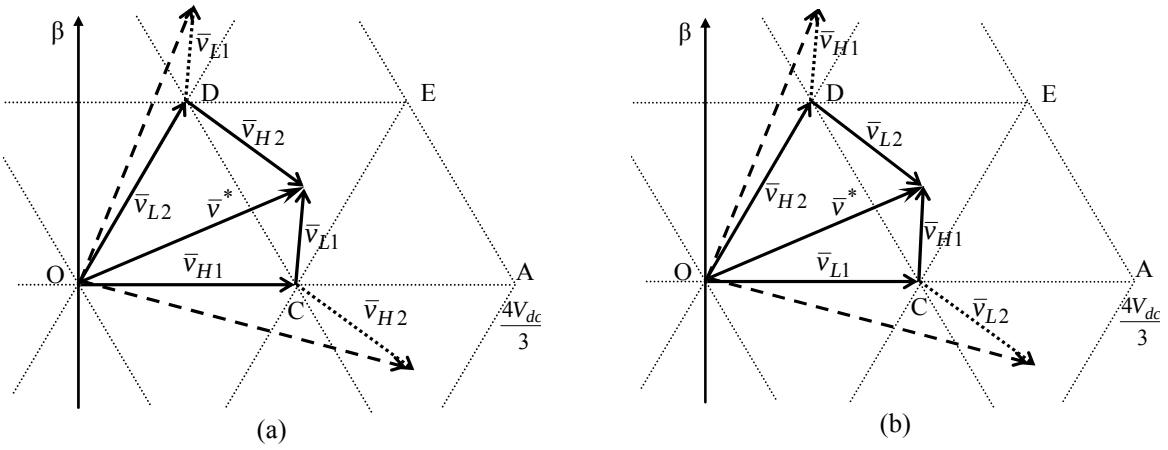


Fig. 7. Improved decomposition for intermediate triangle CDE: (a) first, (b) second big switching period.

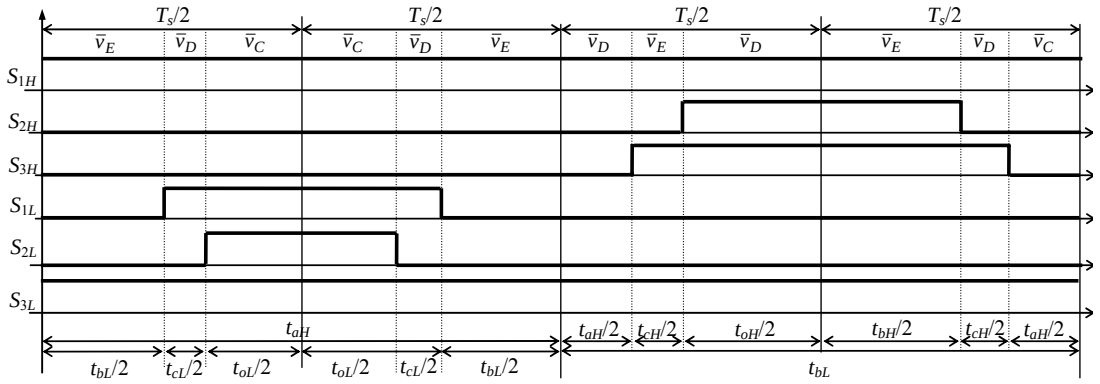


Fig. 8. Improved decomposition modulation for intermediate triangle CDE first switching pattern.

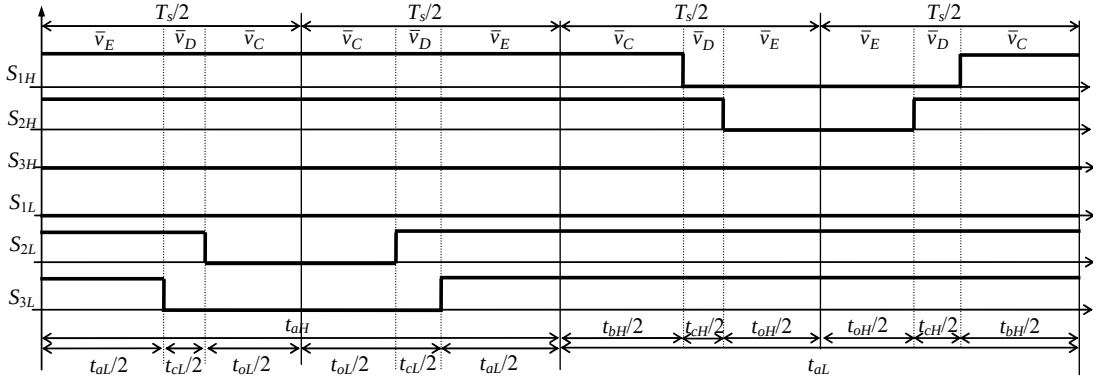


Fig. 9. Improved decomposition modulation for intermediate triangle CDE: second switching pattern.

$$\bar{v}_{H1} = \bar{v}_D , \tag{12}$$

As can be seen from the diagrams the principle of symmetry was fulfilled, having each leg fixed on and off for 1/6th of the output cycle, as in single inverter discontinuous modulation. E.g. for triangle CDE is fixed S_{1H} high and S_{3H} low, as can be seen from Fig. 8 and Fig. 9. A drawback of the proposed method is that close to the borders of the triangles two references $\bar{v}_1^*$ and $\bar{v}_2^*$ will produce different voltage levels (e.g. when $\bar{v}_1^*$ is in ACE and $\bar{v}_2^*$ in CDE), that will lead to a "hybrid" voltage vaveform.

4.1.3. Asymmetrical carrier-based composition method

A simple solution to eliminate two pulses within big period is to use asymmetrical modulation for intermediate triangle CDE. Again, the switching patterns are based on the triangular subdivision. For this method can be applied both continuous and discontinuous modulation, as shown in Fig. 10(a) and (b), respectively. Implementation of the asymmetrical modulation can be achieved by either standard triangle carriers. The biggest drawback of the method is multiple instantaneous commutations at the instant when two inverters exchange their roles, as already stated. Again fixing roles for 1/6th of the period would lessen the consequences.

An improved performance requires independent but synchronous carriers of particular waveform, shown in Fig. 11. It can be noted that for the modulating inverter one carrier signal has to be in counter-phase in order to provide proper modulation. Indeed, if the first carrier (for

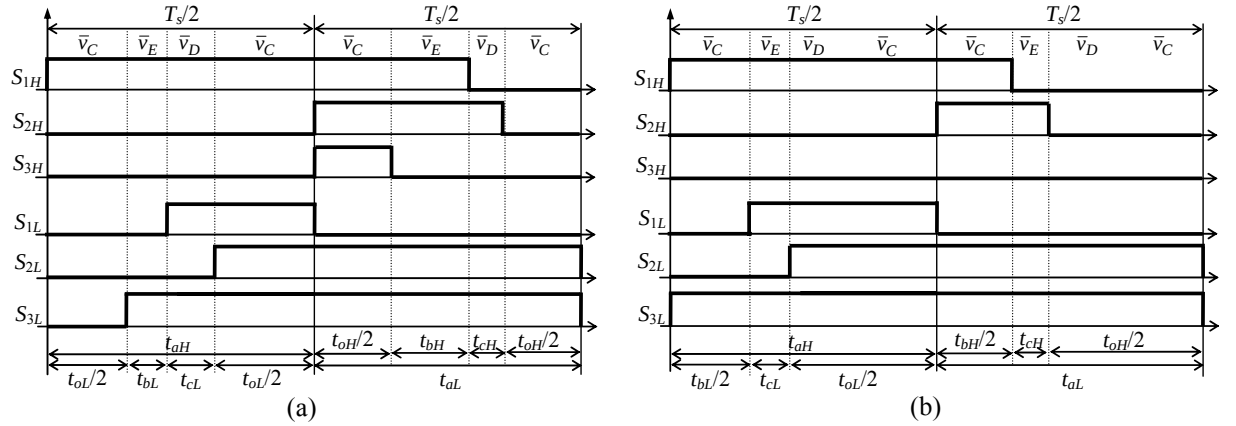


Fig. 10. Decomposition switching pattern using for intermediate triangle CDE (a) continuous, (b) discontinuous asymmetrical modulation.

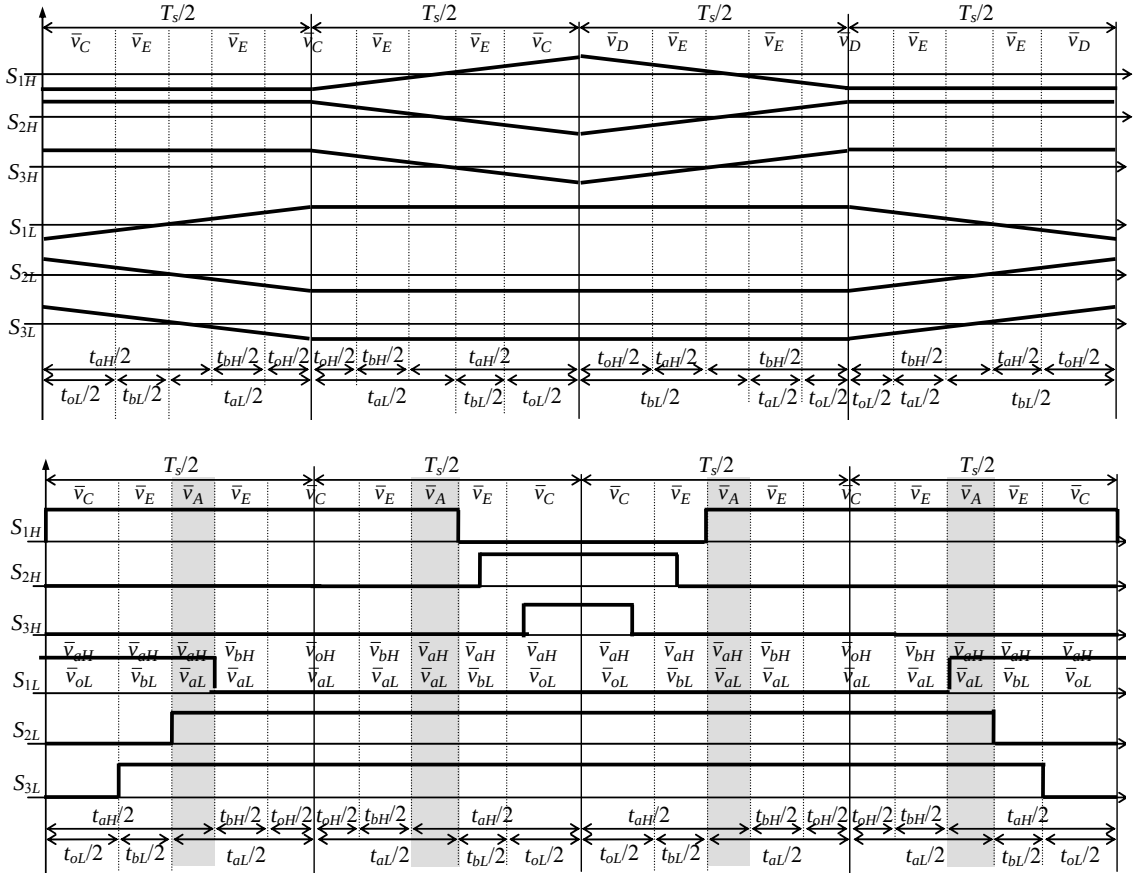


Fig. 11. Special carriers for the composition in intermediate triangle CDE (a) continuous, (b) discontinuous asymmetrical modulation.

S_{1H}) would be in the phase with the other two he overage voltage value would be the same but unwanted pair instead of (v_o, v_o) there is combination (v_a, -v_a) with the same duration [3].

4.2. Discontinuous carrier-based PWM

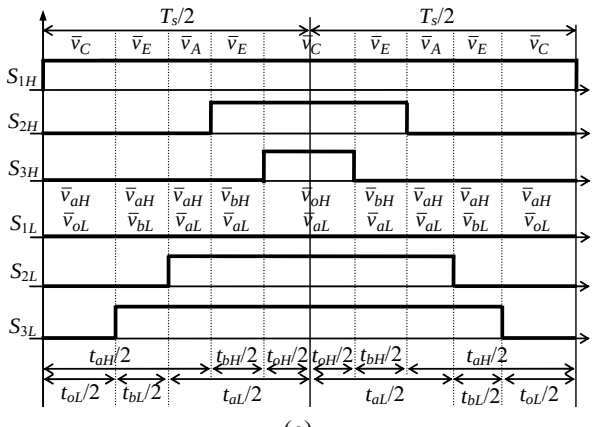
4.2.1. Discontinuous modulation

A better solution would be application of discontinuous modulation for each inverter since it does not contain both zero vectors within the switching period. In particular, the proper application of discontinuous 60º modulation with clamp at voltage peaks to the two inverters eliminates completely big vectors for the inner triangle. Modulating signals expressed in relative units are given by:

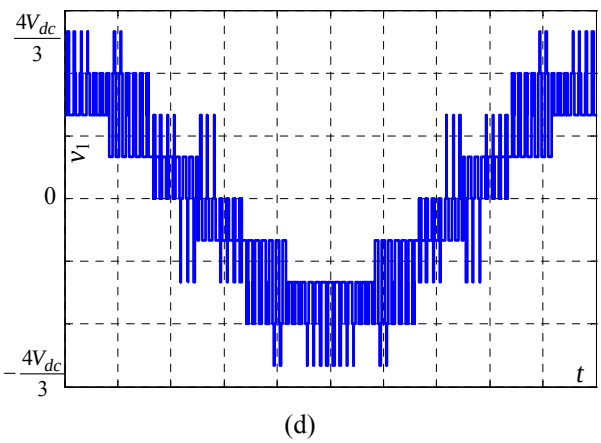
$$(v_{1H}^*, v_{2H}^*, v_{3H}^*) = (1, 1 - m\cos(\theta + \frac{\pi}{6}), 1 - m\cos(\theta - \frac{\pi}{6}))$$
$$(v_{1L}^*, v_{2L}^*, v_{3L}^*) = (0, m\cos(\theta + \frac{\pi}{6}), m\cos(\theta - \frac{\pi}{6})) \quad (13)$$

where signals for the L-inverter are obtained from H-inverter by subtraction from the maximum value to produce opposite output voltage [4]. It can be noted that division to sectors A and B (Fig. 3.26) illustrates the discontinuous modulation (one leg is fixed during each A/B sector). In order to balance on- and off-time of the switches division in half-sectors provides possibility to have both always-on and always-off leg in each sector. Each inverter has six switches with two states each gives exact number of twelve different "half-sectors". Example of the switching patterns in A-half is given in Fig. 12(a), where can be seen that the starting vector corresponds to the name of the half-sector. The explanation of the improper multilevel waveform inside intermediate triangle that can be seen from Fig. 12(b), requires only a brief analysis that will be provided in the following section.

Corresponding to the described modulation, Fig. 13(a) shows experimental voltage waveform for the carrier based discontinuous modulation. The upper half of the figure shows a period (20 ms) of the output voltage corresponding to Fig. 12(b). Additionally, all six PWM signals A0-A5 correspond to PWM signals for legs 1H-3H and 1L-3L respectively have been captured using 8-channel digital probe. The zoomed switching period on the lower half shows switching pattern corresponding to Fig. 12(a) and output voltage within period (position in outer triangle ACE). A



(c)



(d)

Fig. 12. Discontinuous modulation (a) pattern in outer triangle ACE (b) output voltage (m = 0.75, f_s = 2 kHz).

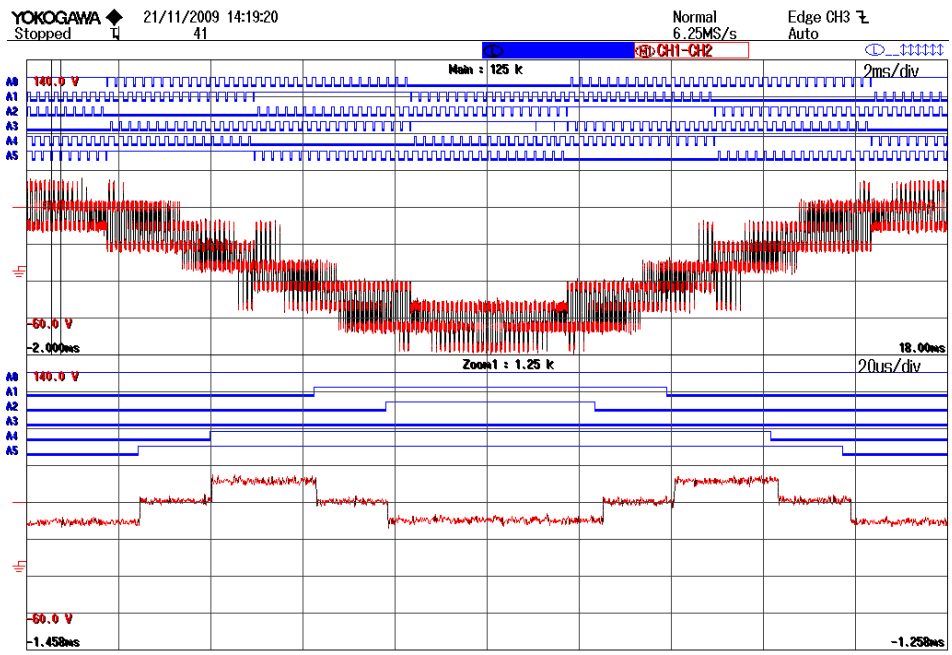


Fig. 13. PWM pattern and voltage output for discontinuous modulation (m = 0.75, f_s = 5 kHz) with zoomed detail in the outer triangle ACE.

reduced switching frequency (5 kHz) has been chosen for the sake of readability. Experimental results show excellent correspondence to the simulation result.

The method is very simple for the implementation and gives power sharing capability and relatively good output waveform, when compared to the simplicity. It is possible to avoid the wrong voltage levels by the inclusion of a much more complex algorithm based on the space vector approach, given in details in the next section.

4.2.2. Asymmetrical slope carriers

The standard term "triangular carrier": usually is referenced to a carrier with two equal slopes. It possesses two important advantages:

- Symmetrical pulses cancel harmonics
- Simpler implementation (up and down values equal)

The constraint for this carrier is limitation to the pulse position, constraining the number of commutation to one in each half of period. For some modulations, asymmetrical triangular carrier is needed to achieve non-centered pulse pattern.

In the case of the dual inverter the space modulation becomes complex for the intermediate triangle case [1]. For example, a switching sequence proposed for two triangular areas in [5] are shown in Fig. 14. These patterns cannot be implemented with standard symmetrical carrier, which provides a maximum of one commutation can take place in each half of the switching period.

The Fig. 15(a) demonstrates synchronized of the two carrier signals: standard and asymmetrical. Carrier signal C_{1H} has peak at a quarter of the period, and compare is set to PRD in that part. EVB has symmetrical 50 % duty pulses. It can be seen that two waveforms are synchronized (pulse leading edge match). The Fig. 15(b) shows that pulse can be produced just

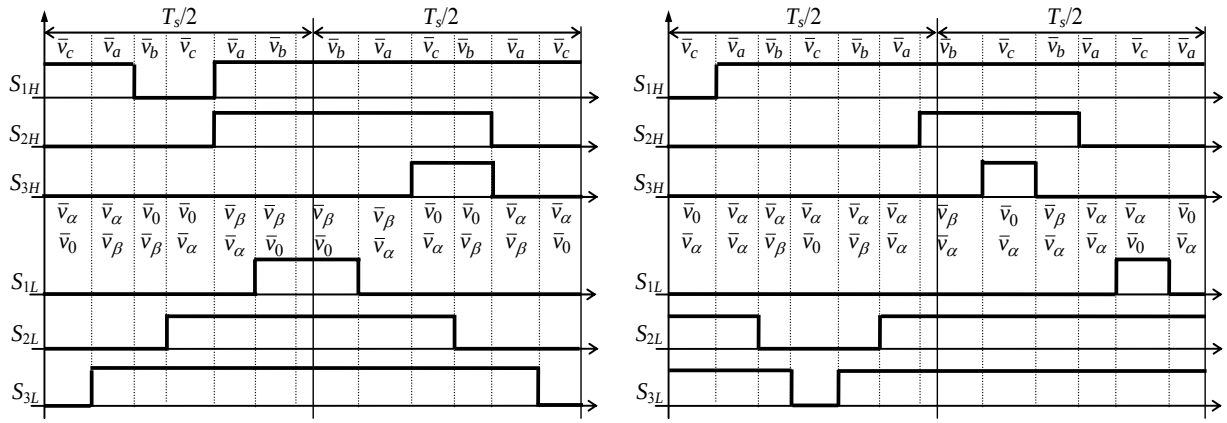


Fig. 14. Proposed switching sequence that needs asymmetrically sloped carrier (a) intermediate triangle CDE, (b)

in the first half of the switching period. It is done by introducing period lower than the "symmetric" value, then (immediately after "peak") changing both slope and counter in order to have equal T_s (e.g. 50 μs) in total.

Both changes take place immediately, on the fly, so there are small imprecision's. For more precise implementation, it might be manually calibration to determine, better values (maybe not exact because slope takes different values). Period can be changed only when counter reaches top value, so it is rewritten in the second part. The resulting frequency of the carrier is unfortunately approximate because the counter and slope (even if changed for a proper value) are not exactly equal to calculated due to of the discrete numbers (e.g. 5625/4 = 1406.25). Due to this reason, two carriers would run asynchronously so they need to be "reset" in the beginning of the each switching period. Although the method possess error of the digitalization due to digital counter registers the steps in today's processors are very small on the time scale, for example in F2812 the digitalization error is on the order of 0.2 μs.

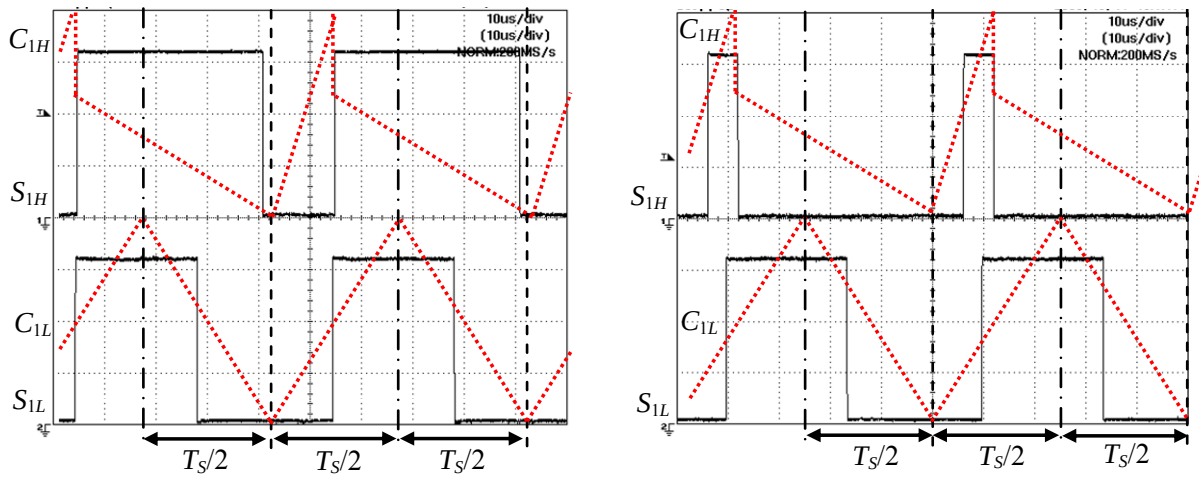


Fig. 15. Experimental results (a) synchronization check with the standard carrier, (b) pulse in the first half only.

4.3. Space vector pulse-width modulation

4.3.1. Determination of the switching sequence

In order to determine the switching sequence, four representative triangles will be examined OCD (inner), CDE (intermediate), ACE and BDE (outers), as shown in Fig. 16(a). Additionally the hexagon is divided in A-B subsectors determined by comparison of corresponding application times of the same inverter, e.g. inverter H:

$$t_{aH} \geq t_{bH}, \tag{14}$$

The voltage reference vector $\bar{v}*$ lays in one of these triangles, leading to the following four relevant cases.

A. Inner triangle OCD

For the inner triangle the NTV are $\bar{v}_O$, $\bar{v}_C$, and $\bar{v}_D$ which can be obtained by the following combinations of voltage vectors selected for the two inverters:

- ($\bar{v}_{oH}$, $\bar{v}_{oL}$), forming $\bar{v}_O$,
- ($\bar{v}_{aH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{aL}$), forming $\bar{v}_C$,
- ($\bar{v}_{bH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{bL}$), forming $\bar{v}_D$.

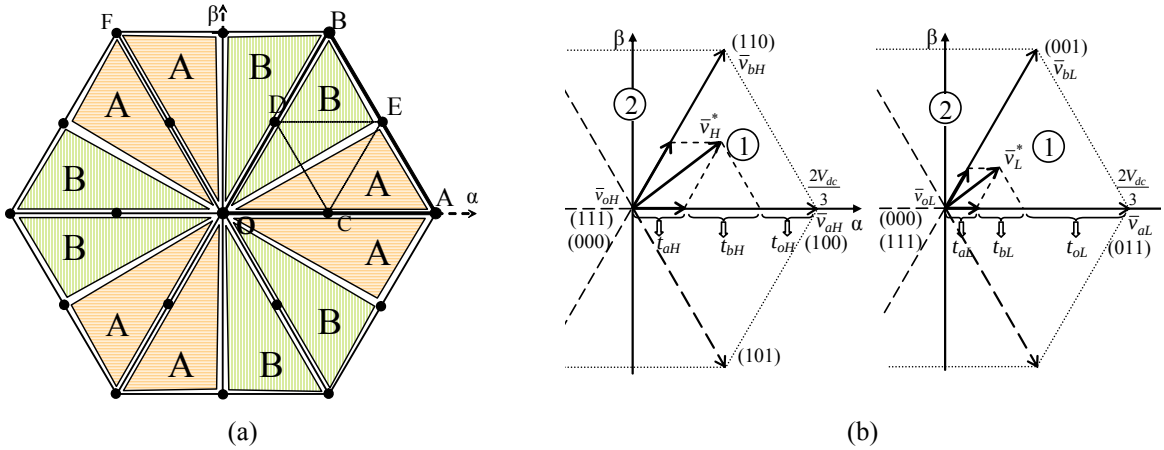
By using these combinations, since $\bar{v}^* = \bar{v}_H^* + \bar{v}_L^*$ is inside the inner triangle, for any value of $\bar{v}_H^*$ and $\bar{v}_L^*$, Fig. 16(b), the total application time of active vectors is

$$t_{aH} + t_{bH} + t_{aL} + t_{bL} \leq T_s \tag{15}$$

By combining (15) with (2) yields

$$t_{oH} + t_{oL} \geq T_S \tag{16}$$

Note that (16) provides a criterion for the identification of the inner triangle OCD. The voltage vector combinations can be arranged within the switching period to obtain a switching sequence suitable for the implementation in PWM generation unit of industrial DSPs, as represented in Fig. 17(a). In the figure is emphasized (grey) the overlap between the two null vectors ($\bar{v}_{oH}$ and



(a) (b)

Fig. 16. (a) Dual inverter voltage vector plot in the case $V_H = V_L = V_{dc}$. (b) Space vector composition of $\bar{v}_H^*$ and $\bar{v}_L^*$ by using the two adjacent active vectors for each inverter.

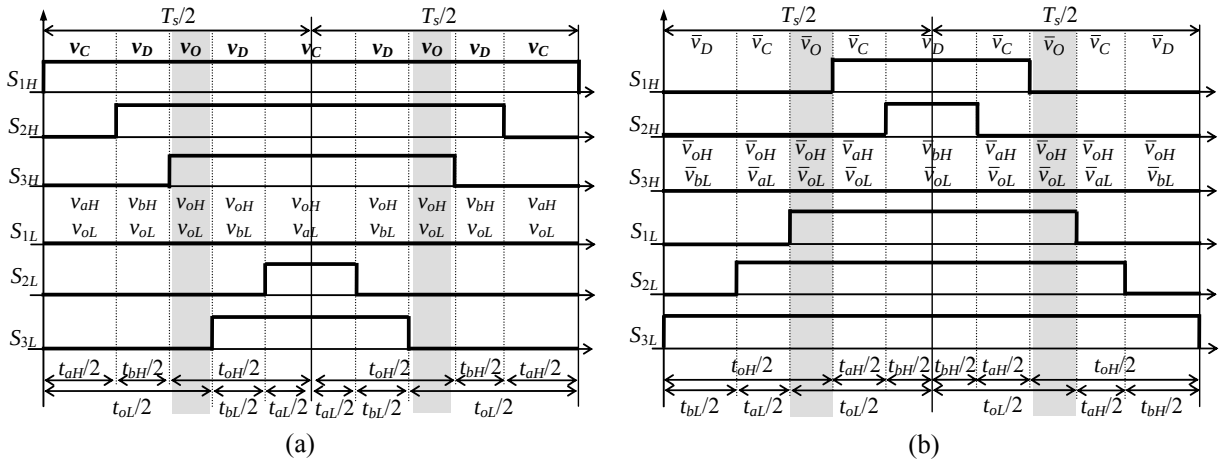


Fig. 17. Proposed switching sequences for inner triangle OCD case (a) A-half, (b) B-half.

$\bar{v}_{oL}$), provided by (16), which secures the generation of $\bar{v}^*$ only by vectors $\bar{v}_O$, $\bar{v}_C$, and $\bar{v}_D$. For the B-half the order of the duty cycles remains the same (e.g. $T_{aH} > T_{bH} > T_{cH}$), they just increase/decrease.

The proposed switching sequence belongs to symmetrical and discontinuous modulation, minimizing the number of commutations. A continuous modulation can be easily obtained by introducing the null vector $\bar{v}_O$ in the middle and at the ends of the switching period.

B. Outer triangle ACE

For the first outer triangle the NTV are $\bar{v}_A$, $\bar{v}_C$, and $\bar{v}_E$, which can be composed by the combinations:

- ($\bar{v}_{aH}$, $\bar{v}_{aL}$), forming $\bar{v}_A$,
- ($\bar{v}_{aH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{aL}$), forming $\bar{v}_C$,
- ($\bar{v}_{aH}$, $\bar{v}_{bL}$) and ($\bar{v}_{bH}$, $\bar{v}_{aL}$), forming $\bar{v}_E$.

Since $\bar{v}^*$ lies inside the triangle ACE, its component along $\bar{v}_{aH}$ is bigger than the amplitude of $\bar{v}_{aH}$ (see Fig. 16). Similar to the previous case, for application times this consideration leads to

$$t_{aH} + t_{aL} \geq T_S \tag{17}$$

Equation (17) provides a criterion for the identification of the outer triangle ACE. Also in this case, the voltage vector combinations can be arranged within the switching period to obtain a switching sequence suitable for the implementation in PWM generation unit of industrial DSPs, as represented in Fig. 18(a). In the figure is emphasized the overlap between the two active vectors ($\bar{v}_{aH}$ and $\bar{v}_{aL}$), provided by (17), which allows the generation of $\bar{v}^*$ only by vectors $\bar{v}_A$, $\bar{v}_C$ and $\bar{v}_E$. As in the previous case of the inner triangle, the proposed sequence leads to symmetrical and discontinuous modulation, with the difference that is not possible anymore to introduce continuous modulation.

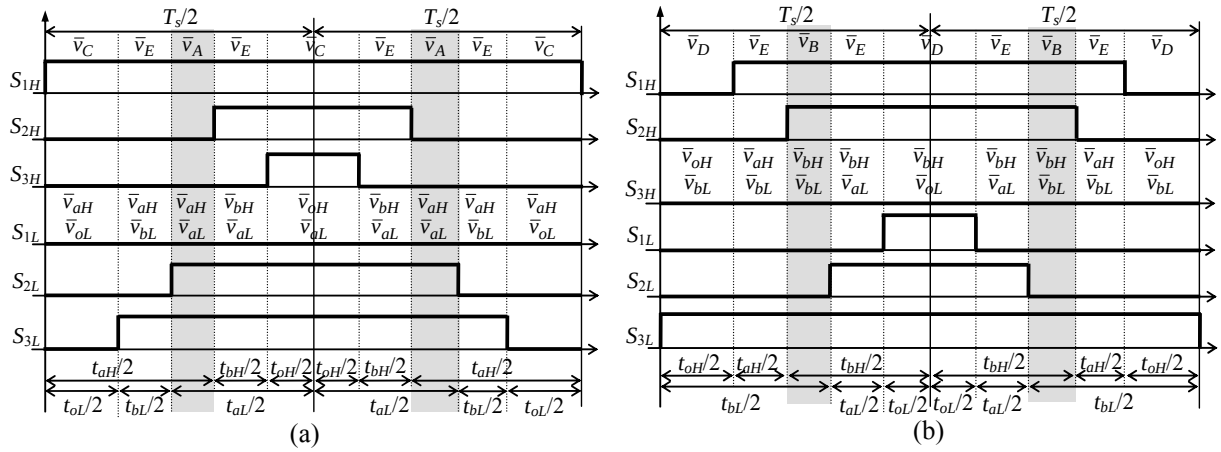


Fig. 18. Proposed switching sequences for the outer triangles (a) ACE, (b) BDE.

C. Triangle BDE

For the second outer triangle the NTV are $\bar{v}_B$, $\bar{v}_D$, and $\bar{v}_E$. Due to the symmetry of outer triangles ACE and BDE, this case can be treated as the previous one, involving vectors $\bar{v}_{bH}$ and $\bar{v}_{bL}$ instead of $\bar{v}_{aH}$ and $\bar{v}_{aL}$, respectively, leading to

$$t_{bH} + t_{bL} \geq T_S \tag{18}$$

Also in this case, (18) provides a criterion for the identification of the outer triangle BDE. The proposed switching sequence is shown in Fig. 18(b), again symmetrical and discontinuous as in the previous case.

D. Triangle CDE

For the intermediate triangle the NTV are $\bar{v}_C$, $\bar{v}_D$, and $\bar{v}_E$, which can be generated by the combinations:

- ($\bar{v}_{aH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{aL}$), forming $\bar{v}_C$,
- ($\bar{v}_{bH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{bL}$), forming $\bar{v}_D$,
- ($\bar{v}_{aH}$, $\bar{v}_{bL}$) and ($\bar{v}_{bH}$, $\bar{v}_{aL}$), forming $\bar{v}_E$.

The following three conditions define the triangle CDE:

$$t_{oH} + t_{oL} \leq T_S \quad \text{(outside OCD)}, \tag{19}$$

$$t_{aH} + t_{aL} \leq T_S \quad \text{(outside ACE)}, \tag{20}$$

$$t_{bH} + t_{bL} \leq T_S \quad \text{(outside BDE)}, \tag{21}$$

The presence of three simultaneous conditions (19)-(21) makes the case of the intermediate triangle CDE the most complex among the four considered cases.

The proposed switching sequence is shown in Fig. 19(a). The parameter t_x (denoted with grey) stands for a degree of freedom which determines the relative position of the switching sequence of one inverter with respect to the other (i.e., one of the sequences can be translated by the time interval t_x). A similar degree of freedom also exists in the previous three cases (grey intervals in Fig. 17 and Fig. 18). Since application times are already determined, the remaining step is to choose the value for interval t_x, thus completely determining the requirements for the DSP

implementation. In particular, for the existence of all the vector combinations shown in Fig. 19(a), t_x has to satisfy the following constraints (from beginning towards the end of the period):

- $(\bar{v}_{aH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_E$:

$$t_x \leq t_{aH}, \tag{22}$$

- $(\bar{v}_{oH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_D$:

$$t_x \geq t_{aH} - t_{bL}, \tag{23}$$

- $(\bar{v}_{oH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_C$:

$$t_x \leq T_s - t_{bH} - t_{bL}, \tag{24}$$

- $(\bar{v}_{bH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_E$:

$$t_x \geq t_{oL} - t_{bH}, \tag{25}$$

- $(\bar{v}_{bH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_D$:

$$t_x \leq t_{oL}, \tag{26}$$

- $(\bar{v}_{aH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_C$:

$$t_x \geq 0, \tag{27}$$

A detailed derivation of inequalities (22)-(27) is presented in the Appendix, together with the proof that a solution always exists.

Another degree of freedom is expressed by value for interval t_y, which ultimately establishing the requirements for the DSP implementation. Since using symmetric common carrier for each three legs of DSP PWM unit there can be not more than one commutation in each half-period it is important to frame the switching pattern within switching period defined by the unit. This position is defined by additional degree of freedom expressed by value for interval t_y, that has to satisfy two simple conditions:

- $(\bar{v}_{aH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_C$:

$$0 \leq t_y \leq t_x, \tag{28}$$

- $(\bar{v}_{oH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_C$:

$$t_{bH} + t_x - T_s/2 \leq t_y \leq T_s/2 - t_{bL}, \tag{29}$$

While (28) is obvious from Fig. 19(a), a detailed derivation of (29) is presented in the Appendix, together with the proof that a solution always exists. As a value for t_y can be chosen:

$$t_y = (\min\{T_s/2 - t_{bL}, t_x\} + \max\{t_{bH} + t_x - T_s/2,\ 0\})/2, \tag{30}$$

Similarly, for the B-half the solution is analogously developed analyzing the figure Fig. 19(b):

$$t_x \leq t_{oH}, \tag{31}$$

$$t_x \geq t_{oH} - t_{aL}, \tag{32}$$

$$t_x \leq T_s - t_{aH} - t_{aL}, \tag{33}$$

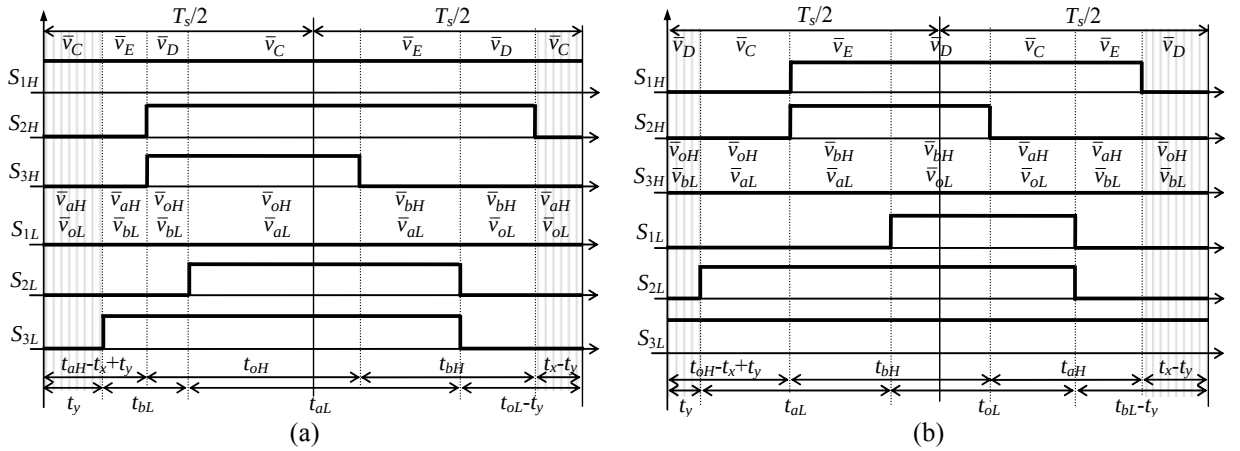


Fig. 19. Switching pattern for intermediate triangle CDE with instantaneous commutations (a) A-half, (b) B-half.

$$t_x \geq t_{bL} - t_{aH}, \tag{34}$$

$$t_x \leq t_{bL}, \tag{35}$$

$$t_x \geq 0, \tag{36}$$

with a possible solution:

$$t_x = (\min\{t_{bL}, T_s - t_{aL} - t_{aH}, t_{oH}\} + \max\{t_{oH} - t_{aL}, t_{bL} - t_{aH}, 0\})/2, \tag{37}$$

Due to the symmetry all regarding t_y can be analogously repeated for the B-half with pattern shown in Fig. 19(b) provided by swapping pairs $t_{bH} \leftrightarrow t_{aH}$ and $t_{bL} \leftrightarrow t_{aL}$ (Appendix). The solution can be:

$$t_y = (\min\{T_s/2 - t_{aL}, t_x\} + \max\{t_{aH} + t_x - T_s/2, 0\})/2, \tag{38}$$

The proposed switching sequence is discontinuous, as in previous cases. However in contrast to previous patterns contain a simultaneous commutation of two legs for both inverters H and L. It is possible to overcome this drawback by introducing the additional vectors $\bar{v}_{cH}$, $\bar{v}_{cL}$ and/or $\bar{v}_{dH}$, $\bar{v}_{dL}$ (depicted in Fig. 6) in the space vector decomposition (Fig. 4), leading to a more complex modulation algorithm. Despite of the asymmetric distribution of pulses within the switching period, the proposed modulation can be implemented in the PWM generation unit of an industrial DSP, as proved by the experimental tests.

4.3.2. Elimination of double instantaneous commutation

The drawback of the proposed sequence is a simultaneous commutation of two legs for both inverters H and L. It is possible to overcome this disadvantage by introducing the additional vector pairs ($\bar{v}_{cH}$, $\bar{v}_{cL}$) or ($\bar{v}_{dH}$, $\bar{v}_{dL}$) (depicted in Fig. 21) in the space vector decomposition previously shown in Fig. 16(b). Pair ($\bar{v}_{cH}$, $\bar{v}_{cL}$) is applied for A-half and will be examined in details, whereas for B-half ($\bar{v}_{dH}$, $\bar{v}_{dL}$) pair the analysis can be repeated in a similar. The application time t_c of the new vector is introduced at the expense of t_{oH} and t_{oL}, and it presents a degree of freedom. It adds two new vector combinations ($\bar{v}_{cH}$, $\bar{v}_{bL}$) and ($\bar{v}_{bH}$, $\bar{v}_{cL}$) equivalent to already present ($\bar{v}_{aH}$, $\bar{v}_{oL}$) and ($\bar{v}_{oH}$, $\bar{v}_{aL}$), as can be seen in Fig. 21. From equation:

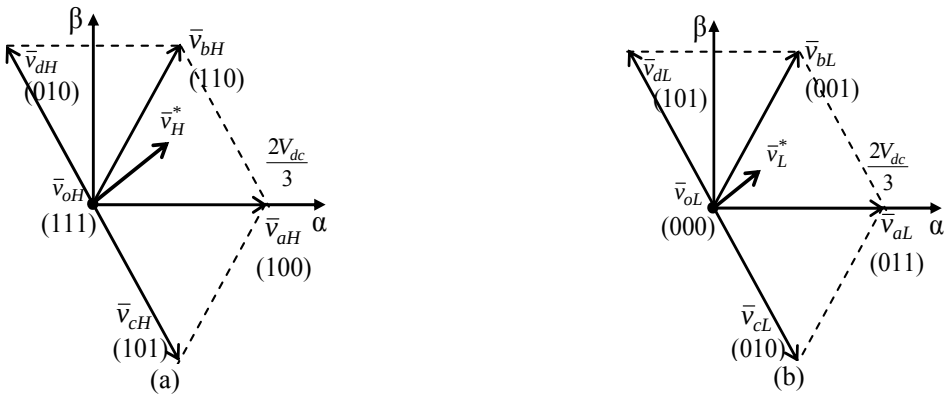


Fig. 20 Introduced vectors $\bar{v}_{cH}$ and $\bar{v}_{cL}$ (a) $\bar{v}_{cH}$ and $\bar{v}_{cL}$ (b) $\bar{v}_{dH}$ and $\bar{v}_{dL}$.

$$\bar{v}_{cH} = \bar{v}_{aH} - \bar{v}_{bH}, \quad \bar{v}_{cL} = \bar{v}_{aL} - \bar{v}_{bL}, \tag{39}$$

yields that t_{bH} and t_{bL} should be increased for an amount of t_c, whereas t_{aH} and t_{aL}, should be decreased for the same time interval:

$$\begin{cases} t'_{bH} = t_{bH} + t_c, \; t'_{bL} = t_{bL} + t_c \\ t'_{aH} = t_{aH} - t_c, \; t'_{aL} = t_{aL} - t_c \\ t'_{oH} = t_{oH} - t_c, \; t'_{oL} = t_{oL} - t_c \end{cases}, \tag{40}$$

where the corresponding application times of the vectors $\bar{v}_{aH}$, $\bar{v}_{bH}$, $\bar{v}_{oH}$ and $\bar{v}_{aL}$, $\bar{v}_{bL}$, $\bar{v}_{oL}$ are now denoted as t'_{aH}, t'_{bH}, t'_{oH}, and t'_{aL}, t'_{bL}, t'_{oL}, respectively. From (40) arises:

$$t_c \le \min\{t_{aH}, t_{aL}, t_{oH}, t_{oL}\}, \tag{41}$$

The proposed asymmetrical switching sequence is shown in Fig. 21(a) with interval t_c chosen to satisfy two critical conditions:

- providing $\bar{v}_C$ at the beginning of the period:

$$0 \le t_c \le t_y, \tag{42}$$

- providing $\bar{v}_C$ in the middle of the period:

$$t_c \le T_s/2 - t_{bH} - t_x + t_y, \tag{43}$$

The proposed asymmetrical switching sequence is shown in Fig. 21(a) with interval t_c chosen to

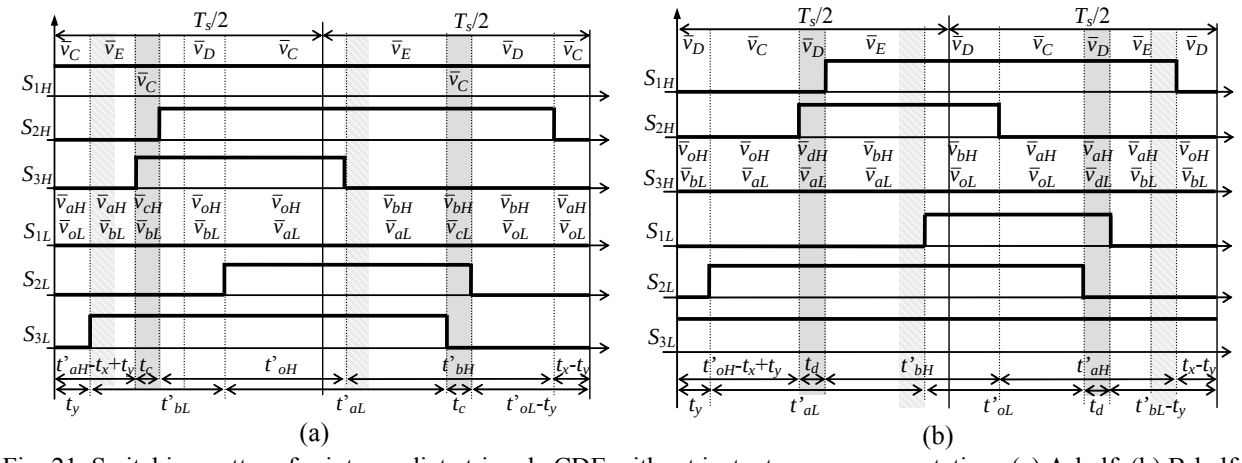


Fig. 21. Switching pattern for intermediate triangle CDE without instantaneous commutations (a) A-half, (b) B-half.

satisfy the conditions:

$$t_c \le T_s/2 - t_{bH} - t_x + t_y, \tag{44}$$

A proposed solution is:

$$t_c = \min\{T_s/2 - t_{bH} - t_x + t_y,\ t_y, t_{aH}, t_{aL}, t_{oH}, t_{oL}\}/2, \tag{45}$$

Due to the symmetry all can be analogously proven for the second case and parameter t_d,

$$t_d \le \min\{T_s/2 - t_{aL} - t_y, t_x - t_y, t_{bH}, t_{bL}, t_{oH}, t_{oL}\}, \tag{46}$$

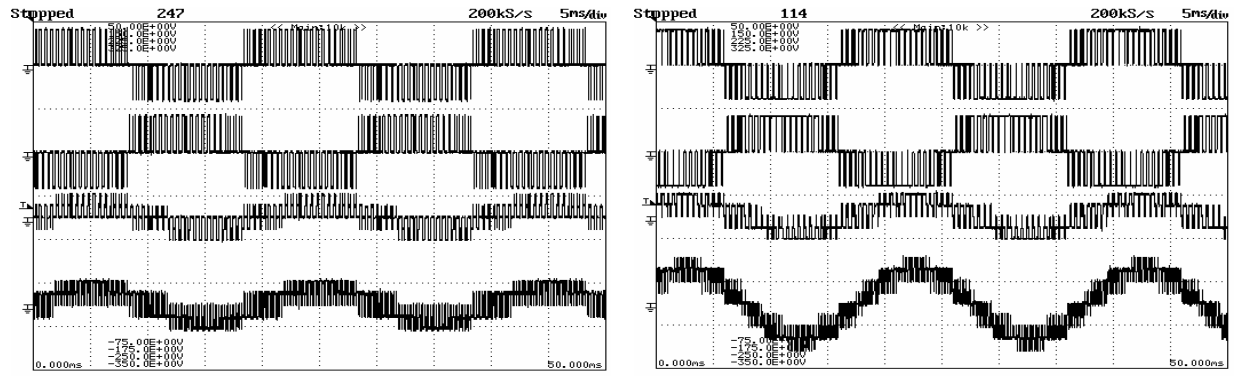
with switching sequence shown in Fig. 21(b).

The proposed switching sequence is discontinuous, as in previous cases, but it does not contain a simultaneous commutation of two legs as in previous case. Despite of the asymmetric distribution of pulses within the switching period, the proposed modulation can be implemented on the PWM generation unit of a standard DSP, as proved by the experimental tests.

4.3.3. Implementation

The voltage waveforms generated by the dual inverter configuration are shown to prove the effectiveness of the proposed SVM algorithm when implemented on a real DSP board. The first situation to be tested is when the power-sharing coefficient is set to k = 0.5 (balanced modulation). In Fig. 22 are depicted the individual inverter voltages (for both inverters "H" and "L"), line-to-line voltages and the total output voltage of the converter in two different cases: (a) reference output voltage inside the inner hexagon, m = 0.45, (b) reference output voltage between the inner and the outer hexagons, m = 0.9 V. A reduced switching frequency has been chosen for the sake of readability (2 kHz instead of 20 kHz). It shows that the output voltage (v_{H1L1}) has proper number of levels (five and nine, respectively) and the proper waveform, whereas line-to-line voltages (v_{H12}, v_{L12}) and the artificial line-to-neutral voltage (v_{H1}) are over three and five levels, respectively.

The second experiment has been done for modulation index m = 0.75 and for both symmetrical (k = 0.5) and asymmetrical (k = 0.65) inverter's power sharing, with results presented in Fig. 23. Each PWM waveform is shown together with its fundamental component obtained by the low-pass filter. Figures 23(a) and 23(c) show individual phase voltages for each inverter. It can be noticed that voltages are in phase opposition in order to achieve maximum



(a) (b)

Fig. 22 Space vector modulation waveforms f = 50 Hz, 50 V/div, from top to bottom: line-to-line voltages (v_{H12}, v_{L12}), artificial line-to-neutral voltage (v_{H1}), and converter output voltage (v_1); (a) m =0.45, (b) m = 0.9.

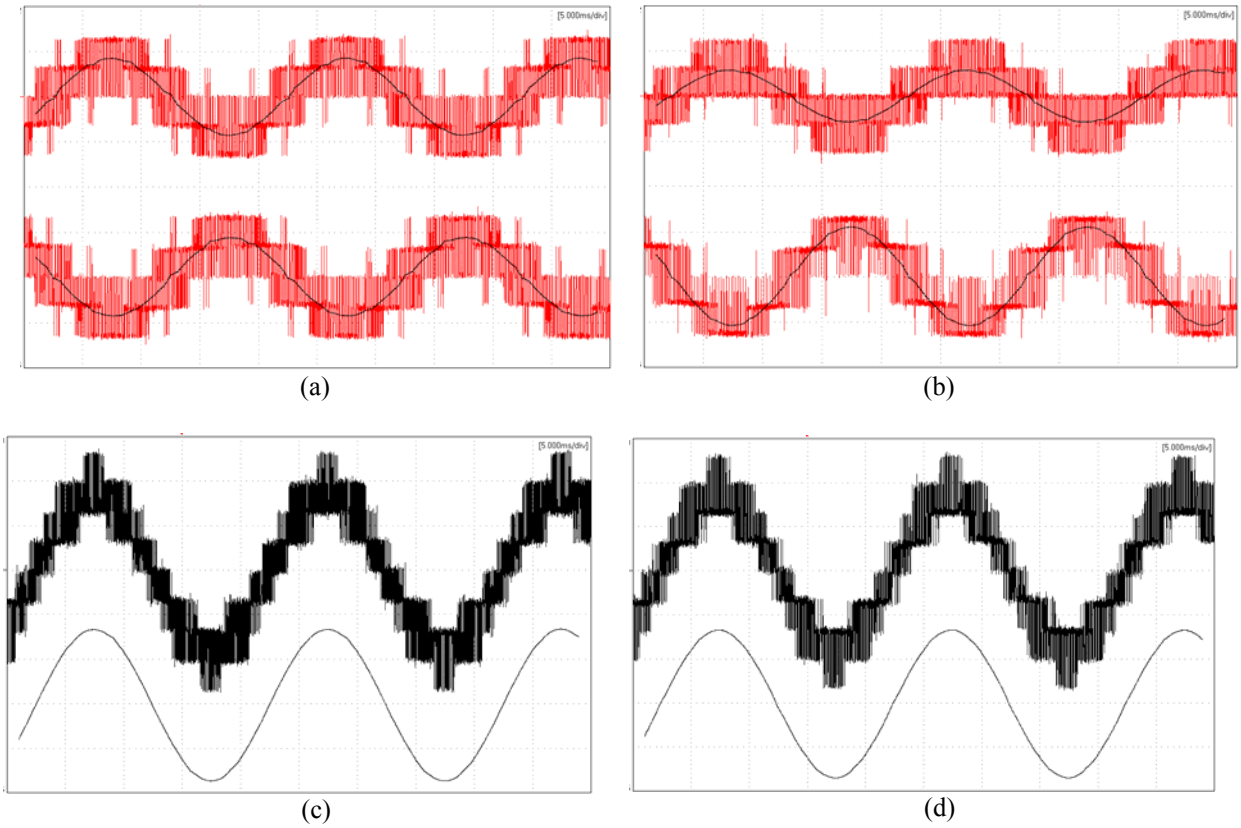


Fig. 23. Voltage output v_1 for $m = 0.75$ (5 ms/div, 20 V/div) (a) Single inverters voltage with fundamental for $k = 0.5$ (b) Single inverters voltage with fundamental for $k = 0.65$ (c) Voltage output v_1 for $k = 0.5$, (d) Voltage output v_1 for $k = 0.65$.

voltage utilization, as specified by (3) and (4). Figures 23(b) and 23(d) show corresponding total output voltages containing maximum nine output voltage levels, followed by its fundamental component. Note that in two cases both output voltages provide equal fundamental component, only individual inverters provide different voltage share.

4.4. Summary

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding a three-phase load with open-end windings has been analyzed in this paper. The dc supplies insulation allows full dc bus utilization and avoids common mode currents without the need of a common mode reactor. The paper has been focused on the development of a modulation strategy able to regulate the power sharing between the dc sources and on the determination of a correct switching sequence for the two inverters. It has been shown that an unbalanced power sharing between the two inverters is possible.

A switching sequence has been proposed which ensures the correct multilevel operation and the possibility to limit the number of simultaneous commutations to one. The experimental tests confirm the effectiveness of the proposed modulation strategy.

4.4.1. Appendix

A. Inequalities for the relative position of the switching sequences (interval t_x)

With reference to Fig. 19, (22)-(27) can be easily derived setting $t_y = 0$ on the figure. The following inequalities need to be satisfied in order to prove the existence of time intervals for all six vector combinations shown in Fig. 19

- $(\bar{v}_{aH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_E$:

$$0 \le t_{aH} - t_x, \tag{47}$$

- $(\bar{v}_{oH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_D$:

$$t_{aH} - t_x \le t_{bL}, \tag{48}$$

- $(\bar{v}_{oH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_C$:

$$t_{bL} \le t_{aH} - t_x + t_{oH}, \tag{49}$$

using (2) leading to (24).

- $(\bar{v}_{bH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_E$:

$$t_{oL} \le t_{bH} - t_x, \tag{50}$$

- $(\bar{v}_{bH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_D$:

$$t_x \le t_{oL}, \tag{51}$$

- $(\bar{v}_{aH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_C$:

$$0 \le t_x, \tag{52}$$

Additionally the solution for t_x exists if the following condition derived from (22)-(27) is valid:

$$\max\{0, t_{aH} - t_{bL}, t_{oL} - t_{bH}\} \le \min\{t_{aH}, T_s - t_{bH} - t_{bL}, t_{oL}\}, \tag{53}$$

It can be proved by verifying, one by one, all nine possible combinations of quantities on the left and right side of the inequality. For this purpose, (19)-(21) must be applied. As an example, the condition by combining (22) and (25):

$$t_{oL} - t_{bH} \le t_{aH}, \tag{54}$$

application of (2) yields

$$t_{oL} \le T_s - t_{oH}, \tag{55}$$

which is true due to (21). A similar procedure can be used for the remaining combinations.

B. Inequalities for the position of the switching sequences within switching period (interval t_y)

Noting that not more than one of four inequalities:

$$t_{aH} \le T_s / 2, \; t_{aL} \le T_s / 2, \tag{56}$$

$$t_{bH} \le T_s / 2, \; t_{bL} \le T_s / 2, \tag{57}$$

can be false, due to (20), (21) and (2). Furthermore, due to (14) for the reference in A-half the false inequality can be only one of (56). Using (24) and regrouping terms gives

$$t_{bH} + t_x - T_s / 2 \le T_s / 2 - t_{bL}, \tag{58}$$

and due to (57)

$$t_{bH} + t_x - T_s / 2 \le t_x, \;\; 0 \le T_s / 2 - t_{bL}, \tag{59}$$

which means that exists solution t_y satisfying (28)-(29).

Due to the symmetry, reasoning can be analogously repeated for the B-half taking into account that the false inequality can be only one of (57), giving the existence of the solution (38).

C. Inequalities for elimination of double instantaneous commutation (interval t_c/t_d)

To prove existence of the solution (45) for t_c it is enough to use already proved (30)

$$0 \le t_y, \tag{60}$$

and (29)

$$0 \le T_s / 2 - t_{bH} - t_x + t_y. \tag{61}$$

Similarly for B-half and parameter t_d by using (38) it is evident:

$$0 \le t_y, \; 0 \le T_s / 2 - t_{aL} - t_y \tag{62}$$

proving existence of non-negative t_d.

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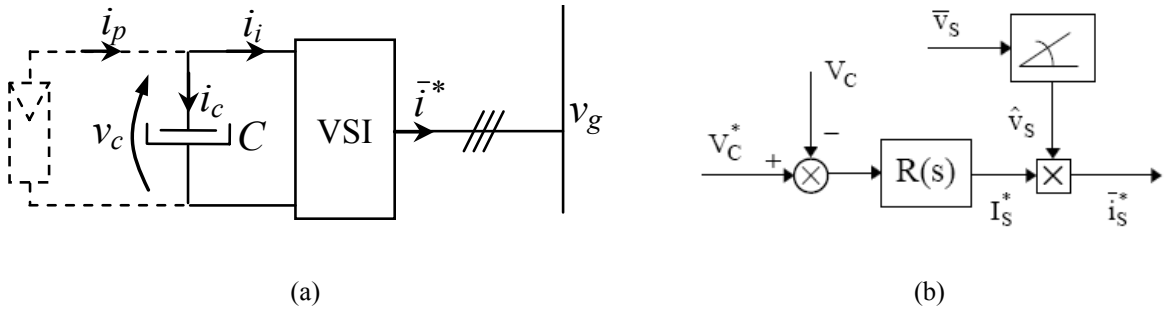
5. Grid connection of dual inverter

Following the general path of power electronics converters, which started from drive applications, during the last decade or two multilevel converters are penetrating into new areas in power generation and active power filtering. These grid-connected applications emerged from the reduced cost and increased reliability of power semiconductor components and digital signal control technology. However, the new solutions introduced some specific issues such are dc voltage control, current control and grid synchronization, both for standard two-level inverter, and even more for multilevel that introduces additional complexity of the control system. These aspects of the control systems are discussed here both theoretically and experimentally. The question of the dc supply is abstracted as much as possible, to have more general approach. Only in the final section, a particular source was chosen for the need of experimental tests. Both numerical and experimental tests are performed for the same operating conditions, showing the system response.

5.1. DC voltage regulation

The first applications of the inverters were in variable speed ac drives, which are the most common industrial loads. They were typically with constant dc voltage provided usually through a unidirectional diode grid rectifier, relieving the control from the dc voltage task. However, this voltage still had to be monitored since bidirectional nature of the inverter could charge it during the drive breaking. In grid-connected applications the converter structure somewhat inversed: dc link is not supplied anymore from the dc side with such stiff source such is grid, so dc voltage control is a typical task, and with available of bidirectional power flow on the ac side. The standard voltage source inverter connected to grid is shown in Fig. 1(a), with dc-source denoted with dashed lines. If source is not present, the inverter can work only as an active power filter with grid-injected active power equal to zero. In practical implementation, due to the losses, the inverter requires a small active power to cover losses eventually leading to capacitor discharge. If a dc source is connected (photovoltaic, wind, fuel cell, battery…) power flow can be to the grid, and additionally in some cases from the grid, depending on the sources nature (e.g. batteries and wind turbines can also receive power). Since the voltage of the capacitor is proportional to the energy stored:

$$E_C = \int v \cdot \mathrm{d}q = \frac{1}{2} C V^2 , \tag{1}$$



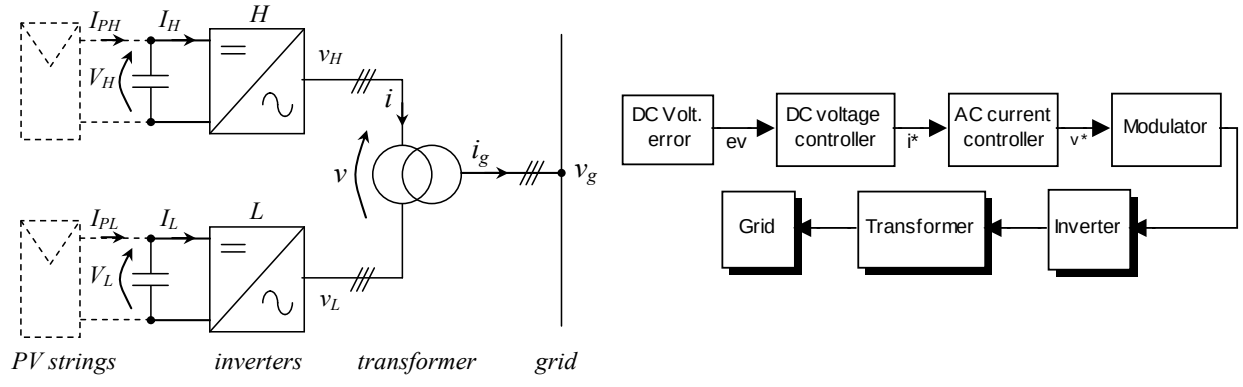
(a) (b)

Fig. 1. Grid-connected VSI (a) structure (b) block diagram of the simple control system.

the voltage v_c can be controlled by active current component of the inverter in a simple manner, illustrated in Fig. 1(b). If desired voltage V_c^* is lower than actual V_c, meaning negative error signal, charging active current reference I_s^* should decrease for the discharge of the capacitor. Therefore, current reference direction has to be supplying (from the grid), and the output current is the only ac variable being controlled. The controller does not have to be as fast as current controller due to relatively high electrical inertia of the capacitors, which eases the tuning of the nested controller structure. Afterward, the result must be added to the reference current value. In each grid-connected application, usually there is an inner control loop for current control and an outer control loop for DC part control [1], [2].

In the case of a dual-inverter, the control algorithm is more complex than for a single inverter, having additional degree of freedom ac voltage sharing between two inverters "H" and "L" to be controlled as well. This additional degree of freedom can be addressed in different ways, as will be presented. A quite complex scheme is the multivariable linear quadratic regulator based on state-space models [3], [4]. It has been applied to the equivalent problem of dc-link neutral-point voltage regulation of a three-level neutral-point-clamped (NPC) inverter. A different solution would be the independent control of each inverter [5], [6], at the price of loss of proper multilevel waveform as already discussed in Chapter IV. In what follows two simple solutions are proposed, using a combination of PI-controllers, thus making straightforward and effective solutions.

The voltage references for the two dc-link voltages V_H^* and V_L^* are determined by the application, and they can be fixed (e.g. active power filter) or variable (e.g. renewable



(a) (b)

Fig. 2. Dual inverter application (a) grid connection (b) block diagram of the structure.

generation). Although the dc bus voltage reference, V_{dc}^*, is the same for both inverters, two distinct voltage controllers have to be implemented to guarantee the system stability for any operating condition. The converter structure is represented in the block diagrams of Fig. 2. In this chapter, the voltage control is described in more detail while the outer loop such is generation and other necessary supervisory tasks are addressed in the Chapter 7.

5.1.1. Proposed proportional current reference

The block diagram of the control system is shown in Fig. 3, with the reference to the structure in Fig. 2(a). The two dc voltages (V_H, V_L) are controlled by two proportional-integral controllers, giving as output the reference of two dc currents (I_H^*, I_L^*). The calculation of inverter output current reference I^* is based on a power balance equation written in steady-state conditions. If the inverter current injected into the grid is in phase with the grid voltage, neglecting inverter and transformer losses the power balance yields

$$V_H I_H + V_L I_L = 3V_g' I\,, \tag{2}$$

where V_g' is RMS grid voltage at the inverter side and I is RMS ac output current of the inverters. Thus, the current reference can be obtained as

$$I^* = \frac{1}{3}\frac{V_H I_H^* + V_L I_L^*}{V_g'}\,, \tag{3}$$

The current injected into the grid is assumed to be in phase with grid voltage, i.e. having only active component, as stated above. The resulting current space vector reference $\bar{i}^*$ for the converter is

$$\bar{i}^* = I^* \hat{v}_g\,, \tag{4}$$

being $\hat{v}_g$ the unity space vector of the grid voltage. For an active power filter operation, reactive and/or harmonic compensation current references can be added in (4).

The coefficient k has a limited variation range depending on the value of the reference output voltage $\bar{v}^*$, as already explained in 3.7. An estimation of the coefficient k can be easily carried out by a simple power balance written assuming $V_H \cong V_L \cong V_{dc}^*$:

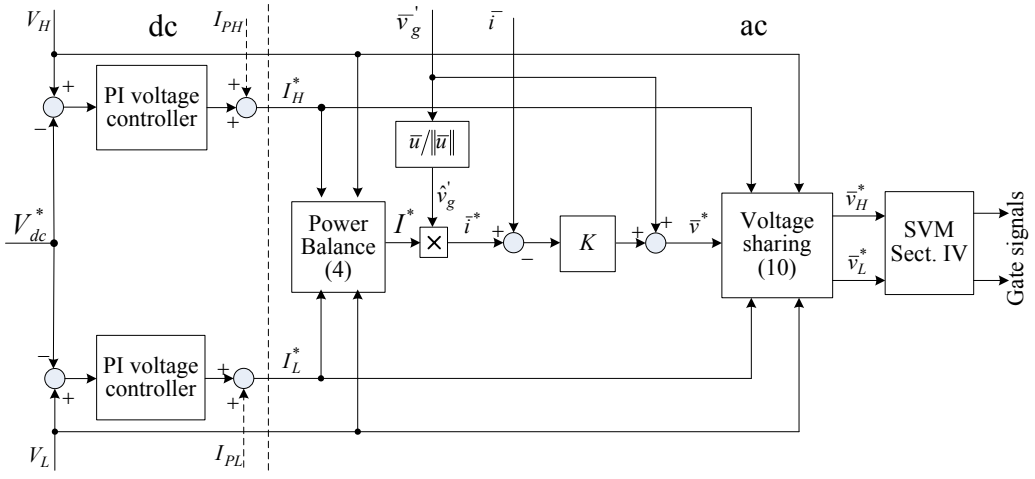


Fig. 3. Block diagram of the proposed control system.

$$k = \frac{p_H}{p} = \frac{V_H I_H}{V_L I_L + V_H I_H} \cong \frac{I_H}{I_L + I_H}, \tag{5}$$

As a consequence, by combining (5) and the definition of coefficient (3.71) the inverter reference voltages $\bar{v}_H^*$, $\bar{v}_L^*$ can be determined as

$$\bar{v}_H^* = \frac{I_H^*}{I_H^* + I_L^*}\bar{v}^*, \ \bar{v}_L^* = \frac{I_L^*}{I_H^* + I_L^*}\bar{v}^* \tag{6}$$

Power sharing coefficient *k* requires more attention since its "reference direction" is highly dependent on the power flow direction. E.g.

- Active filter mode (DI receives active power): $V_H > V_L \Rightarrow k > 0.5 \Rightarrow$ inverter H gets less power
- Generation mode (DI gives active power): $V_H > V_L \Rightarrow k < 0.5 \Rightarrow$ inverter L gives less power

The controllers' outputs I_H^*, I_L^* are limited to positive values, which correspond to the generation only. Similarly, for active power filter application the references can be simply limited to negative values. Furthermore, it has to be verified that both references are within the range of achievable output voltages of each inverter, which depend on their dc voltages. In the case of a single inverter topology, if the voltage demand exceeds available dc voltage, the output voltage is simply saturated. With the dual inverter configuration, total voltage reference must be satisfied, so in case of voltage saturation of one inverter the second has to provide for the missing part. Total voltage reference $\bar{v}^*$ is determined by the current control routine, but to effect modulation it is necessary to determine single inverter voltage references $\bar{v}_H^*$ and $\bar{v}_L^*$. The first limit is maximum available voltage:

$$\left|v^*\right| \le \frac{V_H + V_L}{\sqrt{3}}, \tag{7}$$

Power sharing factor k is determined on the basis of the "displacement" between two dc voltages, e.g. by delta controller. It determines power sharing between two inverters:

$$\begin{gathered} \left|\bar{v}_H^*\right| = (1-K)\left|\bar{v}^*\right|, \text{ if } \left|\bar{v}_L^*\right| = K\left|\bar{v}^*\right| \\ v_{\alpha H}^* = (1-K)v_\alpha^*, \ v_{\beta H}^* = (1-K)v_\beta^*, \ v_{\alpha L}^* = Kv_\alpha^*, \ v_{\beta L}^* = Kv_\beta^* \end{gathered} \tag{8}$$

However not more than one of the inequalities can be false, due to (7):

$$\left|\bar{v}_H^*\right| \le \frac{V_H}{\sqrt{3}}, \ \left|\bar{v}_L^*\right| \le \frac{V_L}{\sqrt{3}} \tag{9}$$

reference values become:

$$\left|\bar{v}_H^*\right| = \frac{V_H}{\sqrt{3}}, \ \left|v_L^*\right| = \frac{K}{1-K}\frac{V_H}{\sqrt{3}}, \text{ if } K \le \frac{V_L}{V_H + V_L} \tag{10}$$

or:

$$\left|v_H^*\right| = \frac{1-K}{K}\frac{V_L}{\sqrt{3}}, \ \left|v_L^*\right| = \frac{V_L}{\sqrt{3}}, \text{ if } K \ge \frac{V_L}{V_H + V_L} \tag{11}$$

This problem was addressed in [7], with algorithm shown in Fig. 4.

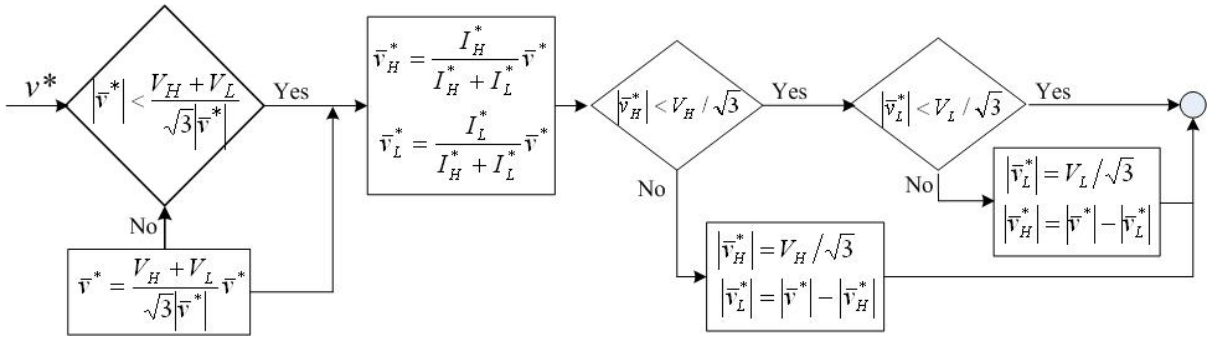


Fig. 4. Block diagram of the voltage reference saturation algorithm.

A feed-forward action can be added in order to compensate sudden changes in PV currents (dashed lines I_{PH}, I_{PL} in Fig. 3). This compensation requires the presence of two further current transducers, but it makes possible higher dynamic response to be achieved [7]. It should be noted that sensorless reconstruction of the inverters dc-link currents from the output current is not possible due to very high ripple content. Only the opposite is true: low-frequency output current can be reconstructed by using only dc-link sensor, with numerous proposed methods such is [8].

5.1.2. Proposed Σ-Δ controller

Another control scheme for a given dual inverter structure is presented in Fig. 5, again with the application of two PI controllers for two dc voltages V_H, V_L, but organized in a "sigma - delta" (Σ-Δ) linear combination [9]. Again, dc-bus voltages V_H and V_L are independently controlled to guarantee the system stability for any operating condition. However, within this chapter equal references $V_H^* = V_L^*$ are presumed.

In particular, V_H and V_L are regulated by two PI controllers, here called "sigma" (Σ) and "delta" (Δ). The voltage controller Σ acts in order to set the average value of dc bus voltages (i.e., their sum), whereas the voltage controller Δ acts in order to set the difference between the dc bus voltages (i.e., their difference). The input signals of both voltage controllers, V_Σ and V_Δ, can be built by adding and subtracting each other the individual dc voltage errors ΔV_H and ΔV_L, as follows

$$\begin{cases} V_\Sigma = \Delta V_H + \Delta V_L = (V_H + V_L) - (V_H^* + V_L^*) \\ V_\Delta = \Delta V_H - \Delta V_L = (V_H - V_L) - (V_H^* - V_L^*) \end{cases}, \tag{12}$$

being

$$\begin{cases} \Delta V_H = V_H - V_H^* \\ \Delta V_L = V_L - V_L^* \end{cases}, \tag{13}$$

and finally

$$\begin{cases} V_\Sigma = \Delta V_H + \Delta V_L = (V_H + V_L) - 2V_{dc}^* \\ V_\Delta = \Delta V_H - \Delta V_L = V_H - V_L \end{cases}, \tag{14}$$

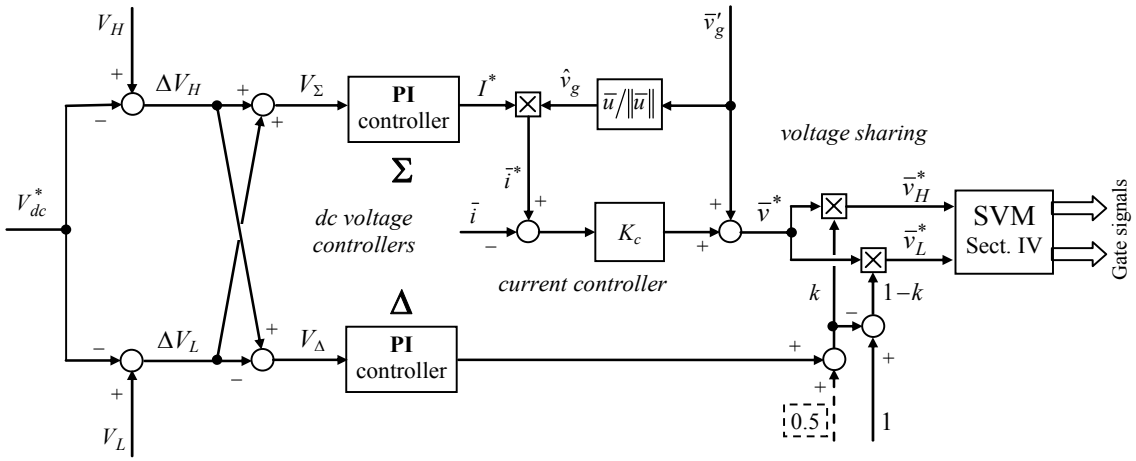


Fig. 5. Block diagram of the regulation system.

Therefore outputs of the two controllers are providing directly references I^* and k^*, instead by (3) and (5), from the previous method, respectively. The rest of the block diagram is analogous as in the previous subsection.

5.2. Current control

Current control in grid-connected applications differs significantly from the current control in drive applications for a few reasons:

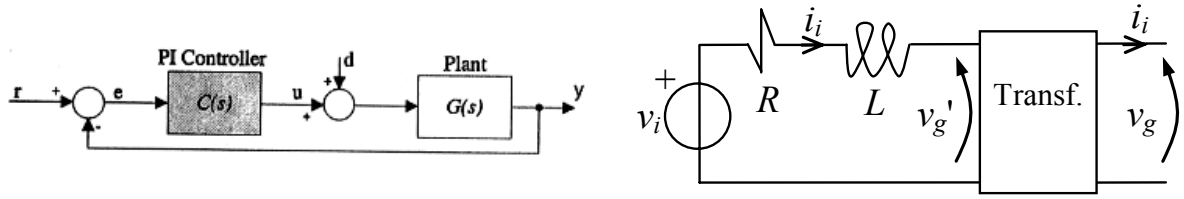
- Grid voltage, which behaves as disturbance, is distorted, in contrast to motor back-EMF, which is very pure by the design.
- Current reference is distorted for active-power filter, sinusoidal only for pure generation, in contrast to drives where sinusoidal reference is required to diminish torque oscillations.
- Equivalent inductance, behaving as a filter, is smaller on the order of a magnitude with respect to drives. The reason is the inductive nature of the motor as a load. This significantly aggravates the current control issues.

Control strategies can be generally classified in two large groups [10]

- Linear current controllers (PI controllers in various reference frames),
- Nonlinear controllers (hysteresis, delta, dead-beat with or without predictive algorithms).

5.2.1. Survey of current control techniques

In this section, fundamental current control techniques of three-phase voltage source PWM inverters are discussed. Only two major tasks of the control system will be discussed: reference tracking and disturbance rejection, adopting the linear current control methods as the most popular. The major reason for the popularity of the linear controllers is separation between current error compensation and voltage modulation. It enables fully independent design of the overall control structure, so open loop testing of the converter and load can be easily performed.



(a) (b)

Fig. 6. Block diagram of the linear control system (a) Overall structure. (b) equivalent circuit.

Furthermore, it allows exploiting the advantages of open-loop modulators: constant switching frequency, well-defined harmonic spectrum, optimum switching pattern and good dc link utilization. In the block diagram represented in Fig. 9(a) for given $G(s)$ the output depends both on input $R(s)$, disturbance $D(s)$ and chosen controller $C(s)$. The output equation Y(s) in Laplace domain gives:

$$Y(s) = \frac{C(s)G(s)}{1 + C(s)G(s)} R(s) - \frac{G(s)}{1 + C(s)G(s)} D(s). \tag{15}$$

For current control plant, transfer function is usually simplified to

$$G_i = \frac{1/R}{1 + Ts}, \tag{16}$$

and $T = L/R$ is time constant.

To achieve good reference tracking and disturbance rejection tasks means

$$\frac{C(s)G(s)}{1 + C(s)G(s)} \approx 1, \quad \frac{G(s)}{1 + C(s)G(s)} \approx 0, \tag{17}$$

for all the values of s. Since $C(s)$ changes with s, condition (17) cannot be fulfilled ideally, because it would mean

$$C(s) \to \infty, \tag{18}$$

so a tradeoff is required. From the Laplace final value theorem:

$$\lim_{t \to \infty} y(t) = \lim_{s \to 0} sY(s) \tag{19}$$

yields the condition to achieve zero steady-state error:

$$\lim_{s \to 0} C(s) \to \infty, \tag{20}$$

In the following two most typical cases will be analyzed: constant and sinusoidal reference values:

A. Constant reference values

$$R(s) = I_m/s, \; D(s) = E_m/s, \tag{21}$$

The output becomes

$$Y(s) = \frac{I_m}{s} \frac{C(s)}{R + RTs + C(s)} - \frac{E_m}{s} \frac{1}{R + RTs + C(s)} \tag{22}$$

Applying the Laplace final value theorem (19) gives conditions for the zero steady-state error

$$\lim_{s\to 0}\frac{C(s)}{R+RTs+C(s)}=1,\quad \lim_{s\to 0}\frac{1}{R+RTs+C(s)}=0, \tag{23}$$

yielding again condition (20). The simplest possibility to achieve goal (1) is to choose P-controller with infinite gain k:

$$C(s)=k,\quad k\to\infty, \tag{24}$$

since:

$$\lim_{s\to 0}\frac{k_p}{R+RTs+k_p}=\frac{k_p}{R+k_p},\quad \lim_{s\to 0}\frac{1}{R+RTs+C(s)}=\frac{1}{R+k_p}, \tag{25}$$

Obviously infinite gain is not realistic in practice due to the noise. Another possibility to "obtain infinity" is division with zero:

$$\lim_{s\to 0}C(s)=\lim_{s\to 0}\frac{k_i}{s}\to\infty, \tag{26}$$

Therefore for dc quantities control it is enough to have I-controller, however in the further analysis it shows too slow transient response. Finally, a combination of the previous two actions is used to unite zero steady state error and good dynamics, forming a PI controller

$$C(s)=k_p+\frac{k_i}{s}, \tag{27}$$

For given constant reference obtains the following reference tracking

$$Y(s)=\frac{I_m}{s}-\frac{RTs+R}{RTs^2+Rs+k_ps+k_i}I_m, \tag{28}$$

Now by choosing parameters k_p and k_i dynamic response can be tuned (underdumped, critically dumped etc.).

The simplicity and effectiveness of the PI current control for constant reference lead to the development of the synchronous reference frame control, also called *dq* control. With a dissemination of the ac motor drives, it established as a industrial standard. The same principle could be implemented in the grid-connected application, transforming the grid current and voltage waveforms into a reference frame that rotates synchronously with the grid voltage e.g., *abc→dq*. By means of this, the control variables become dc values; thus, filtering and controlling can be easier achieved. For improving the performance of PI controller in such a structure as depicted in Fig. 7, cross-coupling terms and voltage feedforward are usually used [11].

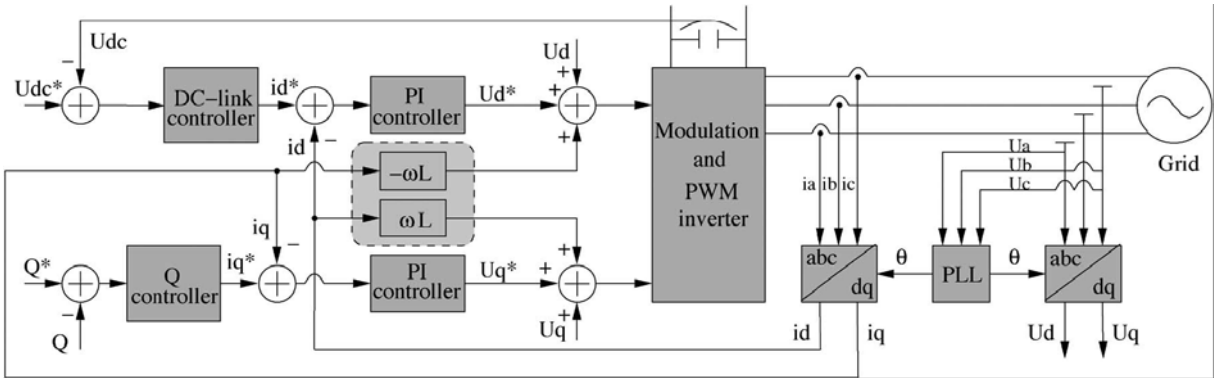


Fig. 7. General structure for synchronous rotating frame control structure.

Nevertheless, as will be shown, the compensation capability of the low-order harmonics in the case of PI controllers is very poor, standing as a major drawback when using it in grid-connected systems.

B. Sinusoidal reference values

Another possible approach is to remain in the stationary reference frame, as shown in Fig. 8. In this case, the grid currents are transformed into stationary reference frame using the $abc \rightarrow \alpha\beta$ module. However zero steady-state error previously derived for constant reference and constant disturbance cannot be generalized to all the other cases. A well known example comes from the drive application, where PI controller cannot regulate current during transient while speed and consequently disturbance is changing [12]. Since the control variables are sinusoidal in this situation and due to the known drawback of PI controller in failing to remove the steady-state error when controlling sinusoidal waveforms, employment of other controller types is necessary.

It can be easily shown that PI controller cannot regulate sinusoidal quantities starting by transformation of the sinusoidal references

$$r_s(t) = \sin \omega t\,, \quad r_c(t) = \cos \omega t\,, \tag{29}$$

into Laplace domain gives

$$R_s(s) = \frac{\omega}{s^2 + \omega^2}\,, \quad R_c(s) = \frac{s}{s^2 + \omega^2}\,, \tag{30}$$

with the difference between sine and cosine rising from Laplace initial value theorem:

$$\lim_{s \to \infty} sR(s) = r(0-)\,. \tag{31}$$

However in this case final value theorem cannot be applied since all poles of polynomial $sF(s)$ are not in the left-hand plane:

$$Y(s) = \frac{k_p s + k_i}{s(R + RTs) + k_p s + k_i} \frac{\omega}{s^2 + \omega^2}\,, \tag{32}$$

The output contains term:

$$\frac{As + B}{s^2 + \omega^2}\,, \tag{33}$$

where A and B represents phase and amplitude difference between reference and output. Although controller parameters k_p and k_i can be chosen to provide proper output ($A = 0$, $B = \omega$), or neutralize the disturbance in a similar manner, but cannot fulfill both equations

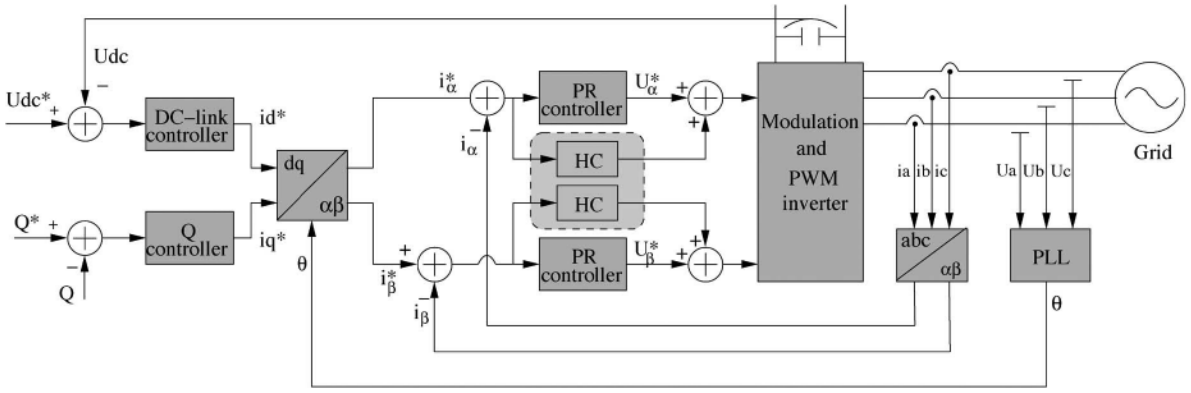
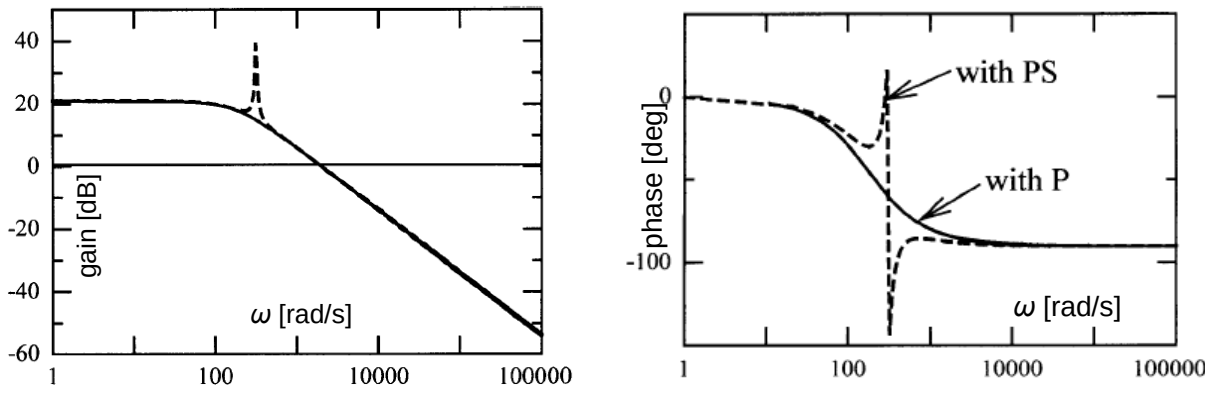


Fig. 8. General structure for stationary reference frame control structure.



(a) (b)

Fig. 9. Bode diagram of the resonant controller (a) gain, (b) phase characteristic.

simultaneously. The main drawback of this controller is a relatively small gain around fundamental frequency.

C. Resonant current controllers

Proportional resonant (PR) controller gained a large popularity in the last decade in current regulation of grid-tied systems [13]. Particular characteristic of this controller is the achievement of a very high gain around the resonance frequency, thus being capable to eliminate the steady-state error between the controlled signal and its reference. The width of the frequency band around the resonance point is proportional to on the integral time constant k_i [11]. This controller has transfer function directly derived form PI controller, but for the case of sinusoidal reference:

$$\lim_{s\to j\omega} C(s) = \lim_{s\to j\omega} (k_p + \frac{k_i s}{s^2+\omega^2}) \to \infty, \tag{34}$$

The Bode diagram of the controller compared with only a P regulator and regulator is compared in Fig. 9.

Sometimes it is called generalized integrator, since for $\omega = 0$ it gives ordinary integrator. Note that it also behaves as an integrator since it satisfies the equation:

$$\frac{d^2 f}{dt^2} + \omega^2 f = k\frac{du}{dt}, \tag{35}$$

so it can give non-zero output for zero input, on the basis of previous non-zero input. The method however does not require the grid phase angle, but it does not make an important advantage over the other methods since some sort of the angle detection is necessary for dc voltage control. Because this controller acts on a very narrow band around its resonant frequency ω, the implementation of harmonic compensator for low-order harmonics is possible without influencing at all the behavior of the current controller [14]. However, it leads to the significant increase of the computational burden, which is the main drawback of this controller.

5.2.2. Proportional controller

As previously stated, the transforms such are Clarke (*αβ*-domain) or Park (*dq*-domain) lead to the introduction of low order harmonics due to distorted grid voltage and consequently current distortion. For this reason, the control is chosen to be in original *abc*-domain. Since the two inverters "H" and "L" supply the transformer's winding from both sides (open-ends), their output ac current is the same: $\bar{i} = \bar{i}_H = \bar{i}_L$, depicted in Fig. 2(a). The Σ voltage controller directly generates the magnitude of the current reference for the dual inverter, I^*, corresponding to the active power injected into the grid, as shown in Fig. 5. If the ac current is in phase with the grid voltage, the resulting current space vector reference $\bar{i}^*$ is

$$\bar{i}^* = I^* \hat{v}_g , \tag{36}$$

being $\hat{v}_g$ the unity space vector of the grid voltage, that can be estimated by the standard phase-locked loop technique. It can be noted that reactive and/or harmonic compensation current references can be added to $\bar{i}^*$ if active power filter operations are required.

To avoid the drawbacks of the discussed control methods, a simple proportional controller in the stationary reference frame has been adopted [15], using the grid voltage as feed-forward action. In this way, the effect of the grid voltage, which is considered as a disturbance, is eliminated, and the converter is able to perform as an active filter if required [16]. Two more circuit elements influence the current control: filter inductance and the transformer. The filter is typically connected on the low voltage side to achieve higher equivalent value of the inductance. Regarding the transformer, two possible feedback current signals can be measured, on the both transformer sides, but better results are obtained on the inverter side (more direct controlled than through the transformer). In particular, for the equivalent circuit given in Fig. 10(a), the voltage equation leads to

$$v^* = Ri + L\frac{\mathrm{d}i}{\mathrm{d}t} + v'_g , \tag{37}$$

with the same denotations as (2), so the reference voltage $\bar{v}^*$ can be calculated as

$$\bar{v}^* = K_c(\bar{i}^* - \bar{i}) + \bar{v}'_g . \tag{38}$$

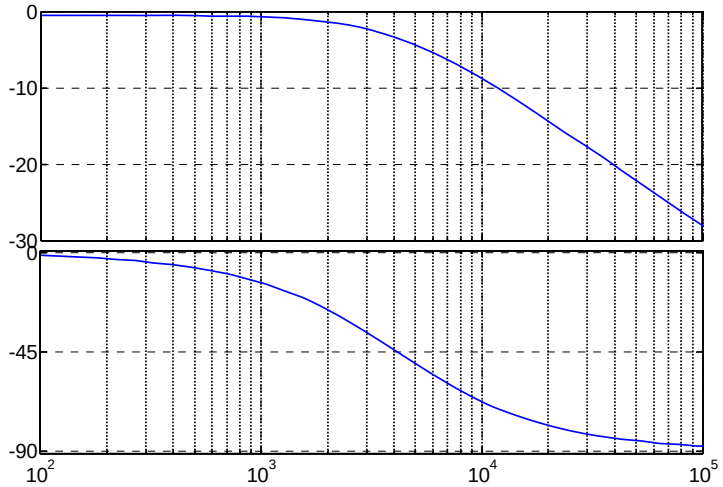


Fig. 10. Bode diagram for proportional current controller for different bandwidth frequency 4000 rad/s.

Transfer function is given by:

$$I(s) = \frac{1}{\frac{L}{K}s + (\frac{R}{K} + 1)} I^*(s) = \frac{\frac{K}{R+K}}{\frac{L}{R+K}s + 1} I^*(s), \tag{39}$$

where grid voltage was exempt from the consideration as a disturbance. Obtained result is a simple first-order filter (i.e. low-pass), with bandwidth angular frequency

$$\omega_{BW} = \frac{R+K}{L}, \tag{40}$$

The choice of K is a compromise between high values giving higher bandwidth but weak filtering (to attenuate noise). The Bode diagram of obtained low-pass filter is shown in Fig. 10(b). The frequency response deteriorates as the frequency increases, e.g. over 1-2 kHz. However, an actual power distribution line exhibits such high inductive impedance as to attenuate existing harmonic components in a higher frequency range. This limitation can be further reduced by slight increase of filter inductance. Furthermore, in the proposed system, a small steady-state current error is not a critical drawback, since the controlled variables are dc voltages.

Regarding the voltage feed-forward, the prerequisites are needed to implement a feed-forward control scheme:

- The disturbance must be measurable,
- The effect of the disturbance to the output of the system must be known,
- The time it takes for the feed-forward controller to affect the output must not be longer than the time it takes for the disturbance.

Since these conditions are met, feed-forward can be tuned to be extremely effective. The practical results will be shown with the experimental results.

5.3. Synchronization with the grid

Synchronization with the grid voltage is equivalent to angle extraction from the voltage signals. The first such application was resolver - rotary electrical transformer used as angle sensor back from WWII. It provided two signals phase shifted by 90°, popularly called quadrature (i.e. orthogonal) signals. In contrast to the resolver, the main difficulty in grid-connected applications is distortion (low-order harmonics) of the voltage due to high proliferation of non-linear (rectifier) loads. The simplest way to extract angle from pair of signals in quadrature (sinus and cosine) is to calculate arctangent. The shortcoming is a lower quality of the output since it is an open loop method. When the angle extraction involves closed loop calculation it is called phase-locked loop (PLL).

5.3.1. Quadrature signals phase-locked loop

The implementation of the closed loop corrects the output by a negative feedback principle. To avoid non-linearity of the trigonometric functions cross-multiplication is applied to get advantage of formula:

$$\lim_{x\to 0}\frac{\sin x}{x}=1, \tag{41}$$

or in a more practical form:

$$\sin\theta\cos\theta_e-\cos\theta\sin\theta_e=\sin(\theta-\theta_e)\approx\theta-\theta_e, \tag{42}$$

giving an error signal of the angle tracking system. Applying a PI controller value of the error has to converge towards zero due to (41). In order to understand this system is useful to make an analogy with current controller for voltage source inerter. The input of the controller is current error, the output is voltage reference since:

$$i=\frac{1}{L}\int v\mathrm{d}t, \tag{43}$$

where L is equivalent inductance of the controlled object. Analogously for a angle tracker the output of the controller will be frequency of the angle because:

$$\theta=\int\omega\mathrm{d}t. \tag{44}$$

Then, having obtained frequency, additional integrator is sufficient to obtain tracked angle. The described system is traditionally called "phase-locked loop" (PLL) shown in Fig. 11. The integrator has been presumed to have unity gain due to the degree of freedom with previous block (PI). Taking into account sinus approximation transfer function become:

$$Y(s)=\frac{(k_p+\frac{k_i}{s})\frac{1}{s}}{1+(k_p+\frac{k_i}{s})\frac{1}{s}}U(s)=\frac{k_ps+k_i}{s^2+k_ps+k_i}U(s)=\frac{2\xi\omega_0s+\omega_0^2}{s^2+2\xi\omega_0s+\omega_0^2}U(s), \tag{45}$$

where the new parameters are:

$$k_p=2\xi\omega_0,\ k_i=\omega_0^2. \tag{46}$$

The error of the system will be:

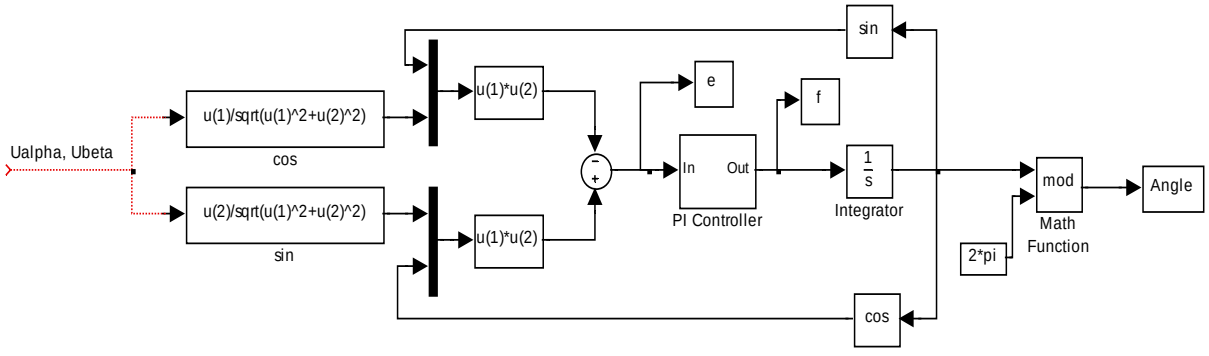


Fig. 11. Block diagram of the PLL.

$$E(s) = Y(s) - U(s) = -\frac{s^2}{s^2 + k_p s + k_i}, \tag{47}$$

when applying Laplace final value theorem (19) gives:

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s) = \lim_{s\to 0} -\frac{s^3}{s^2 + k_p s + k_i} U(s) = 0, \tag{48}$$

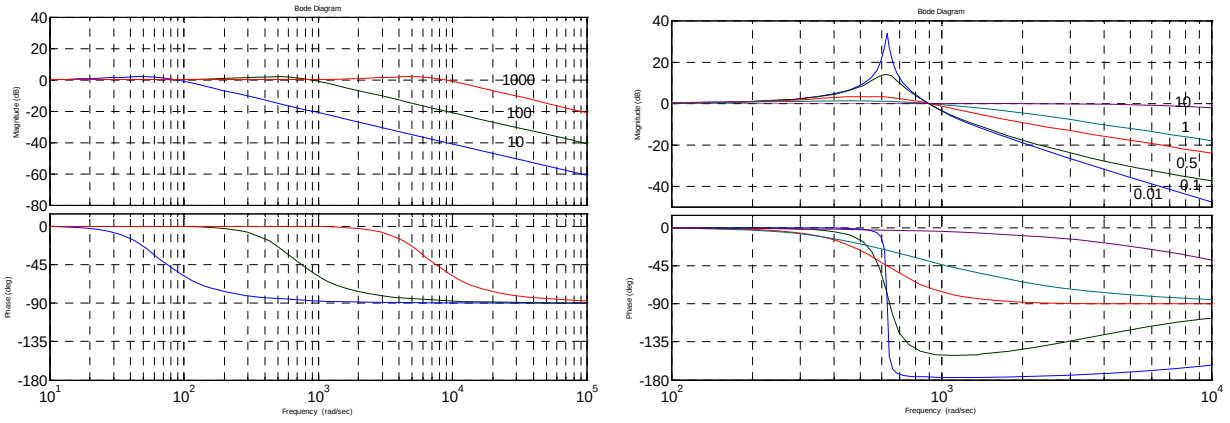
which proves that the output of proposed system is really wanted angle. From (48) yields that system can track constant (corresponding to $1/s$ term in Laplace domain) and linear rising input (corresponding to $1/s^2$), but not the higher order functions. In possible grid application it would mean that the system can determine the angle (linear rise), but cannot track a constant change in frequency. Since the grid frequency changes are very small and slow, the structure can be adopted as a simple and suitable solution, with tracking error inversely proportional to integral gain k_i.

Bode diagrams of transfer functions (45) for different values of the parameters are shown in Fig. 12. It can be seen that by choosing ω_0 close to (known) grid frequency and low-value ξ (around 0.1) provides very strong attenuation of unwanted higher harmonics. Of course, the price is slow dynamic, but with the assumption of the stable grid this drawback is noticeable only during the startup when it takes few seconds for the system to reach steady state. As an example ω_0 = 270 rad/s and ξ = 0.067 can be chosen from the diagrams in Fig. 12. Low value for the damping has been chosen to attenuate harmonics. The response time of the chosen values and frequency of the oscillations can be assessed by known poles expression:

$$y = e^{-\xi\omega_0 t}\left(A\cos\sqrt{1-\xi^2}\,\omega_0 t + B\sin\sqrt{1-\xi^2}\,\omega_0 t\right), \tag{49}$$

The expression $1/\xi\omega_0$ is the time constant, while the $\sqrt{1-\xi^2}\,\omega_0$ is frequency of the oscillations.

It should be noted that PLL is sequence-sensitive, i.e. requires three-phase voltages (a, b, c) have to be in positive sequence, because for proper function requires two signals in quadrature with the second lagging by 90°. This is shown in commonly used diagram where voltage vector rotates in negative mathematical sense, where a-phase reaches maximum before b-phase for 1/3 of a period, analogously as for the position of αβ-axes.



(a) (b)

Fig. 12. Bode diagrams: (a) for ξ = 0.7 and different f_n [Hz], (b) f_n = 100 Hz and different ξ.

5.3.2. Control in dq-domain

In the *dq*-rotating frame, "angle error" can be directly obtained using (42). Denoting that grid voltage is aligned in d-axis, q-axis value has to be ideally zero, i.e. very small in practice. This gives a possibility to apply the same structure as already proposed one (Fig. 11). The whole scheme of the proposed system is shown on Fig. 13(a).

$$\mathbf{v} = E_m[\cos\theta \quad \cos\left(\theta - \frac{2\pi}{3}\right) \quad \cos\left(\theta - \frac{2\pi}{3}\right)]^{\mathrm{t}}, \tag{50}$$

after the application of the Clarke transform become:

$$\mathbf{v} = E_m[\cos\theta \quad \sin\theta]^{\mathrm{t}}, \tag{51}$$

Park transformation gives:

$$\mathbf{v}_{dq} = E_m\begin{bmatrix}\cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e\end{bmatrix}\begin{bmatrix}\cos\theta \\ \sin\theta\end{bmatrix} = E_m\begin{bmatrix}\cos\theta\cos\theta_e + \sin\theta\sin\theta_e \\ \sin\theta\cos\theta_e - \cos\theta\sin\theta_e\end{bmatrix} = E_m\begin{bmatrix}\cos(\theta-\theta_e) \\ \sin(\theta-\theta_e)\end{bmatrix}, \tag{52}$$

The expression (52) has the same form as (42), therefore the system works in the same way [17].

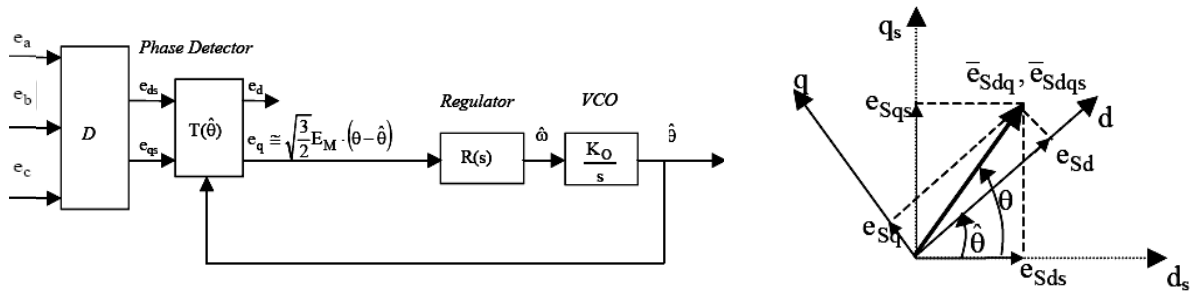
Arbitrary waveform can be dissolved in Fourier harmonic series, but in the three-phase circuits a particular “holistic” approach uses known fact that three-phase symmetrical supply falls to three single-phase circuits. Three-phase quantities are phasors of same frequency, their amplitudes, whereas phase angles may differ. They form an equivalent representation (3 → 3) of symmetric components with common frequency for each three. Applying Clarke transform $\mathbf{S_C}$ to such n^{th} triplet gives:

$$\begin{bmatrix}v_\alpha^{(n)} \\ v_\beta^{(n)}\end{bmatrix} = \mathbf{S_C}V_{abc}^{(n)} = \mathbf{S_C}\begin{bmatrix}v_a^{(n)} \\ v_b^{(n)} \\ v_c^{(n)}\end{bmatrix} = \begin{bmatrix}2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3}\end{bmatrix}\begin{bmatrix}V_n\cos(n\theta+\varphi_n) \\ V_n\cos(n\theta+\varphi_n-2n\pi/3) \\ V_n\cos(n\theta+\varphi_n+2n\pi/3)\end{bmatrix}, \tag{53}$$

The obtained result shows that in αβ-domain it preserves its frequency:

$$\begin{bmatrix}v_\alpha^{(n)} \\ v_\beta^{(n)}\end{bmatrix} = \begin{bmatrix}\frac{2}{3}(1-\cos\frac{2n\pi}{3})V_n\cos(n\theta+\varphi_n) \\ \frac{2}{\sqrt{3}}\sin\frac{2n\pi}{3}V_n\sin(n\theta+\varphi_n)\end{bmatrix}. \tag{54}$$

Taking into account known result that all harmonics phasors (6*k*+1)-order are positive, and (6*k*-1)-order of negative sequence, and applying Park transformation $\mathbf{S_P}$ yields:



(a) (b)

Fig. 13. Tracking filter for angle extraction (a) block diagram, (b) vector diagram.

$$\begin{bmatrix} v_d^{(6k\pm1)} \\ v_q^{(6k\pm1)} \end{bmatrix} = \mathbf{S_P} V_{\alpha\beta}^{(6k\pm1)} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha^{(6k\pm1)} \\ v_\beta^{(6k\pm1)} \end{bmatrix}. \tag{55}$$

and finally:

$$\begin{bmatrix} v_d^{(6k\pm1)} \\ v_q^{(6k\pm1)} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_n \cos((6k\pm1)\theta + \varphi_n) \\ \pm V_n \sin((6k\pm1)\theta + \varphi_n) \end{bmatrix} == \begin{bmatrix} V_n \cos(6k\theta + \varphi_n) \\ \pm V_n \sin(6k\theta + \varphi_n) \end{bmatrix}. \tag{56}$$

Only 6*k*-order harmonics are obtained.

5.4. Experimental results

The aspects of the experimental test will be set forth in the opposite order than in the previous discussion, i.e. starting from the innermost loop towards the outer. At the end, overall results of the system will be presented.

The first microprocessors had fixed-point arithmetic (starting from 8-bit). In the fixed-point arithmetic Q15 numbers were considered in [-1, 1] range in order to save ability of multiplication. Consequently, in this arithmetic all measured values as well as references had to be in this range. This required the introduction of a per-unit system where the system quantities are expressed as fractions of a defined base unit quantity, grouped in Tab. 1. The per-unit system includes:

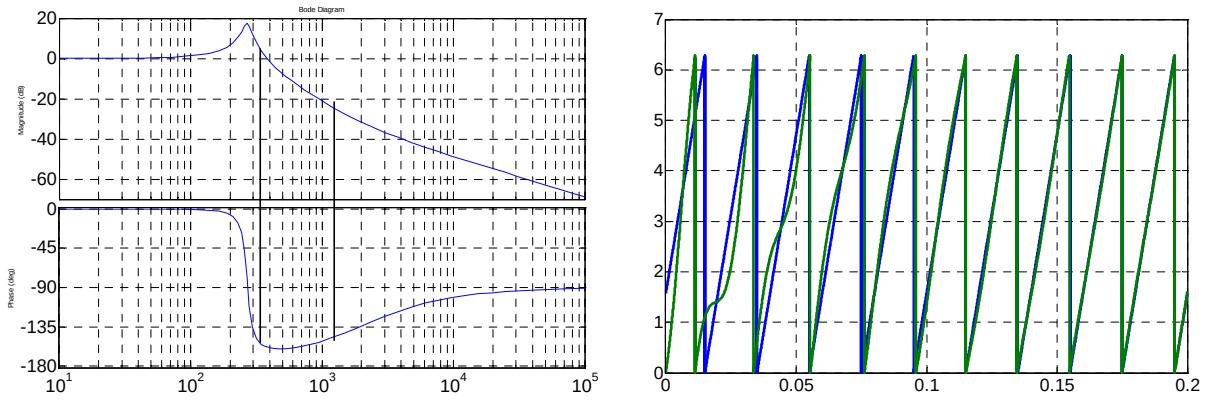
- Measured values
- Input reference values
- Parameters (gains, scaling coefficients etc.)
- Intermediate results
- Output references

In contrast to the old generations of embedded system processors, modern ones with their word length and processing speed came closer to the PC processors enabling the use of the ordinary (human) arithmetic. For example, C2812 processor with 32-bit word, 150 MHz clock and introduced *IQmath* arithmetic is one of the kind. *IQmath* provides 32-bit precision numbers with the range at the choice of the programmer. E.g. "standard" IQ24 format provides range

$$[-128, 127.999999940] \tag{57}$$

Tab. 1. The main parameters of the A/D conversion system.

Quantity	Parameter	Value
AC voltage (grid)	V_G	377.6 V
DC voltage measurement	V_{DC}	50.4 V
AC current (inverter side)	I_I	57 A
DC current	I_{DC}	48 A
Transformer ratio	r_t	9.58



(a) (b)

Fig. 14. Bode diagrams: (a) for chosen values ξ=0.067 and f_n = 43 Hz, (b) angle response.

Furthermore, this concept can be used for tracing/debugging by datalog routine for IQ format numbers. Absolute units control system is natural and straightforward, every action and behavior is clear and direct. This is particularly convenient and time saving for making the simulation (e.g. in *Matlab*), where the processor is very powerful in word length, memory and size. Due to the tradition author used the relative unit system.

5.4.1. PLL

Parameters for the model (Fig. 14) can be calculated using chosen values ω_0 = 270 rad/s and ξ = 0.067:

$$k_p = 2 \cdot 0.067 \cdot 270 = 36.18\,,\; k_i = 270^2 = 72900\,, \tag{58}$$

Regarding the DSP-scaled parameters, it should be noted that DSP integrator is simply an adder, therefore

$$\Delta t = T_s, \tag{59}$$

which has to be taken into account for the parameters:

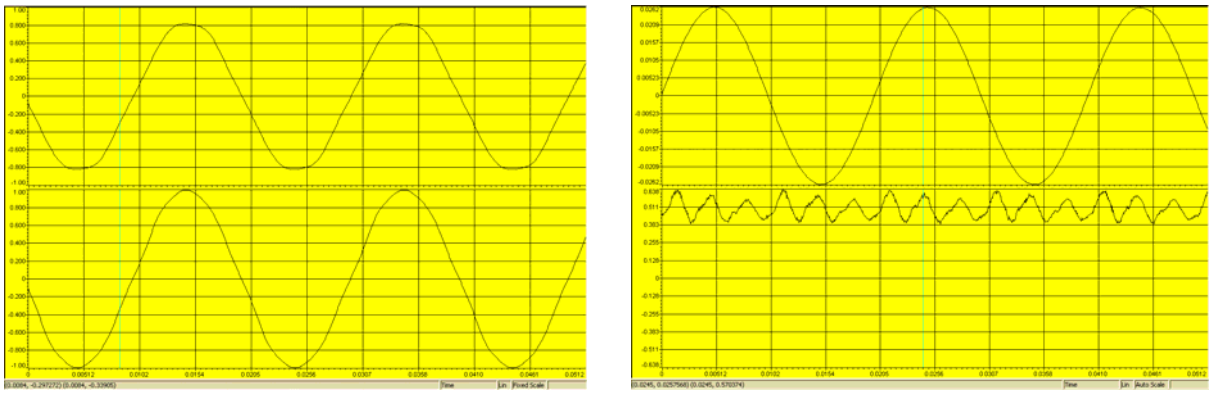
$$k_{pd} = k_p \cdot T_s = 36.18 \cdot 0.00005\,,\; k_{id} = k_i{}^2 T_s^2 = (270 \cdot 0.00005)^2\,. \tag{60}$$

Additionally, if DSP has per unit trigonometric functions the coefficient 1/(2π) has to be inserted in integrator as gain.

The experimental results are shown in Fig. 15(a), showing distorted phase-to-neutral grid voltage in upper trace and obtained PLL output in the lower trace. In Fig. 15(b) shows obtained PLL frequency signal in lower trace, which compared to ideal 50 Hz signal shows strong present of the sixth harmonic from both fifth and seventh harmonic in grid voltage (56).

5.4.2. Current controller parameters

Feedforward action based on (38) is very important because directly influences the work of the current controller. To output of the current controller is voltage reference $\bar{v}^*$ to be produced by the modulator. In relative units, the reference is equal to the modulation index m. The feed-forward is calculated from the measured values of dc voltages V_H and V_L, and measured value of



(a) (b)

Fig. 15. Experimental results: (a) Input phase voltage (upper) and obtained PLL signal (lower), (b) fundamental output and frequency signal (with notable sixth harmonic).

the grid voltage (separately for each phase), here denoted generally as V_G. All these three values are obtained as relative values v_H, v_L and v_G respectively of its correspondent base values V_{DC}, and V_G defined by sensors hardware. Therefore, feedforward term can be calculated:

$$m = v^* = \frac{V_p^*}{V_{pm}} = \frac{V_p^* \cdot \sqrt{3}}{V_H + V_L} = \frac{v_G \cdot (V_G / R_T) \cdot \sqrt{3}}{(v_H + v_L) V_{DC}} = \frac{\sqrt{3} V_G}{R_T \cdot V_{DC}} \frac{v_G}{(v_H + v_L)} \tag{61}$$

where V_{pm} is maximum peak output voltage of the dual inverter

$$V_{pm} = \frac{V_H + V_L}{\sqrt{3}}. \tag{62}$$

Therefore feedforward value of the grid voltage need to be scaled by the coefficient:

$$k_{ff} = \frac{\sqrt{3} V_G}{R_T \cdot V_{DC}} = \frac{\sqrt{3} \cdot 377.6}{57 \cdot 9.58} = 1.2 \tag{63}$$

A test of the proper feed-forward action needs to be performed before to proceed with current control. It is a simple "zero reference test", checking whether the output current is indeed equal to zero for reference set to zero. By comparing feed-forward signal with total output signal the feed-forward signal can be adjusted.

To calculate the feedback gain, parameters of the circuit (primary side) are:

$$R_e = 2 \cdot 2.57\Omega = 5.14\,\Omega, \tag{64}$$

and the equivalent inductance

$$L_e' = L_t' + L_f' = 5 + \cdot 18.4\Omega = 23.4\,\text{mH}, \tag{65}$$

Parameters referred to the secondary side are:

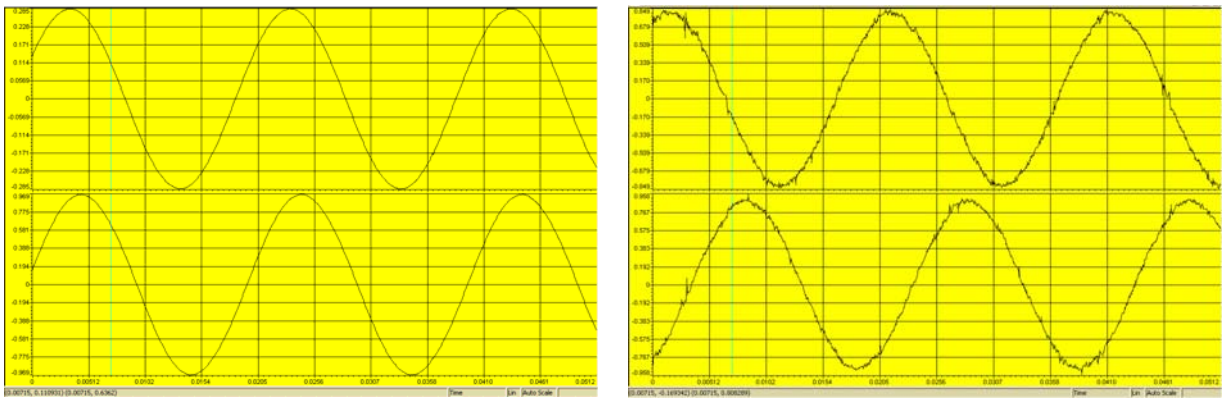
$$R_e'' = R_e' / r_t^2 = 56\ \text{m}\Omega,\ L_e'' = L_e' / r_t^2 = 255\ \mu\text{H} \tag{66}$$

Time constant of the circuit is:

$$T_e = L_e'' / R_e'' = 0.255 / 56 = 4.6\ \text{ms} \tag{67}$$

E.g. for $\omega_{BW} = 3000$ rad/s it gives:

$$K = \omega_{BW} L_e'' - R_e'' = 0.255 - 0.056 \approx 0.71\ \Omega \tag{68}$$



(a) (b)

Fig. 16. Inverter current reference and response for different values of K (a) K = 2.3, (b) K = 3.49

The problem is that this controller introduces attenuation:

$$\frac{K}{R+K}<1 \tag{69}$$

and requires $K>>R$, yielding that K is limited only by the noise. The chosen value is

$$\omega_{BW} = R+K/L = 4140 \text{ rad/s} \tag{70}$$

The attenuation a of the 50 Hz signal is acceptable:

$$a=\frac{K}{R+K}=\frac{1}{0.056+1}=0.95 \tag{71}$$

Finally, applying proper scaling coefficient for the relative unit DSP application can be obtained analogously as (61):

$$k=K\frac{\sqrt{3}I_I}{V_{DC}}=1\frac{50.4}{57}=0.884. \tag{72}$$

The experimental results are shown in Fig. 16, showing the effect of the proper gain choice. The depicted current is current injected to the grid.

5.4.3. Voltage controller parameters

The control structure of ideal system (no delays) for slow changes is shown in Fig. 17. The presumption is that control loop is slow that is does not see changes within one cycle (50 Hz). The ac current magnitude reference I* is proportional to power since voltage is constant and there are in phase. Transfer function is given by:

$$V(s)=\frac{k_p s+k_i}{\mathrm{C}s^2+k_p s+k_i}V^*(s)=\frac{\frac{k_p}{C}s+\frac{k_i}{C}}{\mathrm{s}^2+\frac{k_p}{C}s+\frac{k_i}{C}}V^*(s). \tag{73}$$

where power losses were exempt from the consideration as a disturbance. Obtained result is a second-order filter (i.e. low-pass), with bode characteristic given in the Where the connection between parameters is:

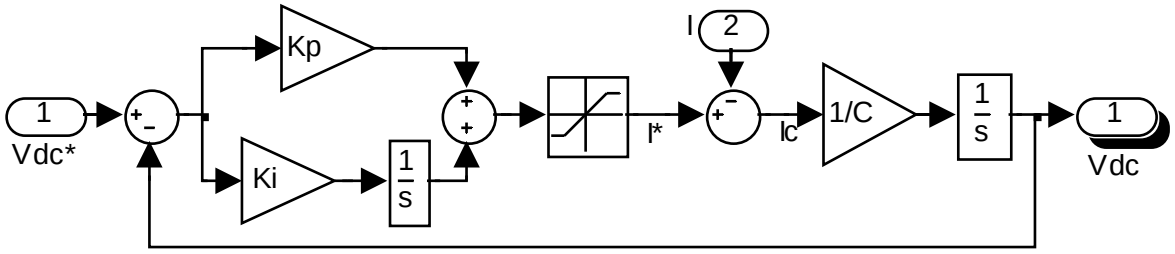


Fig. 17. Block diagram of the voltage regulation system.

$$\omega_0 = \sqrt{\frac{k_i}{C}}\,,\ \xi = \frac{k_p}{2\sqrt{k_i C}}\,. \tag{74}$$

E.g. for chosen $k_p = 0.8$, $k_i = 50$ with $C = 4$ mF, which gives $\omega_0 = 111.8$ rad/s and $\xi = 0.89$, with Bode diagrams shown in Low bandwidth is kept to avoid high-frequency harmonics as well as 100 Hz power oscillations. The response time of the chosen values and frequency of the oscillations can be assessed by known poles expression:
For chosen parameters

$$k_p = 1\,,\ k_i = 50\,,\ (\text{C} = 26.2\ \text{mF}), \tag{75}$$

corresponding to:

$$\omega_0 = \sqrt{k_i / C} = \sqrt{50 / 0.0262} = 43.7\ \text{rad/s}, \tag{76}$$

and

$$\xi = \frac{k_p}{2\sqrt{k_i C}} = \frac{1}{2\sqrt{50 \cdot 0.0262}} = 0.44\,. \tag{77}$$

Finally, applying proper scaling coefficient for the relative unit DSP application gives:

$$k_v = \frac{I_I}{V_{DC}} = \frac{57}{50.4} = 1.13. \tag{78}$$

Additionally k_i has to be T_s time less.

5.4.4. Simulation of the system

The numerical results have been obtained by implementing the whole PV generation system in MATLAB-Simulink environment. The system model parameters are based on the real laboratory prototype used for the experimental tests. The electrical model of each PV string was obtained by fitting the I-V characteristic of a parallel arrangement of six "*Solar Shell*" SP150 modules, including connection cables from the roof to the lab. The I-V and P-V characteristics of the PV modules, used in the simulation are related to the environmental condition during the experimental test in terms of solar irradiance and temperature of the module.

In the first case, Fig. 18, the voltage reference decreases from 38 V to 27.5 V, approximately, corresponding to open-circuit voltage and MPP voltage, respectively (see Fig. 7 (b)). This step leads to a sudden increment of the PV generated power. In particular, Fig. 18(a) shows the time response of dc voltages (V_H and V_L, blue lines) and dc currents (I_H and I_L, green lines) for the two

inverters. It can be seen that the system reaches steady-state condition without overshoot in less than 40 ms, meaning only two periods of grid voltage.

The output of the dual inverter (ac voltage, v, and ac current, i) is shown in Fig. 18 (b). During this transient, there is an increase of the modulation index due to the lowering of the dc voltage. As expected, the instantaneous values of the resulting output voltage v change its waveform from seven-level to nine-level. These results confirm the correct operation of the multilevel modulation technique in these regions. The resulting current ripple practically disappears, as shown in Fig. 18(b).

Fig. 18(c) shows that grid voltage v_g (line-to-neutral) and grid current i_g are in phase, as expected. Being the grid voltage fixed, the current amplitude increases in response of the sudden change of the PV generated power. It can be noted that, for grid-connected application producing only active power, the MPP corresponds to the operating point with maximum grid current amplitude. The second case, Fig. 19, is related to the opposite step of the voltage reference V_{dc}^*,

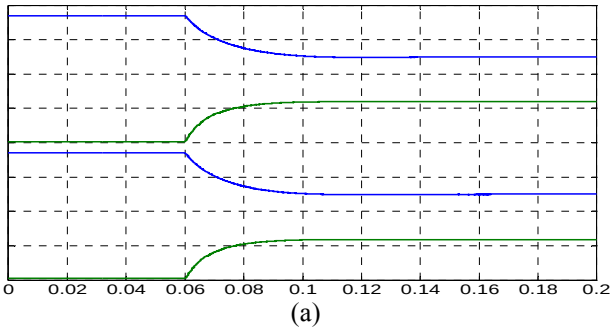


Fig. 18. Step change of V_{dc}^* (decrease) from 37 V to 26 V, time scale 20 ms/div: (a) dc voltage (10 V/div, -40 V offset) and dc current (20 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) converter ac voltage (20 V/div) and converter ac current (20 A/div). (c) grid voltage (150 V/div) and grid current (2 A/div); traces top to bottom.

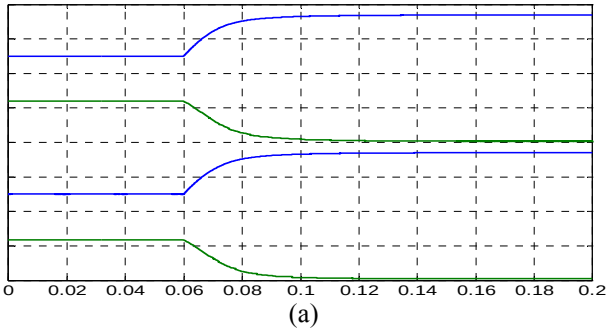


Fig. 19. Step change (increase) of V_{dc}^* from 27 V to 37 V, time scale 20 ms/div: (a) dc voltage (10 V/div, -40 V offset) and dc current (20 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) converter ac voltage (20 V/div) and converter ac current (20 A/div). (c) grid voltage (150 V/div) and grid current (2 A/div); top and bottom traces.

from 27.5 V to 38 V, yielding to a sudden decrement of PV generated power.

Fig. 19 (a) shows the time response of dc voltage (V_H and V_L, blue lines) and dc currents (I_H and I_L, green lines) for the two inverters. Also in this case, the system response is good and steady state condition is reached in few ac periods, without overshoot.

The output of the dual inverter (ac voltage, v, and ac current, i) during the transient is shown in Fig. 19(b). In this case, a decrease of modulation index due to the higher available dc voltage can be noted. Fig. 19(c) shows grid voltage v_g and grid current i_g. The transient affects only the grid current amplitude, as stated for the previous case.

5.4.5. Testing of the system

A grid-connected system based on the implemented dual inverter has been as realized as a prototype. The main characteristics of the whole system are summarized in Tab. 2, whereas the picture of the experimental set-up are given is given in Fig. 20. The system layout is based on two arrays of parallel-connected PV modules SP150 resulting with low voltages around 30-40 V, and a grid-transformer with the proper turn ratio enables voltage adaptation. Here PV modules are used merely as dc voltage sources, in order to test the control algorithm by setting the dc voltage reference for both the inverters, whereas PV generation issues will be discussed in details in the Chapter 6.

The presented control algorithm has been implemented in a TMS320F2812 DSP capable of modulating two three-phase inverters simultaneously and carrying out described control algorithms. The DSP board with the dual inverter, transformers and sensors is shown in Fig. 20.

First of all, the voltage waveforms generated by the dual-inverter configuration are shown to prove the effectiveness of the proposed control scheme when implemented on a real laboratory prototype used for the experimental tests. In particular, Figs. 21 and 22 depict the system responses to step changes in the dc voltage reference V_{dc}^*, assuming $V_H^* = V_L^* = V_{dc}^*$. The voltage excursion has been chosen to be large enough in order to verify both the dynamic response and the stability of the proposed control system. The I-V and characteristic of the PV modules will not be elaborated in details; in general, it behaves like most of the power sources giving lover voltage for higher output current.

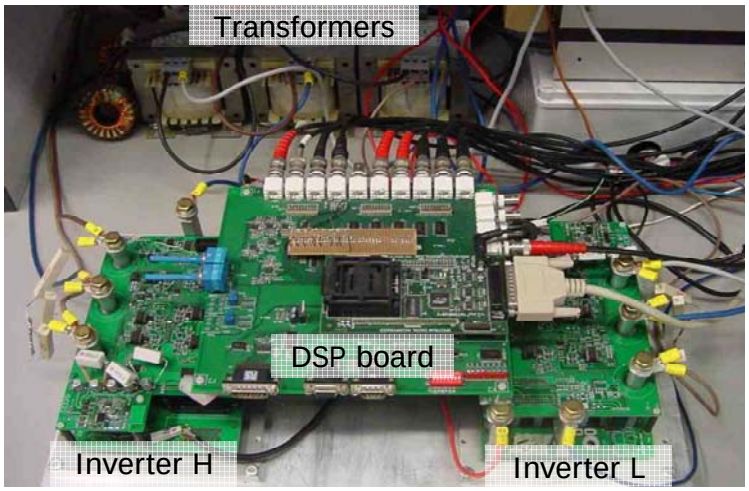


Fig. 20. Dual inverter experimental setup.

Tab. 2. The main parameters of the grid-connected dual inverter system.

Dual inverter	
configuration (H and L)	two-level VSI
MOSFETs (6 in parallel per switch)	IRF2807
MOSFETs ratings	V_{DSS}=75[V]; R_{DS}=13[mΩ]
dc-bus capacitance	23 [mF]
switching frequency	20 [kHz]
Transformer and grid	
turn ratio	230/24 [V/V]
converter/grid-side winding connection	open ends/star
rated power	1500 [VA]
short circuit voltage	6.9 [%]
ac link inductance (converter side)	0.4 [mH]
grid voltage (line-to-line), frequency	250 [V], 50 [Hz]

In the first case, Fig. 21, the voltage reference V_{dc}^* has a step-variation from 38 V to 30 V, approximately, corresponding to open-circuit voltage and point of the maximum PV power, respectively. This variation leads to a sudden increment of the PV generated power. In particular, Fig. 21(a) shows the time response of dc voltage and dc current for both the inverters. It can be seen that the system reaches steady-state condition without overshoot in less than 40 ms, meaning only two periods of grid voltage.

The output of the dual inverter (ac voltage and ac current) is shown in Fig. 21(b). During this transient there is an increase of the modulation index due to the lowering of the dc voltage. As expected, the instantaneous values of the resulting output voltage (v) changes its waveform from seven levels to nine levels. These results confirm the correct operation of the multilevel modulation technique in these regions. The resulting current ripple practically disappears, as shown in the lower trace. Fig. 21(c) shows that grid voltage v_g (line-to-neutral) and grid current i_g are in phase, as expected. Being the grid voltage fixed, the current amplitude increases in response of the sudden change of the generated power. It can be noted that, for grid-connected application producing only active power, the increase of generated power corresponds to the operating point with increased grid current amplitude.

The second case is related to the opposite step of the voltage reference V_{dc}^*, from 30 V to 38 V, yielding to a sudden decrement of generated power. Fig. 22(a) shows the time response of dc voltage and dc current for both the inverters. Also in this case, the system response is good and steady state condition is reached in few ac periods, without overshoot. The output of the dual inverter (ac voltage, v, and ac current, i) during the transient is shown in Fig. 22(b). In this case, a decrease of modulation index due to the higher available dc voltage can be noted. Fig. 22(c) shows grid voltage v_g and grid current i_g. The transient affects only the grid current amplitude, as for the previous case.

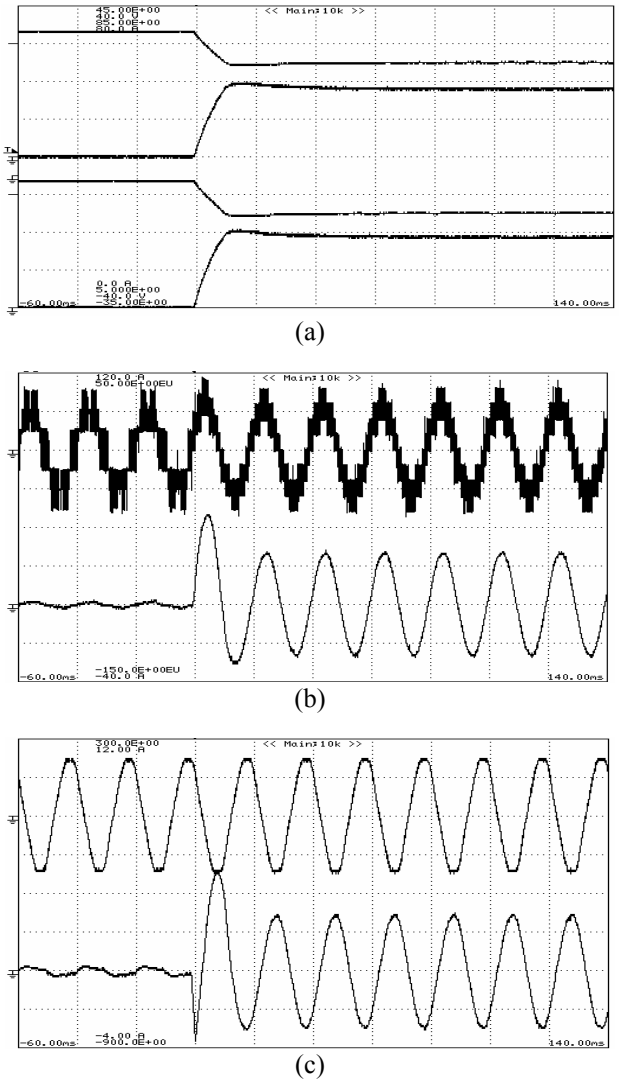


Fig. 21. Step change of V_{dc}^* from 38 V to 30 V, time scale 20 ms/div: (a) dc voltage (10 V/div, 35 V offset) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) converter ac voltage (25 V/div) and converter ac current (20 A/div). (c) grid voltage (150 V/div) and grid current (2 A/div); traces top to bottom.

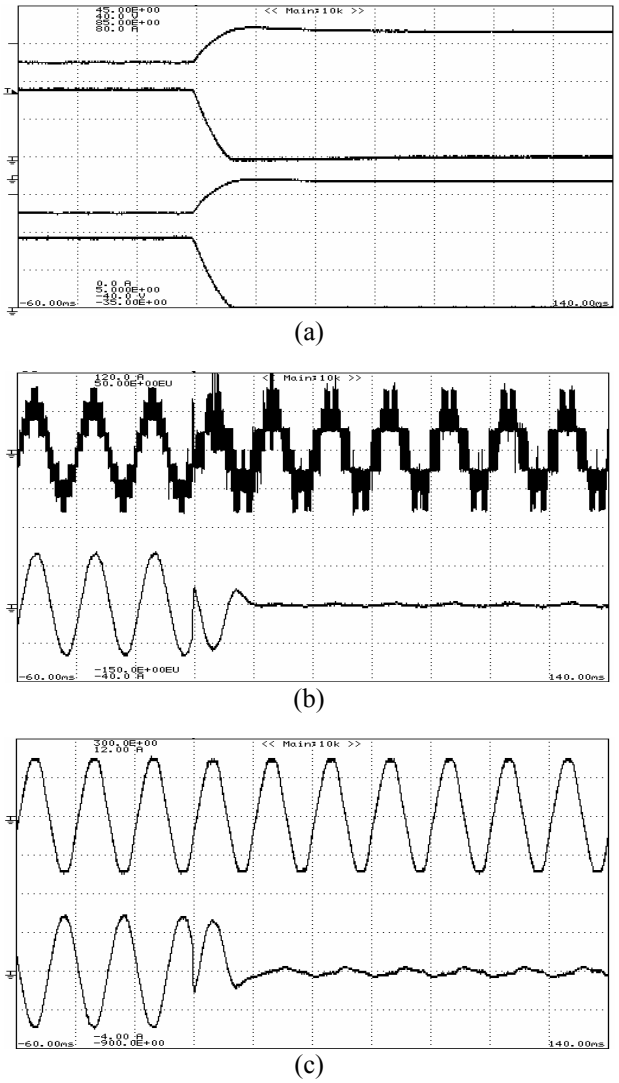


Fig. 22. Step change of V_{dc}^* from 30 V to 38 V, time scale 20 ms/div: (a) dc voltage (10 V/div, 35 V offset) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) converter ac voltage (25 V/div) and converter ac current (20 A/div). (c) grid voltage (150 V/div) and grid current (2 A/div); top and bottom traces.

5.5. Summary

This chapter introduces dual inverter grid-connected application, which has not been proposed yet in the literature. The first proposed scheme is simple but contains higher nonlinearity and cannot provide both generation and recharging in a continuous manner. The second scheme removes the stated drawbacks, but is slightly more complex.

A novel regulation scheme for the grid connection of a dual inverter system has been analyzed and tested. The proposed conversion topology includes two insulated dc supplies and a three-phase open-end winding transformer. The resulting output ac voltages have a multilevel waveform, equivalent to that of a 3-level inverter, with a reduced ac current ripple. Furthermore, the energy generation is provided to the grid with a power factor that approaches unity and additional active filter tasks could be readily introduced. For the generation of the proper

multilevel waveforms, a SVM algorithm introduced in chapter 4 has been adopted, having the merit to be easily implemented in industrial DSP controllers without the need of additional hardware (e.g. FPGA). The two inverters directly perform the regulation of the two PV string voltages by means of a novel control scheme. For the maximization of the solar energy conversion, an original MPPT algorithm has been proposed, based on the comparison of the operating points of the two PV strings.

Presented theoretical analysis has been implemented and fully experimentally verified. In particular, the subsystems (the voltage regulation, current control, grid synchronization) have been separately tested, to provide tuning for the optimal performance. The resulting settling time in response to dc voltage transients is in the order of tens of ms, suitable for realistic environmental changes of solar irradiance and/or temperature of PV cells.

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6. PV generation with dual inverter

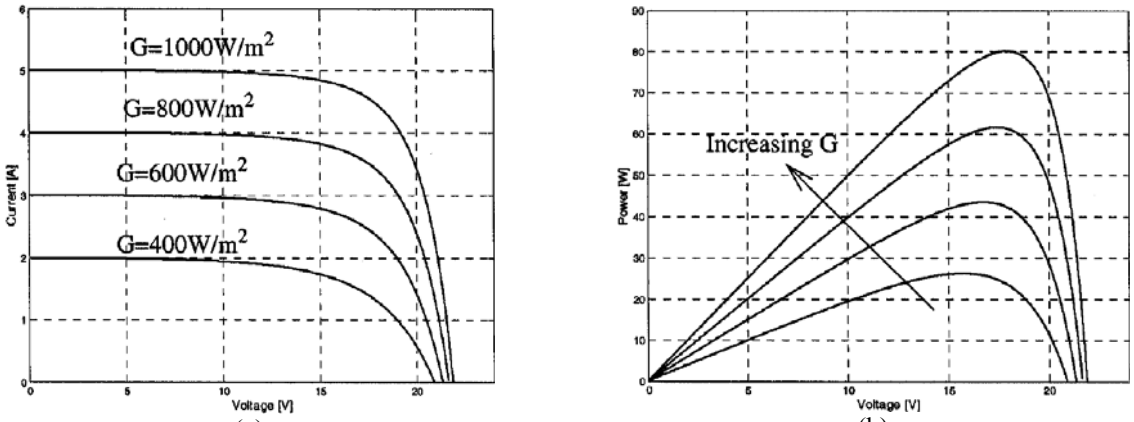
Photovoltaic production has been doubling every two years since 2002, making it the world's fastest-growing energy technology. Net metering and financial incentives, such as preferential feed-in tariffs for solar-generated electricity; have supported solar PV installations in many countries. Grid parity, the point at which photovoltaic electricity is equal to or cheaper than grid power, is achieved first in areas with abundant sun and high costs for electricity such as in California and Japan. Grid parity has been reached in Hawaii and other islands that otherwise use fossil fuel (diesel fuel) to produce electricity, and most of the US is expected to reach grid parity by 2015. In this chapter, photovoltaic (PV) panels will be described, as a source of dc voltage used in experiment. A broader insight will be given on the relatively new topic, however keeping the key point from the electric source point of view. Mass introduction of the inherently uncontrollable photovoltaic sources induced a completely new group of problem previously unknown in power engineering. The intermittent nature of renewable resources and often harsh operating environments makes the design of power electronics for these systems quite challenging.

6.1. Photovoltaic field

6.1.1. Panel ratings

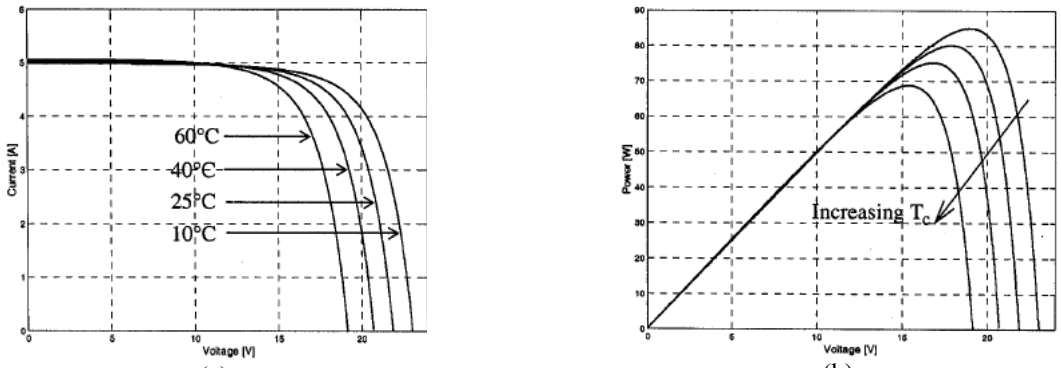
The dependence from the illumination discussed in section 1.2 is shown additionally in Fig. 1. However, from (1.3) yields also an important dependence of the I-V characteristic from the cell temperature (T): increase of the temperature affects (1.4) directly by T, but also by I_o. The net effect is the reduction of the open-circuit voltage V_{oc} almost linearly with increasing temperature. Since the band gap energy decreases with rising temperature, more photons have enough energy to create electron-hole pairs. As a consequence of increasing minority carrier diffusion, the short-circuit current is observed to increase slightly. In total, the increase of the temperature has detrimental effect on the power, as can be seen in Fig. 2. For this reason, hot climate areas might not necessarily be the best for the PV generation, with the surface cell temperatures reaching as high as 125°C in hot deserts [1].

PV modules are rated at a set of conditions known as Standard Test Conditions (STC), which specifies a cell temperature of 25 °C and an irradiance of 1000 W/m2 with an AM1.5 spectrum. These conditions are artificial, since the steady state would require full sunshine at air temperature around 0 °C, so they are obtained only in production, where PV modules are tested in a chamber known as a flash simulator. This device contains a flash bulb and filter designed to mimic sunlight as closely as possible (with accuracy around 3 %). Because the flash takes place



(a) (b)

Fig. 1. Influence of the irradiance (G) at constant temperature (a) I-V characteristic, (b) P-V characteristic.



(a) (b)

Fig. 2. Influence of the temperature (T_c) at constant irradiance (a) I-V characteristic, (b) P-V characteristic.

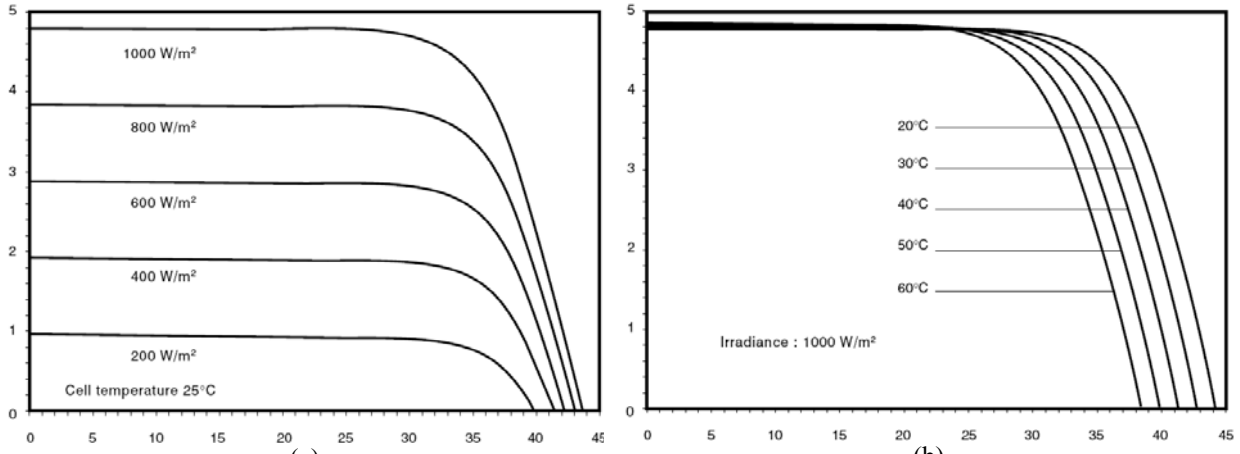
in only 50 milliseconds, the cells do not heat up appreciably. For example, *SP150* has power 150 W provided STC, which is called "rated power", but a more appropriate term is “peak power”, sometimes denoted in watt-peak (W_p) to be distinguished. Since its surface area is around 1.125 m^2 it would mean 13.3% efficiency.

Cell temperature is always significantly higher than ambient temperature due to the irradiation. As an illustration, brief measurements carried by the author shown that in a sunny early-spring day with T_a = 17 °C cell temperature is $T_c \approx 41$ °C. Similarly on a sunny summer day with T_a = 34 °C cell temperature is $T_c \approx 62$ °C. In order to have more realistic ratings, a parameter called Nominal Operating Cell Temperature (NOCT) is introduced by manufacturers. It establishes conditions of ambient temperature 20 °C with wind 1 m/s, and irradiance of 800 W/m^2 with air mass 1.5 (AM1.5) spectrum. Typical values for NOCT are between 42 and 46 °C [2]. In general case cell temperature T_c, can be estimated from the ambient temperature T_a [°C], and the irradiance E [W/m^2] with the use of NOCT:

$$T_c = T_a + \frac{NOCT - 20}{800} E \tag{1}$$

where NOCT is obtained in °C. For example *SP150* has NOCT 45 °C with P_{MPP} = 109 W and V_{oc} = 39.9 V. The characteristics of the module under different irradiance and temperature are depicted in Fig. 3.

A simple and reliable method to measure the I-V curve in actual working conditions is the introduction of a small test-circuit. The circuit contains



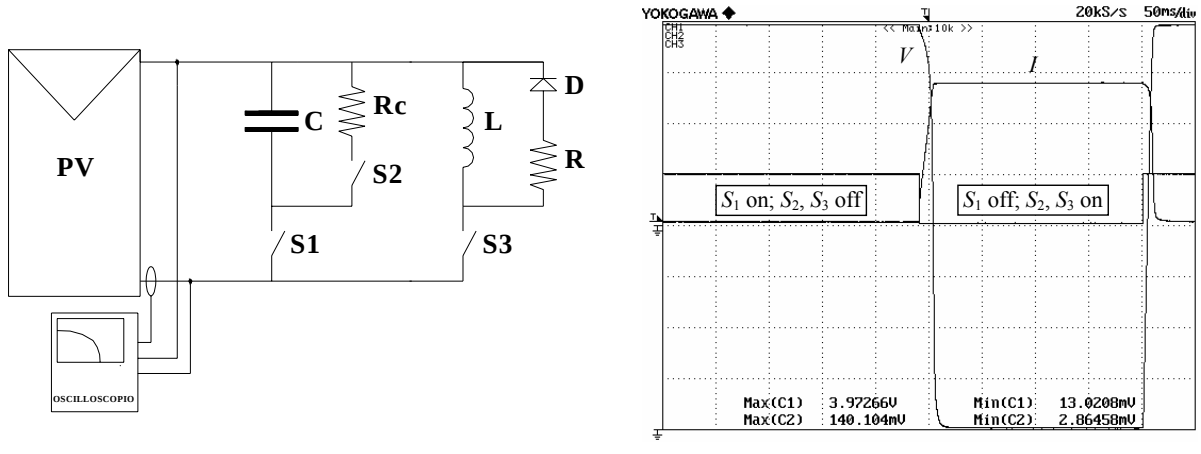
(a) (b)

Fig. 3. *SP150* module I-V characteristics for constant (a) cell temperature (b) irradiance.

- Energy storage elements (capacitors or reactors),
- Dissipative elements (resistors) for resetting the storage elements,
- Controllable silicon switches (transistors or mosfets) to switch on/off current/voltage path for the elements.

An example of the circuit is given in Fig. 4(a), with two storage elements, two dissipative and three controllable switches (mosfets). A diode D serves as a flywheel diode for the reactor L. Switches are commanded in on/off states with 50 % duty cycle, as depicted in Fig. 4(b), in such way that the same signal comes to S_2 and S_3, but opposite to S_1. In the first half-cycle, when S_1 is on, module current starts from short-circuit value to charge the capacitor C, towards the open-circuit zero current in steady state. Then S_1 goes off, and S_3 turn on, providing module current path through the reactor, while S_2 discharges capacitor through the resistor R_c. After this half-cycle the first one repeats: S_1 goes on providing current path for charging capacitor, while diode D demagnetizes reactor. The obtained dynamic characteristic is shown in Fig. 5.

The circuit requires switching elements that can withstand both PV module current and voltage ratings, but the passive elements can be chosen small, because they are not to withstand the maximum PV module power, but only the transient. By choosing small values for capacitance and inductance and increasing the switching period, smaller power ratings for



(a) (b)

Fig. 4. Test-circuit (a) layout, (b) command signals and obtained voltage and current waveforms.

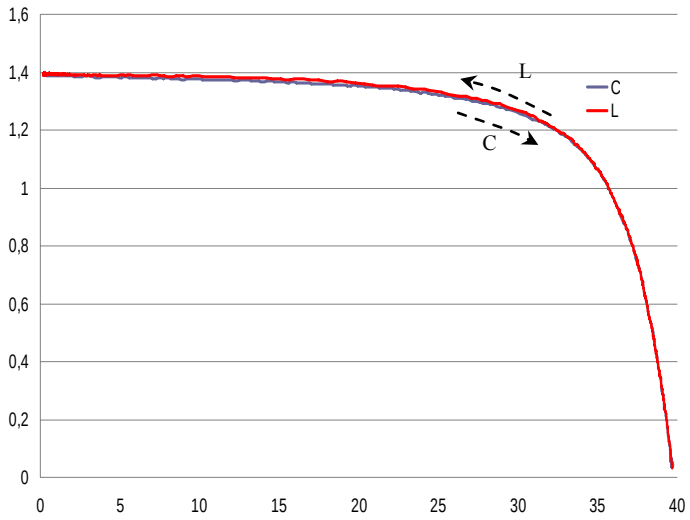


Fig. 5. I-V characteristic obtained by the test-circuit.

resistances can be obtained. However, a tradeoff must be made between to small storage values, when transient becomes too fast and parasitic effects come more influent. The goal is to obtain static characteristic, since the changes in grid-connected application are with slow dynamic.

The described method enables the experimental extraction of the I-V characteristic and its implementation in *MATLAB-Simulink* environment to obtain numerical results of the whole PV generation system. In this way, the system model parameters are based on the real laboratory prototype used for the experimental tests. The electrical model of PV string was obtained by fitting the I-V characteristic of a *Solar Shell SP150* module, including connection cables from the roof to the lab. In order to model parallel arrangement of six, the current was simply multiplied by six. The lookup table *Simulink* block computes an approximation to characteristic I-V from given data vectors I and V by interpolation-extrapolation method. Therefore, the I-V and P-V characteristics of the PV modules, given in the work, are related to the environmental condition during the experimental test in terms of solar irradiance and temperature of the module.

6.1.2. Series/parallel connection of the modules

As all the other elements of electrical circuits, PV modules/panels/arrays can be connected in series and parallel connection, forming a PV field. The configuration of the modules is optimized on the basis of the output power and chosen converter type. The main issue of interest is the circuit behavior in the following cases:

- Partial shadowing with following voltage and current decrease,
- An inverse current flow when module is poorly illuminated (night, cloudy day, partial shadow). The current sense is towards the module.

Cells electrical output is extremely sensitive to shading. When even a small portion of a cell, module, or array is shaded while the remainder is in sunlight, the output falls dramatically due to the electrons reversing course through the shaded portion of the P-N junction. In order words, its characteristic becomes closer to ordinary diode, finding itself reversely polarized in the string, as already explained in Section 1.2. Therefore, it is extremely important that a PV installation be not shaded at all by vegetation or architectural features. Similarly, when active load (e.g. batter-

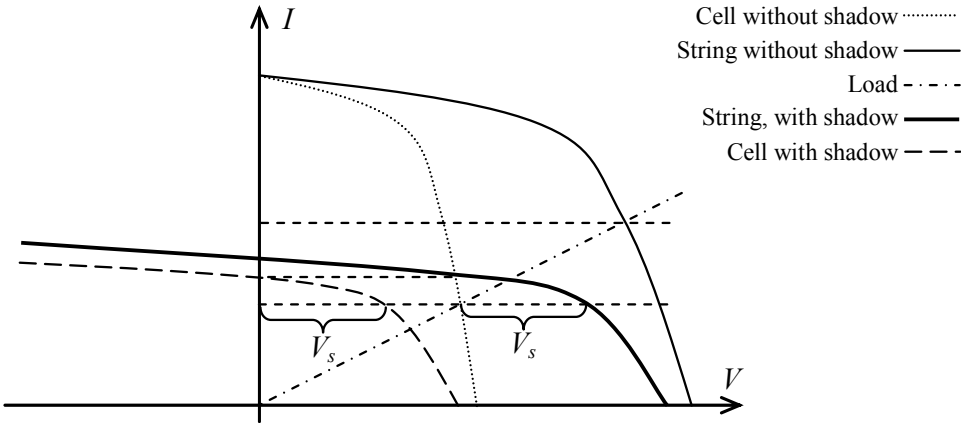


Fig. 6. I-V curves for string with one shadowed cell and (a) two cells, (b) large number of cells in total.

ies, motor in breaking mode or grid) voltage exceeds the panel voltage it tends to change the direction of the current, so cell's diode structure does not oppose since they are directly polarized. These two situations are very important for the PV application and require further analysis.

The simplest case of partial shadowing can be analyzed if only two cells are connected in series (extreme example of low number of cells connected), shadowed cell might be (or not) reverse-biased, depending on the load. The graphical illustration is shown in Fig. 6. The cells are sharing the same current that can be so high for the shadowed cell that it requires its inverse polarization. When even one cell is even partially covered, short-circuit current is drastically reduced limiting the current of the whole panel at the same amount. However, the shadowed cell still contributes with positive voltage V_s, and its maximum negative voltage cannot exceed V_{oc} of the non-shadowed cell (since load requires total positive voltage). Note that both output current output and voltage are drastically reduced compared to normal state.

By increasing the number of cell in series the situation deteriorates since applied voltage on the shadowed cell becomes negative, as can be seen from Fig. 7, and the resulting negative voltage increases with the number of cells in series n_c. Although the maximum negative voltage applied to the shadowed cell is always less than $(n\text{-}1)V_{oc}$, this limit is very high and eventually can approach to cell breakdown voltage V_{br}, which is typically around 15-20 V. Typical behavior of the cells in reverse-bias region are shown in Fig. 8. Although current is lower than for unshaded condition, due to the increased (negative) voltage the power of the shadowed cell can

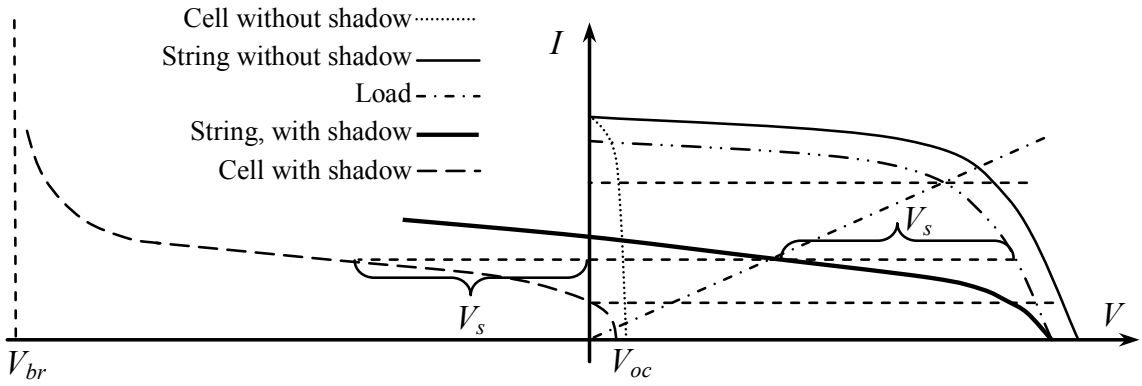


Fig. 7. I-V curves for string with one shadowed cell and (a) two cells, (b) large number of cells in total.

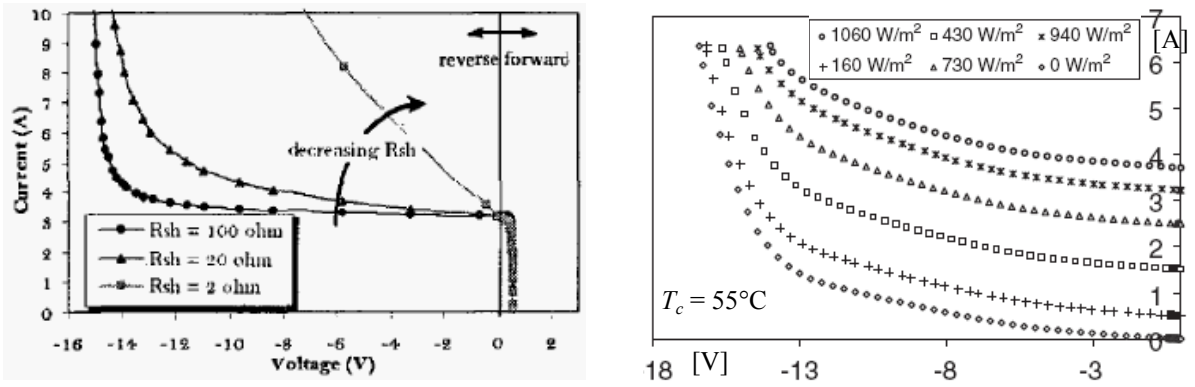
exceed tens of times its maximum value, leading to heating and possible destruction of the cell. This behavior in the reverse-bias region is called “hot-spot” [3], [4].

The conclusion is that possible number of cells n_c in series is determined by cell forward (threshold) voltage V_{th} and cell reverse breakdown voltage V_{br}

$$V_{br} = n_c \cdot V_{th} . \tag{2}$$

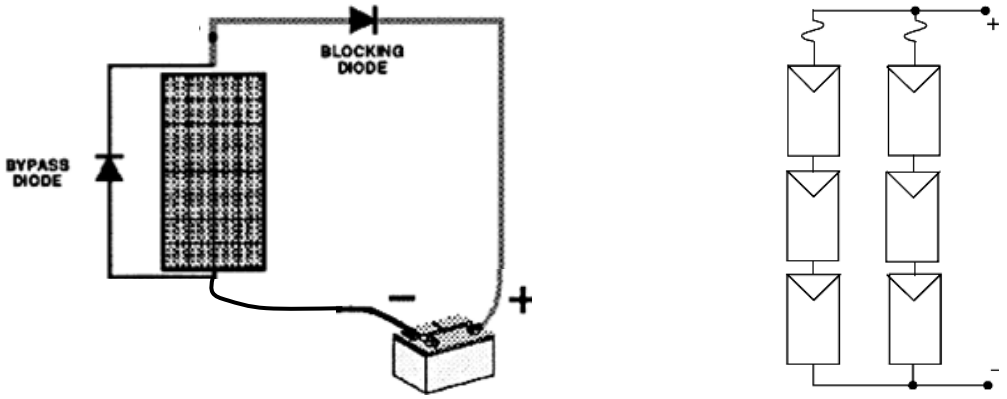
Adopting typical values V_{th} = 0.6 V and V_{br} = 18 V leads to n_c = 30. Since in grid-connected applications number of diodes in string in order to reach 600 V dc can be around 1300, the application of so-called bypass diode connected in anti-parallel is absolutely necessary, however bypassing of every cell by additional diode is both impractical and unnecessary. This diode is “clamped” to each group with defined number of cells in series to limit its reverse voltage in case of shadowing to diode threshold voltage V_{th}. Individual modules will normally have several internally connected bypass diodes, as shown in Fig. 9(a),. For example, *SP150* panel a group consists of 36 cells [5]. Note that with application of the bypass diode higher current is available at the price of drastically reduced output voltage (compared to original).

Under nighttime conditions, when none of the cells is generating appreciable photocurrent, it is necessary to consider the module as a series connection of diodes that may be forward biased by the system storage batteries. A possible solution for the second problem is connection of the diode in series with panel (called a blocking diode) to prevent current from flowing in the reverse direction, as shown in Fig. 9(a). Nevertheless, it would mean a forward voltage drop and associated power loss in order of few percents of the total module output power. Therefore, it is more efficient to use module with higher V_{oc} (having more cells in series), so the load voltage remains under threshold voltage of the diodes (even in dark condition). However adding to many cells would also increase working voltage, which can be unwanted, so these two requirements need to be compromised. As an illustration the simplest system of a with 28-cell module directly connected to an ordinary 12 V lead-acid car battery system would produce 14.6 V during the day, but at night sharing 12.8 V battery voltage would mean 0.46 V of direct polarization for each diode and from V-I equation (1.3) 4.63 mA discharge current. On the other side, a 33-cell panel would share 0.39 V and just 0.32 mA (more than ten times less). Furthermore, under weak sun or high temperatures, the module output voltage could be less than the battery voltage and no charging would occur. In fact, blocking diodes are rarely used in PV systems [6].



(a) (b)

Fig. 8. Reverse bias V-I characteristics at different irradiances (a) cells, modules and arrays, (b) V-I curves.



(a) (b)

Fig. 9. PV cells connection (a) bypass and blocking diode, (b) parallel connection of the modules.

So far, only connection in series of the cells was discussed, but modules are often connected in parallel connection of Fig. 9(b). It has advantage that since shadowed cell (module) reduces output by its current contribution only, without the need of bypass diodes. However, similarly arises problem of opposite current that is a loss and can be even dangerous for the panel due forming the hot spots. In the case of many such connected modules losses are equal to the rated power multiplied by the number of the panels. Therefore application of the blocking diodes can be considered, but introducing ever present voltage drop. In this type of connection, fuses are connected in series with each series string of modules, so that if a string fails, any excess current from the remaining strings that might otherwise flow in the reverse direction through the failed string will be limited by the fuse in the failed string. For large number of the modules fuses can be considered as convenient solution, with a drawback of unnoticed "loss" of the shadowed panel after the tripping. It is possible that in reality partial shadowing does not reduce V_{oc} of the shadowed panel so drastically. For no-load conditions panels will give (small) current to the shadowed one, but since they are usually work around MPP with significant drop ($0.2V_{oc}$) shadowed panel will not be reversely biased.

6.2. Maximum power point tracking

Outside the atmosphere, the annual solar irradiation is about 12000 kWh/m² (solar constant 1367 W/m² for 8760 hours). At every site on the earth, half of the year is night, with no sunshine. The atmosphere reduces the irradiance at least by 25 %. Clouds and dust increase this reduction so that the best sites on earth, in extreme desert areas, receive an annual solar irradiation that cannot be more than 2500 kWh/m². On the other hand, there are cloudy sites at high latitudes with an annual irradiation far below 1000 kWh/m². Furthermore, at today's technology state, mass production cell conversion efficiency is 10-15 %. Additionally (usually much slower) changes are due to the dusting and aging of the cells.

Due to such limited amount of the available radiation and low conversion efficiency the maximization of both the output power and efficiency are indispensable for a PV system to be an economically justified. Main objective of research and development is thereby a drastic lowering

of the manufacturing costs and lately also a substantial increase of the efficiency. Together with an application as renewable grid-connected energy resource, a large number of maximum power point tracking algorithms has been represented.

Unlike the current of the MPP, the photovoltaic voltage of the MPP is usually bounded by 70%–82% of the open circuit voltage. This gives a lower bound and upper limit of the tracking range. Because the photovoltaic current dramatically varies with insolation, the transient response of MPP tracking can occasionally cause the photovoltaic current to saturate at the short-circuit current. This should be prevented because its nonlinear feature causes a sudden voltage drop and results in both instability and power losses.

6.2.1. Maximum power point tracking state of the art

The first terrestrial applications of the photovoltaic cells were simple standalone such are small electronic devices (pocket calculators, watches etc.) or battery charging at remote installations. The first commercial installation of this kind was in 1966 on in Japan for fully self-sufficient electrical power Lighthouse. The delivered power is determined by the load, so it can vary from two extreme cases no-load to short-circuit condition. This permits the cells ratings (voltage, power etc.) were selected based on the load and the inherent V-I characteristics of the cells (large internal resistance) made no need to introduce an additional converter to maximize the power [7]. There is a smaller market for off-grid power for remote dwellings, boats, recreational vehicles, electric cars, roadside emergency telephones, remote sensing, and cathodic protection of pipelines. The three leading countries (Germany, Japan and the US) represent nearly 89% of the total worldwide PV installed capacity.

With the penetration of the PV sources to grid generation, this issue fundamentally changes: first, it requires a dc/ac converter (inverter) and second, there is no particular demand from the load, but the goal is to maximize the power (and consequently profit). These demands lead to development and application of numerous MPP tracking algorithms. Strictly speaking, only permanent sweeping of the *V-I* characteristic can determine exact position of the MPP in every instant for all working conditions (different irradiance, shadows, and temperature). However, this mode of constant perturbation is quite unacceptable from a practical point of view, and it can be adopted just in very few cases (e.g. for low-power applications if performed in regular and not so often intervals [8]). For this reason, many “approximate” methods, today commonly accepted under name “MPPT algorithms”, have been developed.

Generally, methods can be divided in two classes, based on type of the applied loop.

1) Open loop control, using *a priori* model of the panel behavior (usually eventually updated). Basic representatives are
   - Application of pilot cells [8], serving as a model of the all included PV cells. It is very easy and cheap to implement as it does not necessarily require DSP or microcontroller control.
   - Open-circuit voltage/short-circuit current based methods [9], employing numerical methods to show a linear dependence between the “cell currents corresponding to maximum power” and the “cell-short circuit currents”

$$I_{MP} = k_i I_{SC} \tag{3}$$

with "known" current factor $k_i \approx 0.86$. It is shown that "cell voltages corresponding to maximum power" exhibit a linear dependence, independent of panel configuration, with respect to cell "open-circuit voltages" for different insolation and temperature levels, again with "determined" $k_v \approx 0.71$.

$$V_{MP} = k_v V_{OC} \tag{4}$$

- Model (parameter) based methods, e.g. small-signal model parameterization [10], or nonlinear "one cycle control" technique based on the integration of a switched variable [11].

2) Closed loop control, which compares the actual output current to the previous one in order to perform MPPT. Basic representatives are
   - "Perturb and observe" (P&O, sometimes also called "hill climbing") [12], a very simple and natural method usually uses PV power as a criteria, but it has been shown that output electric parameters of the converter can be used as well [8]. The biggest drawback is the variable operating point even under stable external conditions.
   - Incremental conductance (INC) [13], is based on the simple mathematical fact that the derivative of the power fulfils the condition

$$\frac{\mathrm{d}P}{\mathrm{d}V} = 0 \tag{5}$$

   INC and P&O are two by far most popular methods. Together with their numerous variations, they practically established themselves as industry standard due to their simplicity and ease of application.
   - Fuzzy logic and neural network [14] are still nontraditional methods more complex to implement and require field-specific tuning.
   - Sliding mode control [15], using a sliding-mode observer control technique, based on a model.
   - Ripple correlation control [16], based on the power variation at double grid frequency superimposed to the dc link voltage for a single-phase inverter Thus, dc link voltage variation is occurred. This dc link voltage variation introduces the PV current variation.
   - Load current/voltage maximization [17], which for a voltage-source type load, maximizes the load current to reach the maximum output power, and vice versa for the current-source load. The main benefit is the application of only one sensor.

6.2.2. Dual inverter photovoltaic application

Over the last two decades, there was strong trend towards high-power plants with peak power of 60 MW [18]. This relatively new application field still demands development of specific power electronic topologies and control techniques. Multilevel converters are a viable solution for this PV application, with the advantages already discussed in Chapter 1. Among numerous configurations, the dual inverter application scheme in the photovoltaic area is shown in Fig. 10. Another important benefit in some applications (e.g. battery supply) is a halved nominal voltage, lowering insulation requirement, and the possibility to split easily available panels into two

groups to provide two isolated dc sources. The PV conversion system considered here is based on a symmetric structure, having two inverters with the same voltage and current ratings, and supplied by two equal strings of PV panels. The *V-I* characteristic of a PV string continuously moves due to the environmental changes, and the operating point should be kept close to the MPP to optimize the conversion efficiency.

With reference to the PV generation system shown in Fig. 10, two relevant configurations should be taken into account:

1) If the conversion scheme includes intermediate dc/dc choppers for the MPPT regulation (dashed blocks in Fig. 10), each of the two PV strings can operate close to its own MPP. In this way both the dc inverter voltages V_H and V_L can be set to a fixed optimal value, V_{dc}^*, determined on the basis of both the inverter/transformer design and the ac grid voltage level. The presence of a dc/dc chopper allows the PV panels to operate over a wider voltage range, with a fixed inverter dc voltage and a simplified system design. On the other hand, the dc/dc chopper increases the cost and decreases the conversion efficiency at most operating points.
2) In the case of a direct connection between inverters and PV strings, $V_H = V_{PH}$ and $V_L = V_{PL}$, the MPPT action must be performed by inverters, and the dc inverter voltages continuously change. Since the PV strings are supposed to be equal, being originated by a single PV field divided in two identical parts, a single MPPT regulation can be considered, as in the case of a single PV field. This solution is adopted here, excluding an intermediate include intermediate dc/dc chopper.

The connection of PV fields to the ac grid is made with a voltage source inverter (VSI), and it may, transformer, or even both. In many countries, the national electric standards require a transformer to achieve galvanic insulation of panels with respect to the grid [19]. Transformerless and high-frequency transformer topologies are preferred for avoiding bulky low-frequency (LF) transformer, but are usually limited to single-phase connections with powers up to few kilowatts. Hence, PV conversion schemes including a line-frequency transformer prevails in high-power, three-phase systems, ranging from few tens of kilowatts up to megawatts. The presence of a LF transformer enables voltage adaptation, allowing the direct connection of high power generation systems to either low- or medium-voltage grids (10 kV or more).

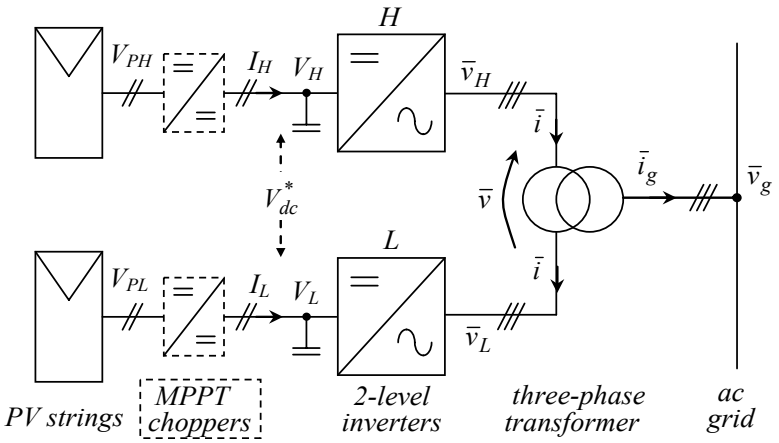


Fig. 10. Proposed dual-inverter configuration for the PV generation system.

The dual inverter has been proposed by the author in [20] as a novel topology for PV grid-connected systems, and it is further developed by introducing a corresponding control system. The converter is connected to the grid by the open-end primary windings of a standard three-phase transformer. The whole PV field is arranged in two symmetric PV strings, which are supplying separately two inverters, as shown in Fig. 10. The secondary winding of the transformer can be connected to the grid either with star or delta configuration. Note that the transformer contributes with its leakage inductance to the ac-link inductance, which serves as both grid interface, and filter.

Besides the presence of the converter, another important feature for PV plants is provision of maximum output power. A considerable number of techniques have been developed to suit different applications depending also on the topology and the rated power, as previously stated. The dual VSI topology [20] is considered, shown in Fig. 10, and a novel MPPT algorithm has been applied to maximize power injection into the grid. A renewed control scheme including simple proportional-integral (PI) controllers is proposed to achieve the commanded value of dc voltages necessary for MPPT of PV strings. A suitable SVM strategy described in Chapter 4 has been implemented to provide proper multilevel waveform and simple implementation in industrial digital signal processors (DSP). Besides power generation, the system can operate as an active power filter, with features such as load balancing, harmonics compensation and reactive power injection.

As previously stated, the proposed algorithm is based on the assumption that the two PV strings have the same *P-V* (or *I-V*) characteristic. Hence, PV strings should consist of equal-number and same-type of PV modules. In spite of the small difference between the *P-V* characteristics of two identical PV modules (the dispersion is in the order of few %), when many PV modules are arranged in two big strings their global P-V characteristics are averaged and practically coincides. The partial shadowing problem is much more critical at lower power applications, such as portable chargers, where even a small shadowed area drastically reduced relative output power. There are two reasons why high-power installations less sensitive to partial shadowing problem [21]:

- The plants are purposely built without possible obstructions, thus the shadowing occurs less often.
- Even in the case of the shadowing, the covered area represents a small part of the total power, except during brief transients such are clouds movements.

Regarding the current control method described in 6.1.1, it should be noted that for operating point close to no load, when I_H^*, $I_L^* \approx 0$ the expression (6.6) tends to be undefined. In this condition small difference between two PV arrays leads to power sharing coefficient k very different from 0.5 (e.g 0.6-0.7). However, this problem is rather of theoretical interest, since grid-connected application always tends to work around maximum power point. As load current augments this ratio becomes closer to 0.5, as can be seen from V-I characteristic.

6.2.3. Proposed maximum power point tracking algorithm

The proposed MPPT algorithm is based on a forced small displacement in the working points of the two PV strings, allowing sharing of data between them based on instantaneous currents

measurement. Similar MPPT schemes have been recently presented in [22] and [23], but with reference to different PV conversion structures. This algorithm is suitable for the dual inverter configuration, due to the presence of two identical strings of PV modules.

In particular, the small voltage difference ΔV^* between reference voltages of the two PV fields V_H^* and V_L^* is on the order of few %, and it can be introduced as follows

$$\begin{cases} V_L^* = K_v V_H^* \\ \Delta V^* = V_H^* - V_L^* = (1 - K_v) V_H^* \end{cases} \tag{6}$$

where the coefficient K_v slightly differs from 1 ($k \cong 0.95 \div 0.98$). Due to the particular shape of power vs. voltage characteristic (P-V curve), the powers generated by the two PV fields, P_L and P_H, practically coincide if the operating points are on the "flat" neighborhood of MPP. Conversely, on "sloped" parts of the P-V curve, one of the powers is higher than the other, or vice-versa, depending on the position of the operating points with respect to the MPP, according to the diagram of Fig. 11(a). In particular, the following three possibilities occur:

$$\begin{cases} P_L < P_H & \Rightarrow \quad V < V_{MPP} \\ P_L = P_H & \Rightarrow \quad V \cong V_{MPP} \\ P_L > P_H & \Rightarrow \quad V > V_{MPP} \end{cases} \tag{7}$$

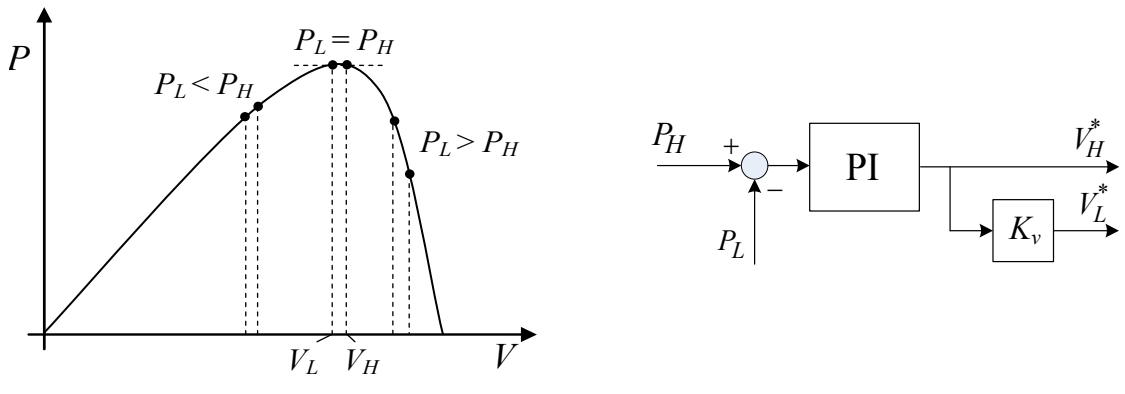
Actually, the difference between P_H and P_L gives an estimation of the slope of the P-V characteristic:

$$\frac{dP}{dV} \cong \frac{P_H - P_L}{(1 - K_v) V_H} \cong K_p (P_H - P_L) \tag{8}$$

Hence, reference dc voltages V_H^* and V_L^* can be found as the output of a simple PI-controller acting on the error between the two powers, as represented in Fig. 11(b). The choice of a proper value for K_v is a tradeoff between efficiency, which is higher as K_v approaches 1, and immunity to both noise and PV modules asymmetry, which increase as K_v diverge from 1.

On the basis of (5.14), the effects of PI regulators Σ and Δ lead to the following steady-state conditions

$$V_\Sigma = 0 \quad \Rightarrow \quad V_H + V_L = V_H^* + V_L^* \tag{9}$$



(a) (b)

Fig. 11. Principle of proposed MPPT algorithm (a) P-V diagram, (b) control scheme.

$$V_{\Delta} = 0 \;\Rightarrow\; V_H - V_L = \Delta V^* \tag{10}$$

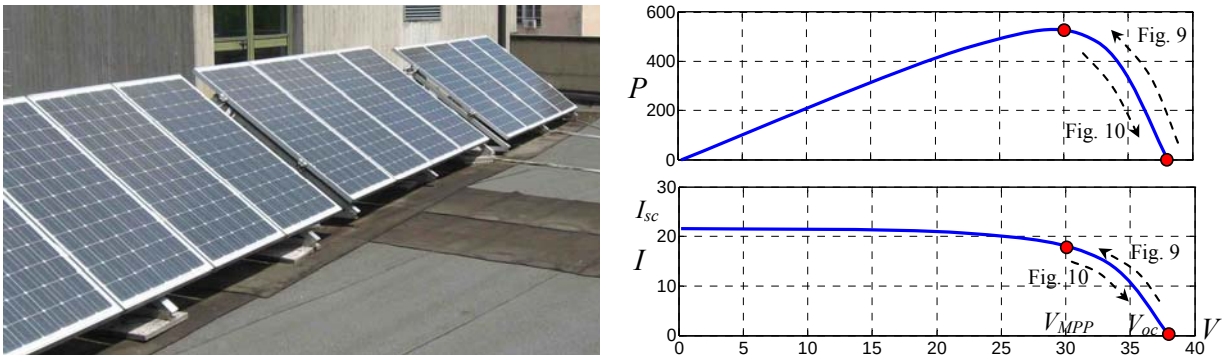
As previously stated, the proposed algorithm is based on the assumption that the two PV strings have the same *P-V* (or *I-V*) characteristic. Hence, PV strings should consist of equal-number and same-type of PV modules. In spite of the small difference between the *P-V* characteristics of two identical PV modules (the dispersion is in the order of few %), when many PV modules are arranged in two big strings their global P-V characteristics are averaged and practically coincides. Usually high-power installations are purposely built without possible obstructions, thus avoiding partial shadowing problem [21].

6.3. Experimental results

A complete PV generation system based on the proposed multilevel converter has been implemented in a prototype. The main characteristics of the PV array are summarized in Tab. 1, whereas the other system components have been already described in the previous chapters. The system layout is based on two strings of six parallel-connected PV modules and a grid-transformer with the proper turn ratio enables voltage adaptation. The resulting PV string voltage is around 30-40 V, allowing the use of low-voltage, high-current MOSFETs. These types of static switches are cheap and have good efficiency, since their on-state resistance is a strong decreasing function of the blocking voltage rating (V_{DSS}). Furthermore, low operating voltages guarantee the electric safety during experiments. Fig. 12(a) shows the twelve "*Solar Shell*" SP150 PV modules (in parallel arrangement of six) used for tests. The I-V and P-V characteristics of the PV modules, given in Fig. 12(b), are related to the environmental condition during the experimental test in terms of solar irradiance and temperature of the module. The control algorithm presented

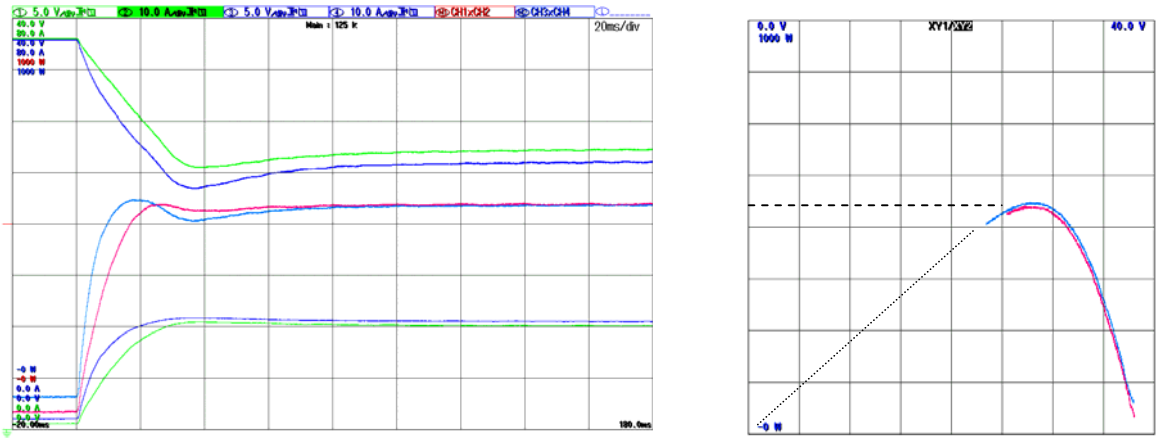
Tab. 1. The main parameters of the PV conversion system.

PV Panels	
type	Shell Solar SQ150-C
string arrangement (H and L)	6 panels in parallel
connection cable resistance (roof to Lab)	43 [mΩ]



(a) (b)

Fig. 12. PV panels utilized for tests. (a) Picture of the arrangement on the roof, (b) V-I and V-P characteristics of the two PV strings (I_{rr} = 750 W/m2, T_c= 35 °C). Dots represent the operating test points.

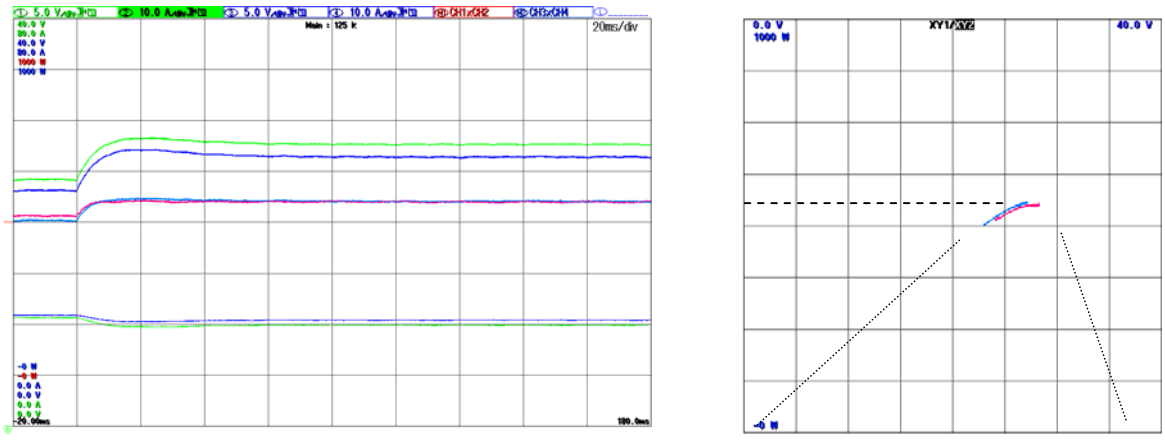


(a) (b)

Fig. 13. Experimental results (I_{rr} = 800 W/m2, T_c = 40 °C): transient from no-load to MPP with K_v = 0.96. (a) top: V_H, V_L (5 V/div), middle: P_L, P_H (125 W/div), bottom: I_L, I_H (10 A/div). (b) top: P_L vs. V_L, bottom: P_H vs. V_H (5 V/div, 125 W/div).

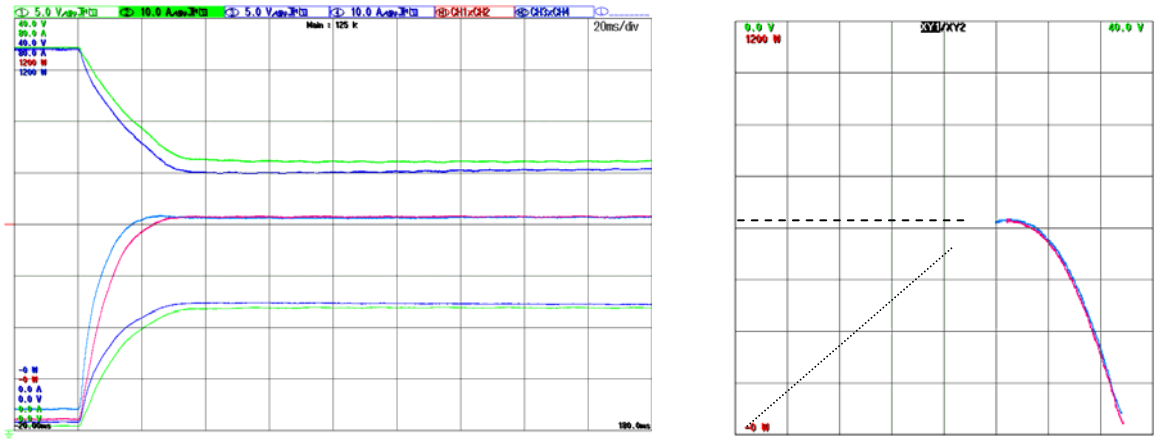
in Chapter 6 has been implemented in a TMS320F2812 DSP capable of controlling two three-phase inverters simultaneously. Reference is made to the scheme of Fig. 12 with the two PV arrays directly connected to the VSIs, without intermediate dc/dc choppers. In this case, the MPPT regulation is achieved by adjusting the dc voltage reference for both the inverters.

The operation of the MPPT controller with reference to opposite starting conditions and with different values of the MPPT parameters (K_v and PI-controller) is shown in this section. Figures 13 and 14 are related to the case of a coefficient K_v = 0.96, leading to a difference between V_H and V_L of about 1 V. In particular, Fig. 13(a) shows the time behavior of dc voltage, dc current, and power for both the inverters starting from the open-circuit voltage (around 38 V) to the MPP, whereas Fig. 13(b) shows the same transient on the corresponding P-V diagram. It can be noted that steady state is reached in about 100 ms, with a smoothed oscillation around the MPP. The same variables are presented in Fig. 14 with reference to a transient from the minimum dc voltage (around 24 V) to the MPP. In this case, the voltage excursion is lower, and the settling time is halved (about 50 ms), without oscillations.



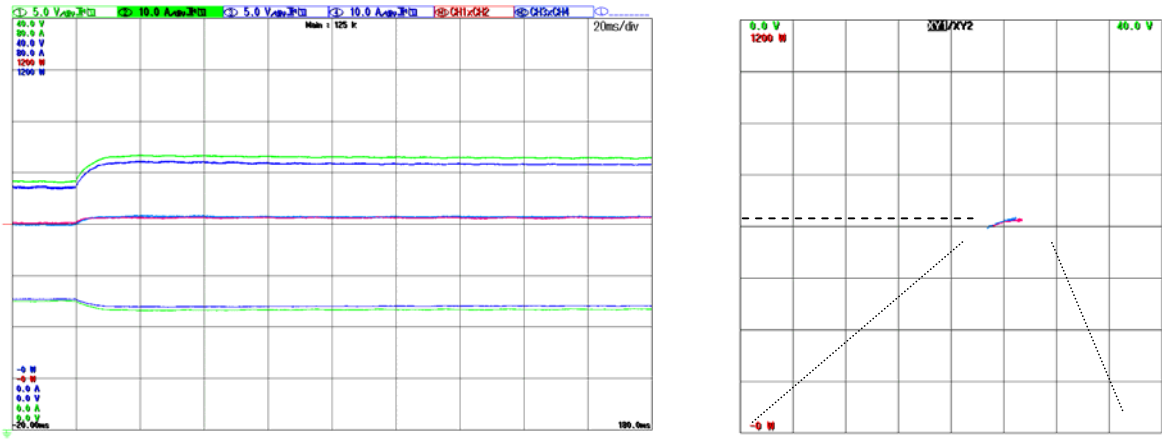
(a) (b)

Fig. 14. Experimental results (I_{rr} = 800 W/m2, T_c = 40 °C): transient from minimum dc voltage to MPP with Kv = 0.96. (a) Top: VH, VL (5 V/div), middle: PH, PL (125 W/div), bottom: IL, IH (10 A/div). (b) Top: PL vs. VL, bottom: PH vs. VH (5 V/div, 125 W/div).



(a) (b)

Fig. 15. Experimental results (I_{rr} = 900 W/m2, T_c= 50 °C): transient from no-load to MPP with K_v = 0.98. (a) Top: V_H, V_L (5 V/div), middle: P_L, P_H (150 W/div), bottom: I_L, I_H (10 A/div). (b) Top: P_L vs. V_L, bottom: P_H vs. V_H (5 V/div, 150 W/div).



(c) (d)

Fig. 16. Experimental results (I_{rr} = 900 W/m2, T_c= 50 °C): transient from no-load to MPP with Kv = 0.98. (a) Top: V_H, V_L (5 V/div), middle: P_L, P_H (150 W/div), bottom: I_L, I_H (10 A/div). (b) Top: P_L vs. V_L, bottom: P_H vs. V_H (5 V/div, 150 W/div).

Figs. 15 and 16 are related to the case of a coefficient K_v = 0.98, leading to a reduced difference between V_H and V_L (about 0.5 V). Also in this case, the former diagrams, Fig. 15, show the transient to the MPP starting from the open-circuit voltage, whereas the latter diagrams, Fig. 16, show the transient to the MPP starting form the minimum dc voltage. Steady-states and settling times are very close to the previous case with K_v = 0.96, proving that also with a very small voltage displacement a satisfactory behavior of the MPPT algorithm can be obtained. Figs. 13 and 14 correspond to the same cases shown in Figs. 13 and 14, respectively. In particular, Fig. 15 shows that, despite of the large voltage excursion between open-circuit and MPP, the steady-state condition is reached without oscillations in about 40 ms. Note that, in all the examined cases, both the steady-state powers P_H and P_L practically coincide with the MPP, proving the effectiveness of the proposed MPPT algorithm.

6.4. Summary

A novel regulation scheme for the grid connection of a photovoltaic generation system has been analyzed and tested. The proposed conversion topology includes two insulated PV strings and a three-phase open-end winding transformer connected through dual three-phase inverter. Furthermore, the energy generation is provided to the grid with a power factor that approaches unity and additional active filter tasks could be readily introduced. For the generation of the proper multilevel waveforms, a modified SVM algorithm has been adopted, with the power sharing feature. The two inverters directly perform the regulation of the two PV string voltages by means of a novel control scheme. For the maximization of the solar energy conversion, an original MPPT algorithm has been proposed, based on the comparison of the operating points of the two PV strings.

The whole PV generation system has been implemented and experimentally verified. In particular, the voltage regulation scheme and the MPPT algorithm have been separately tested, to emphasize the system behavior both in steady-state and transient conditions. The resulting settling time in response to PV voltage transients is in the order of tens of ms, suitable for realistic environmental changes of solar irradiance and/or temperature of PV cells.

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7. Conclusion and future work

7.1. Conclusion

This thesis deals with dual two-level inverter in grid-connected and photovoltaic applications. A huge interest was raised in recent times in these areas and numerous aspects of these three different yet connected structures have been analyzed, with large number of proposed solutions. However, within inverters dual two-level inverter remained on a boundary between standard two-level inverter and typical multilevel converters. For example, few pulse width modulation (PWM) schemes have been developed for this inverter, utilizing both carrier-based PWM and space vector PWM (SVPWM) approaches. However, no systematic analysis has been performed in order to determine basic properties of multi-phase PWM in general, and to establish close correlation between carrier-based PWM and space vector PWM, for dual VSIs.

Important part of the each converter is set of available PWM techniques. The analysis, development, implementation and experimental verification of various PWM techniques for dual two-level inverter were undertaken. Both carrier-based PWM and space vector PWM approaches, restricted to modulation in the linear region, are considered. All these methods are aimed at multilevel output voltage generation applicable in high-power converters. In particular, new algorithms based on the discontinuous modulation are proposed, illustrating the modularity of the dual inverter that originates from standard two-level inverter. These methods provide proper multilevel waveform without simultaneous commutations and in a relatively simple manner, easily applicable to standard DSP PWM units. A number of degrees of freedom, offered by dual inverter configuration, allow both development of the proper modulation schemes and flexible control of the system achieving also management of the sources such are asymmetrical loading, power balancing etc. The necessity of such feature arises in non-grid supplied systems, where the modulator becomes a part of the voltage control system.

A similar kind of balanced output voltage is necessary if power balancing is desired because of the source asymmetry that can be both inherent or due to the variable conditions. In addition, characterization of modulation methods is performed regarding the voltage limits. Based on the literature survey, presented in Chapter 3, a lack of systematic analysis and development in the area of PWM methods for dual VSIs is evident. While dual inverter topology has been known for twenty years, an increased rate of development is evident during the last three-five years. This is primarily driven by the search for new solutions in high-power areas where two-level inverters do not represent a satisfactory solution. Thus, for example, in high power applications, where limited power ratings of the currently available power semiconductors are an obstacle, ability of the multilevel converters to apply the higher number of voltage levels over the increased number of the switches represents a decisive advantage. This concept represents a counterpart of the multiphase approach, where the increased power capability is achieved at the same voltage rating

by increasing the number of current paths. Similar applies to the fault tolerant applications where multilevel and multiphase converters are considered as a viable solution.

Yet, whether the application is grid-supplied or not, a PWM scheme with appropriate multilevel waveform is a necessary part of the control system. For development of such PWM schemes, properties of the dual inverter need to be considered carefully, since these are different from the well-established industrial two-level three-phase inverters, as well as from “standard” types of multilevel converters (diode-clamped, flying capacitor). Modeling of the dual VSIs, presented in chapter 3, was based on the general concepts that are also applicable to two-level VSIs. However, space vector representation of a dual two-level VSI needs to take into account existence of seven such two-level hexagons, located in center (one) and vertices (six) of single two-level vector plot. An advantage, obtained by using the vector space decomposition, is a clear dissection of the vector mapping into different triangular sections, which is of paramount importance during the synthesis of the SVPWM strategies. Furthermore, this can be generalized to dual inverters with more levels. However, it should be noted that dual inverter structure becomes attractive for lower number of constituting voltage levels, where it still holds both benefits from its constituting units and their established connection.

The multilevel PWM schemes, analyzed in the thesis in conjunction with optimum voltage utilization, are all aimed at dual inverters with separate dc sources, in which case power balancing of two inverters is necessary. To achieve this, output voltage must be synthesized as a sum of two collinear vectors (in an averaged sense), which is a demanding task for proper multilevel modulation. It is also shown that simple extension of the standard three-phase SVPWM (with symmetrical placement of zero vectors) does not produce proper output waveform. In Chapter 4, four different approaches have been adopted:

- composition of switching periods;
- carrier based method with discontinuous modulation;
- asymmetrical carrier method;
- space vector modulation.

These methods cover wide range of output performances, from the simplest based on carrier signals that are providing imperfect multilevel waveform to the sophisticated space vector modulation with small harmonic content and no simultaneous commutations. Yet, all the presented techniques are capable of power sharing between the two sources, a basic tool for dc voltage control. In addition, all methods are developed for the implementation in a standard DSP PWM unit.

In order to investigate practical aspects of dual topology, the developed low-voltage converter was connected to the grid by transformers. Obtained topology simulates high-power grid applications connected to medium voltage level, and either generating or power conditioning purpose. The proposed dual inverter structure provides multilevel voltage waveform reducing the demand for a bulky grid filter. An original control method for dc voltage balance in a grid-connected has been developed and tested in Chapter 6.

Finally, connecting the developed system to the PV field, a grid-connected PV generation system is obtained. Compared to standard generation system on fossil fuels it is characterized by the uncontrollability of the "generator" and wide range of the working points, which significantly complicates both design and the control tasks. Therefore, the maximum power point tracking

algorithm makes the core of any PV system. A new method has been proposed based on the dual inverter structure with double supplies. The results presented in Chapter 7 have shown fast and stable response both in static and dynamic conditions.

7.2. Future work

The material presented in this thesis, although characterized by significant new knowledge, leaves large space for further research works. Since the analysis presented in the thesis has been narrowed to the single-commutation PWM schemes for DSP application, operating in the linear region of modulation, and PV generation, there are plenty of ways to continue further. Some of them are listed here as possible directions for future work:

- investigation of the operation of the dual inverter in the overmodulation range;
- development of carrier-based schemes with particular (non-common) carriers;
- detailed characterization of the harmonics and switching losses caused by application of various PWM schemes;
- investigation of possibilities for output current ripple reduction by means of different space vector selection and organization within a switching period;
- extension of the developed modulation schemes to the dual configurations with multilevel inverter itself (number of levels higher than two);
- extension of the dual three-phase inverter by modular application in multiphase multilevel drive;
- research on the impact of measurement sensitivity to MPPT algorithm and possible sensor reduction;
- investigation of the active power application of the dual inverter, possibly simultaneously with PV generation.