ALMA MATER STUDIORUM – UNIVERSITY OF BOLOGNA

DEPARTMENT OF ELECTRICAL ENGINEERING

PhD IN ELECTRICAL ENGINEERING
XXIV CYCLE

SD 09/E1 - Elettrotecnica
SSD ING-IND/31 - Elettrotecnica

Analysis and Implementation of Multiphase-Multilevel Inverter for Open-Winding Loads

by

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March 2012, Bologna, Italy

Acknowledgment

With the blessing of **My Father** and **Mother**, praise the All Mighty **GOD** for completing my PhD research work successfully. It is my utmost privilege to acknowledge many individuals who come across during my research study period with **UniBo** and might many not listed below but they will be in my heart, **'**are not just the words its my experience**'**.

First of all I express my heartfelt thank and sincere gratitude to my Advisor, **Prof. Gabriele Grandi**, who accepted me has his research student came from **INDIA** and provided me opportunity with the grant to work under his insight, highly skilled professional supervision. I am always thankful for his encouragement, support and priceless, immense technical knowledge shared and concepts given to me. Above all without his right direction this thesis could not be framed and all the research results obtained motivated by him and merits goes to his hand. Always I wish to get his extended collaboration for my perspective future research work.

I like to thank **Prof. Domenico Casadei**, PhD coordinator, and **Prof. Fiorenzo Filippetti**, **Prof. Angelo Tani**, for their support provided with theoretical concepts and motivated during my study period.

I like to wish and always thankful to the support provided by **Ing. Matteo Marano**, with his vast industrial experience helped me to get technical information and shared his knowledge for developing my hardware prototype model. Thank to **Ing. Marco Landini**, **Ing. Andrea Albertini**, for their support provided to my laboratory tasks.

I am extremely thankful to **Dr. Michele Buratin**, Secretary and staff members of the department administrative office, for their priority with care during my official requirements.

I like to wish the support provided by **Dr. Darko Ostojic**, my colleague and senior PhD research candidate with my Advisor, for his supportive hand during my initial settlement with the department, laboratory task, for shared his experience and knowledge.

I like to wish and thankful to **Dr. Mauricio Perez David**, **Dr. Fabio Roveda**, my friends who helped me in various stages during my stay in Italy. Also like to wish **Dr. Michele Mengoni**, **Dr. Alessio Pilati**, for their

support provided to me with laboratory task and sharing some technical information.

Its my privilege to collaborate with the Department of Electrical Engineering, University of Bologna for their standard facilities, open minded to learn recent technology and financial support provided for my research work.

Thank You One and All.

Bologna, 05-03-2012. **Padmanaban Sanjeevikumar**

Analysis and Implementation of Multiphase-Multilevel Inverter for Open-Winding Loads

(Abstract)

Research work carried out in focusing a novel multiphase-multilevel ac motor drive system much suitable for low-voltage high-current power applications. In specific, six-phase asymmetrical induction motor with open-end stator winding configuration, fed from four standard two-level three-phase voltage source inverters (VSIs). Proposed synchronous reference frame control algorithm shares the total dc source power among the 4 VSIs in each switching cycle with three degree of freedom. Precisely, first degree of freedom concerns with the current sharing between two three-phase stator windings. Based on modified multilevel space vector pulse width modulation shares the voltage between each single VSIs of two three-phase stator windings with second and third degree of freedom, having proper multilevel output waveforms.

Complete model of whole ac motor drive based on three-phase space vector decomposition approach was developed in PLECS - numerical simulation software working in MATLAB environment. Proposed synchronous reference control algorithm was framed in MATLAB with modified multilevel space vector pulse width modulator. The effectiveness of the entire ac motor drives system was tested. Simulation results are given in detail to show symmetrical and asymmetrical, power sharing conditions. Furthermore, the three degree of freedom are exploited to investigate fault tolerant capabilities in post-fault conditions. Complete set of simulation results are provided when one, two and three VSIs are faulty.

Hardware prototype model of quad-inverter was implemented with two passive three-phase open-winding loads using two TMS320F2812 DSP controllers. Developed McBSP (multi-channel buffered serial port) communication algorithm able to control the four VSIs for PWM communication and synchronization. Open-loop control scheme based on inverse three-phase decomposition approach was developed to control entire quad-inverter configuration and tested with balanced and unbalanced operating conditions with simplified PWM techniques.

Both simulation and experimental results are always in good agreement with theoretical developments.

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1. Introduction

1.1 Motivation for research

Recent research articles mostly addressing towards multiphase induction motors due to their redundant structure, and reliability with high fault tolerant capabilities. Increasing phase becomes more predominant factor to have additional degree of freedom. On another hand multilevel inverter widely replaces the conventional two-level three-phase voltage source inverter (VSI) by their performance toward lower THD and lower *dv/dt* (leakage current) stresses in output. Combing multiphase motor with multilevel inverter technologies could be good solution for low-voltage high-current application more suitable for industries. Several power conversion structures addressing towards multiphase-multilevel ac motors are proposed last decades for its reliability and performance. In this thesis work proposes a power conversion unit based on multiphase-multilevel inverter, which can be performed as multilevel converter, in particular vital optimum solution for multiphase machines with respect to cost and performances.

In this contest, significant contribution by research work contributed towards dual three-phase induction motor modeling, control aspect, and modulation techniques. But insignificant articles by research related to the power balancing with symmetrical and asymmetrical voltage and/or current contributions for six-phase asymmetrical induction motor, deliberating keeping stator winding open-end configuration. In this dissertation devoted towards the power balancing of a proposed novel multiphase-multilevel ac motor drive system and exploited the fault tolerant capabilities under different critical circumstances.

1.2 Research objectives

The main objectives of this dissertation is to study and develop a complete model of multiphase-multilevel ac motor drive system in numerical simulation software and to implement multiphase-multilevel inverter for two three-phase passive loads in open-winding configuration, as low-voltage high-current prototype hardware module using two DSP TMS320F2812 controllers.

In detail, the objectives are focused towards:

1) To develop a comprehensive model of six-phase asymmetrical induction motor with open-end stator winding configuration based on

Keywords**:** *Multilevel inverter, multiphase inverter, multiphase-multilevel ac motor, dual three-phase induction motor, multiple space vectors, multilevel svpwm, fault-tolerance.*

three-phase space vector decomposition approach in PLECS numerical simulation software working with MATLAB environment.

2) *To study intensively the characteristics of dual-inverter as multilevel converter and then to develop a multiphase-multilevel inverter configuration much suitable for the developed six-phase induction motor.*

3) *To analysis the multiphase-multilevel inverter developed in PLECS numerical simulation software with some carrier based pulse width modulation for multilevel output waveforms. Control algorithm based on inverse three-phase space vector decomposition approach in open-loop scheme.*

4) *To develop a control algorithm based on synchronous reference frame which able to control entire ac drive system and to share the total dc power with three degree of freedom in accordance to theoretical developments.*

5) *To investigate fault tolerance capabilities of whole ac drive system under different developed post-fault condition in accordance to theoretical developments.*

6) *To implement complete low-voltage high-current prototype model of multiphase-multilevel inverter for two three-phase passive loads in open-winding configuration, with two real time DSP TMS320F2812 controllers.*

7) *To frame communication medium with data cable between two DSPs using (McBSP) multi-channel buffered serial port protocol algorithm for PWM communication and synchronization between four three-phase VSIs.*

8) *To develop control algorithm based on inverse three-phase space vector decomposition approach using two DSP controllers in open-loop scheme.*

9) *To develop simplified PWM (independent and level-shifted) methods to investigate the performance of quad- inverter for its output voltages with power sharing capabilities under symmetrical/asymmetrical conditions and synchronization issues using two DSP controllers.*

1.3 Outlines and original contribution of dissertation

This thesis work divided into following major parts and original contribution to this thesis provided by chapters 4–7:

Chapter–2: "Review of multilevel inverters"

This chapter provides survey on optimal three-phase multilevel inverter technologies, starts with traditional configurations: cascaded H-bridge, diode-clamped, capacitor-clamped, hybrid and mixed version of multilevel inverters in particular their benefits and drawbacks based on literatures addressing each inverter configuration.

Proceeds to dual-inverter configuration as multilevel converter, characterized with their complete voltages output expression and applications, (*SUR*) switch utility ratios and comparison with traditional two-level and multilevel inverters, finally discussed with fault tolerance capabilities.

Chapter–3: "Review of multiphase inverters"

This chapter provides survey on optimal multiphase inverter technologies, starts with multiple space vector transformation based on three-phase space vector decomposition approach and its inverse decomposition transformations for analyzing a six-phase system.

Proceeds to detail analysis of six-phase converter both symmetrical/asymmetrical versions, also discussed other multiphase converters: five-, seven-, and nine-phase VSIs for their benefits and applications based on literatures addressing each converter configuration.

Chapter–4: "Quad-inverter based multiphase-multilevel inverter configuration"

This chapter provides original contribution of this dissertation by proposing a novel multiphase-multilevel inverter configuration for two three-phase passive loads in open-winding configuration. Further benefits, switch utility ratios, three-phase space vector representation of the proposed converter were provided.

Proceeds to detail analysis of quad-inverter, its power output expression with three degree of freedom for both symmetrical/asymmetrical power sharing conditions, control aspect in open-loop based on inverse three-phase space vector decomposition approach in specific representing the modulation indices of each single inverter's.

Finally some carrier based pulse width modulation methods are discussed theoretically and implemented for quad-inverter using numerical simulation

software to show its multilevel output waveforms. Benefits and drawbacks of each PWM were discussed with corresponding reference literatures.

Chapter–5: "Quad-inverter configuration for multiphase-multilevel AC motor drive"

This chapter provides the detailed survey on state-of-art-in research for dual three-phase asymmetrical induction motor, modeling techniques, closed loop controls schemes, advantages and applications based on literatures addressing the machine.

Further step original contribution of this dissertation by proposing a novel multiphase-multilevel based dual three-phase induction motor with open-end stator winding configuration, modeling based on three-phase space vector decomposition approach.

Proceeds to proposed synchronous reference frame closed loop algorithm with symmetrical/asymmetrical power (voltage/current) sharing and multilevel output waveform capabilities. Complete theoretical background and numerical simulation results are provided for the whole ac motor drive system.

Chapter–6: "Post-fault tolerance strategy for multiphase-multilevel AC motor drive"

This chapter provides original contribution to this dissertation by proposing some novel post-fault control strategies for the proposed multiphase-multilevel ac motor configuration after detail survey for state-of-art-in research relating to fault tolerant in ac drives from literatures.

Proceed to fault tolerant investigation under different developed post-fault operating conditions, when one, two, or three inverter failure conditions. Complete theoretical background and numerical simulation results are provided under healthy and different post-fault operating conditions.

Chapter–7: "Hardware implementation and experimental results"

This chapter provides the complete hardware implementation of proposed multiphase-multilevel inverter for two three-phase passive loads in open-winding configuration. Also provides the open-loop control scheme based on inverse three-phase space vector decomposition approach developed using two TMS320F2812 DSP controllers working under McBSP protocol for PWM communication and synchronization.

Simplified PWM techniques (independent and level-shifted multilevel modulation) are adopted towards investigation, allowing the power sharing with three degree of freedom.

Complete set of experimental results are given with reference to both symmetrical/asymmetrical conditions.

Chapter 8 - "**Conclusion and future works**"

The main conclusion of this dissertation based on numerical simulation and experimental results obtained with respect to theoretically concepts. Finally, provides few recommendations for future research work.

References

Detailed survey on articles focusing towards multilevel, dual and multiphase inverters, multiphase and multiphase-multilevel ac motor technologies.

Appendix

2. Review of Multilevel inverters

2.1 Introduction

In this chapter the state-of-the-art-in research, multilevel power converter configurations discussed based on literature survey. Several fruitful solution based on different multilevel converter structures have been proposed and contemporary research has engaged novel converter structures and unique modulation strategies. Moreover, three different major multilevel converter structures are widely reported in the most articles: cascaded H-bridge, diode clamped (neutral-clamped), and flying capacitor (capacitor-clamped) power converters. In precise multilevel converter suitable for low-voltage high-current ac power systems are also elaborated in detail. In special attention, this chapter also focused to survey the topology based on conventional two-level inverter to frame multilevel converter, should be valid for performances, cost, and keep open broad research studies to develop further multiphase-multilevel power conversion system in later version.

2.2 Structures of multilevel three-phase inverters

Presently industries acquire low-voltage high-current ac motor drives with megawatt power level utility requirements. For medium voltage grid, troublesome to connect only one power semiconductor switch directly. Resulting, multilevel power conversion structures have been introduced as an alternative solution for high power and medium voltage systems. A multilevel power conversion not only achieves high power ratings, but also usage with renewable energy sources such as photovoltaic, wind, and fuel cells incorporated easily to a multilevel power conversion system for high power applications [1-3]. In addition, many multilevel power conversions employed in universal power conditioner (UPC) [4] and ac traction drive systems [5]. Also these configurations used for recent development in flexible AC transmission system (FACTS) [4].

The concept of multilevel power conversion came to has article since from 1975 [6] and term multilevel began with the three-level converter first time by Nabae [7]. Subsequently, several multilevel converter topologies have been developed and proposed [1-14]. But however, basic concept of multilevel converter achieving higher power rating by using a series of semiconductor switches with several low voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy systems used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, voltage

Keywords**:** *Multilevel inverter, mixed and hybrid multilevel inverter, generalized multilevel inverter, dual-inverter, voltage-limited devices and high power applications.*

rating of the power semiconductor switches depends on rating of dc bus to which they are connected. The attractive benefits of multilevel converters when compared with conventional 2-level converter are briefly summarized as follows [1-3]:

- **Quality of output voltage:** Multilevel converters generate the output voltages with very low distortion, additionally reduce the *dv/dt* stresses; therefore electromagnetic compatibility (EMC) problems significantly minimized.
- **Quality of input current:** Multilevel converters draw input current with very low distortion.
- **Quality of switching frequency:** Multilevel converters can modulate with fundamental and also higher switching frequency PWM. By lower switching frequency provides lower switching loss and higher efficiency.
- **Quality of reducing common mode voltage:** Multilevel converters produce smaller common mode (CM) voltages; therefore, the stress in the bearings of a motor can be lowered. Further common-mode components could eliminate by using advanced PWM strategies proposed in [8].

Even though with all above merits, multilevel converters do possess some drawbacks in particular with greater number of power switches. Lower voltage rated switches can utilized in a multilevel converter, but each switch requires related gate driver circuit. Hence, the overall system becomes expensive with complex control. In next section, most addressed available multilevel converter structures are discussed relating to survey of optimal configuration solution.

2.2.1 Cascaded H-bridge multilevel inverter

A single-phase configuration of an *n*-level H-bridge cascaded inverter is depicted in Fig. 2.1. Each separate dc source is connected to a single-phase full-bridge/or H-bridge, inverter. Each inverter can generate three different voltage level outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain voltage level $+V_{dc}$, switches S_1 and S_4 turned on, where as for voltage level $-V_{dc}$ switches S_2 and S_3 turned on. Zero level voltage can obtain by turning on switches S_1 and S_2 or S_3, and S_4. AC outputs of each synthesized different full-bridge inverter levels are connected in series for summing up to generate multilevel voltage waveform. The number of output phase voltage *n*-levels in a cascade inverter defined by $n = 2l+1$, where l is

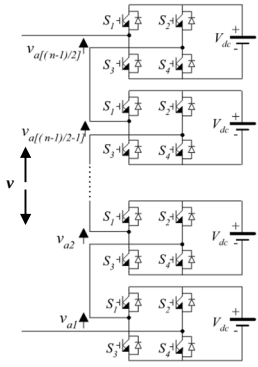


Fig. 2.1: Single leg of *n*-level cascaded H-bridge multilevel converter structure.

the number of separate dc sources. As example phase voltage waveform for *n*-level cascaded H-bridge inverter with (*n*-1)/2 separate dc sources and (*n*-1)/2 full bridges. The output phase voltage generalized as $v = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}\ldots\ldots\ldots\ldots\ldots + v_{an}$.

The Fourier transform of the corresponding stepped waveform follows [9, 5]:

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum [\cos(n\theta_1) + \cos(n\theta_2) + \ldots\ldots\ldots\ldots\ldots + \cos(n\theta_l)] \frac{\sin(n\omega t)}{n}, \quad (1)$$

where n = 1, 3, 5, 7

From Eqs.1, the magnitudes of the Fourier coefficients when normalized with respect to V_{dc} as follows:

$$H(n) = \frac{4}{\pi n} \sum [\cos(n\theta_1) + \cos(n\theta_2) + \ldots\ldots\ldots\ldots\ldots + \cos(n\theta_l)], \quad (2)$$

where n = 1, 3, 5, 7

By choosing conducting angles, θ_1, θ_2,.....,θ_l, such that the voltage total harmonic distortion (THD) is minimized. Predominately, these conduction angles for suppressing lower frequency harmonics of 5th, 7th, 11th, and 13th,… orders are eliminated in output [10].

Multilevel cascaded H-bridge converter, used for applications such as static var generator (SVG), an interface with renewable energy sources, and for battery-based system. Three-phase cascaded inverter can be connected in star, or in delta depending on the application. Experimental prototype model of (SVG) multilevel cascaded converter connected in parallel with the electrical system with flexibility to inject and/or absorbs reactive current flow from an electrical network was given by [11-14]. In this application multilevel cascaded inverter are controlled to regulate the power factor of the current drawn from the source or the bus voltage of the electrical network, where the inverter was installed. Also shown that cascade H-brige

inverter can be directly connected in series with the electrical network for static var compensation (SVC) experimentally given by [11, 15]. Cascaded H-bridge inverters are ideal choice for connecting renewable energy sources with ac grid, since need for separate dc sources which is applicable for photovoltaic and/or fuel cells.

The main benefits and drawbacks of cascaded H-bridge multilevel converters are briefly summarized as follows [16, 1-2]:

Benefits:

- The number of possible output voltage levels are more than twice the number of dc sources ($n = 2l+1$).
- The series of H-bridges makes for modularized layout and packaging. Enable the manufacturing process to be done more fast and cheap.

Drawbacks:

- Separate dc sources required for each of the H-bridges and could generate oscillating dc source power.

Other configuration of cascaded multilevel converter with transformers using standard three-phase bi-level converters was proposed in [8] and detail configuration is shown in Fig. 2.2. The converter uses transformers output to add different voltages. In particular, converters output voltages to be added up; three converters need to be synchronized with a separation of 120° between each phase. For instant to get a three-level voltage between outputs a and b, the output voltage can be synthesized by $v_{ab} = v_{a1\text{-}b1} + v_{b1\text{-}a2} + v_{a2\text{-}b2}$. Isolation transformer is used for step up the voltage and with three synchronized converters the voltages $v_{a1\text{-}b1} + v_{b1\text{-}a2} + v_{a2\text{-}b2}$, are all in phase with tripled output level given by [1].

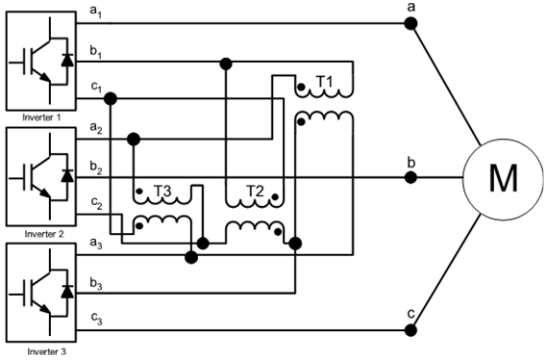


Fig. 2.2: Multilevel inverter with three-phase bi-level converters framed using transformers.

Benefits:

- Since the three power converters are identical and thus control become simpler.

Drawbacks:

- Three converters need separate dc sources, and additional transformer is needed to boost up the output voltages. Leads to complex and expensive structure.

To conclude that cascaded H-bridge multilevel converters are good solution for high power application with good quality of output multilevel voltages, but increasing the level leads to increase separate dc sources which can produce oscillating power and other version need additional expansion of circuitry.

2.2.2 Diode-clamped multilevel inverter

In 1981 Nabae, Takahashi, and Akagi proposed neutral-point converter as a three-level diode-clamped inverter [7]. In later years, further developments several research articles published with experimental results for four-, five-, and six-level diode-clamped converters, in particular applicable towards SVC, variable speed motor drives, and high-voltage system interconnections [4-5,11-22]. A three-phase six-level diode-clamped inverter configuration is shown in Fig. 2.3. Three phases of inverter shares a common dc bus, with five dc-link capacitors increases the levels to six. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device limited to V_{dc} through the clamping diodes.

Table 2.1 list the output voltage levels possible with one phase of inverter with the negative dc trail voltage v_o as reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that other complementary switch be turned off. The complementary switch pairs for phase leg are: (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), and (S_{a5}, $S_{a'5}$). Table 2.1 also shows that in a diode-clamped inverter, the switches that on for particular phase leg is always adjacent and in series.

For six-level inverter, a set of five switches is on at any given time. An n-level diode-clamped inverter has n-level output phase voltages and ($2n$-1)-level output line voltages. Although each active switching devices required to block only a voltage level of V_{dc}, the clamping diodes require different ratings for blocking reverse voltage. Using phase 'a' of Fig. 2.3 as example, when all the lower switches $S_{a'}$ through $S_{a'5}$ are turned on, D_4 must block four voltage levels, or $4V_{dc}$. Similarly, D_3 must block $3V_{dc}$, D_2 must block

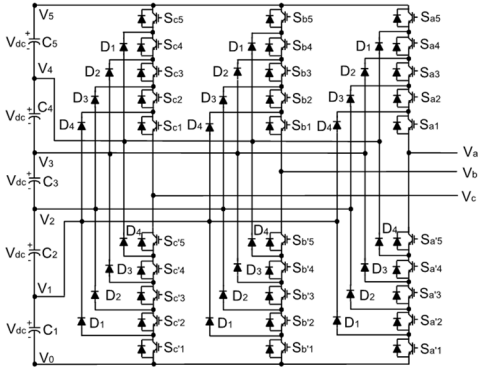


Fig. 2.3: Three-phase 6-level diode-clamped multilevel converter structure.

$2V_{dc}$, and D_1 must block V_{dc}. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_k will require k diodes in series; consequently, number of capacitor at dc side C, number of free wheeling diodes per phase D_w and number of clamping diodes Dc, are given by $C= n$-1; $D_w= 2.(n$-1); $Dc= (n$-1).(n-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter [2].

Table 2.1: Diode-clamped six-level inverter voltage levels and corresponding switch states.

Voltage v_{a0}	**Switch leg-states**									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$v_5 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$v_4 = 4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$v_3 = 3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$v_2 = 2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$v_1 = 1V_{dc}$	0	0	0	0	1	1	1	1	1	0
$v_0 = 0$	0	0	0	0	0	1	1	1	1	1

Practically, multilevel diode-clamped inverter found application as an interface between high-voltage dc transmission line and ac transmission line given in [2]. Other application mostly devoted towards variable speed drives for high-power medium-voltage (2.4 kV to 13.8 kV) motors as proposed in [3, 10, 16, 2]. SVC is an additional focuses for which several authors have proposed for the diode-clamped converter.

The main benefits and drawbacks of diode-clamped multilevel converter are briefly summarized as follows [1-3]:

Benefits:

- Capacitors requirement is minimized, since all the phases shares the same dc source. For this reasons diode-clamped multilevel converters used as a back-to-back converter and practically applicable to high-voltage back-to-back inter-connection and adjustable speed drives.
- Possibility to pre-charge all the capacitors as a group.
- Efficiency is high with fundamental frequency switching.

Drawbacks:

- It is difficult to control, real power flow in case of single inverter because it requires a very precise monitoring and control for intermediate dc levels, which tends to over charges or discharge.
- The number of clamping diodes required is quadratically related to the number of levels. Fundamental frequency switching will cause an increment on voltage and current THD, while increased number of clamping diode makes the configuration bulky.

To conclude diode-clamped multilevel converters are good solution for high power applications with reduced capacitor requirements and all capacitors energized with same dc source, but increasing the level leads to increases quadratically the clamping diodes and the configuration becomes complex with higher levels.

2.2.3 Flying capacitor-clamped multilevel inverter

In 1992 Meynard, and Foch, proposed flying capacitor-clamped multilevel inverter structure which is similar to diode-clamped multilevel inverter, differences instead of using clamping diodes, replaced by capacitors given in [23]. Flying capacitor-clamped multilevel inverter configuration is shown in Fig. 2.4, and as a ladder network of dc side capacitor, each capacitor voltages varies from the next capacitor. Increment in voltage between two adjacent capacitor legs gives the size for voltage steps in output waveform. Advantages of this configuration, it as redundancies with inner voltage levels; means if two or more valid switch combinations can synthesize the output voltage. Table 2.2 shows a list of all combination of phase voltage levels that are possible for six-level circuit shown in Fig. 2.4.

Unlike diode-clamped inverter, the flying-capacitor inverter does not require all switches that are on (conducting) in a consecutive series. Moreover, the flying capacitor-clamped inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [2-3, 24].

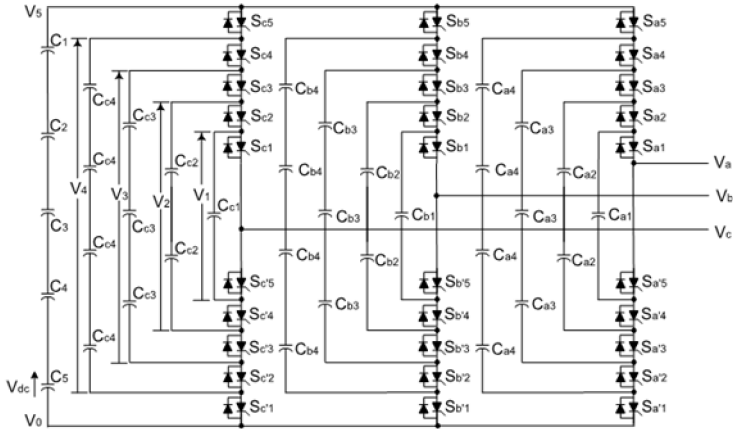


Fig. 2.4: Three-phase 6-level flying capacitor-clamped multilevel converter structure.

Redundancies allow a choice of charging/discharging specific capacitors and by incorporating the control system for balancing the voltages across the various levels. In addition to the (*n*-1) dc link capacitors, the *n*–level flying capacitor-clamped multilevel inverter will requires (*n*-1).(*n*-2)/2 auxiliary capacitor per phase, if the voltage rating of the capacitors is identical to that of the main switches. Flying capacitor multilevel converter found employing application for SVG is given in [2-3]. The main benefits and drawbacks of flying capacitor-clamped multilevel converters are briefly summarized as follows [2-3]:

Benefits:

- Phase redundancy is available for balancing the voltage levels of the capacitors.
- Controlled real and reactive power flow.
- Large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Drawbacks:

- Control is complex to track the voltage levels for all capacitors. Pre-charging all capacitors as a group to the same voltage level and startup are tidies.
- Switch utility ratio and efficiency are poor for real power flow.
- The large numbers of capacitors are both costly and bulky. Inverter construction is also more difficult with increasing levels.

Table 2.2: Flying capacitor-clamped six-level inverter voltage levels and corresponding switch states with redundancy in levels.

Voltage	Switch leg-states									
v_{a0}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$v_{a0}=5V_{dc}$ *(No redundancy)*										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$v_{a0}=4V_{dc}$ *(4 redundancy)*										
$5V_{dc}$-V_{dc}	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc}$-$4V_{dc}$+$3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc}$-$3V_{dc}$+$2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc}$-$2V_{dc}$+V_{dc}	1	1	1	0	1	0	0	0	1	0
$v_{a0}=3V_{dc}$ *(5 redundancy)*										
$5V_{dc}$-$2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc}$-V_{dc}	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc}$-$4V_{dc}$+$3V_{dc}$-V_{dc}	1	0	1	1	0	0	1	0	0	1
$5V_{dc}$-$3V_{dc}$+V_{dc}	1	1	0	0	1	0	0	1	1	0
$4V_{dc}$-$2V_{dc}$+V_{dc}	0	1	1	0	1	1	0	0	1	0
$v_{a0}=2V_{dc}$ *(6 redundancy)*										
$5V_{dc}$-$3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc}$-$4V_{dc}$+V_{dc}	1	0	0	0	1	0	1	1	1	0
$4V_{dc}$-$2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc}$-$3V_{dc}$+V_{dc}	0	1	0	0	1	1	0	1	1	0
$3V_{dc}$-V_{dc}	0	0	1	1	0	1	1	0	0	1
$3V_{dc}$-$2V_{dc}$+V_{dc}	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$v_{a0}=4V_{dc}$ *(4 redundancy)*										
$5V_{dc}$-$4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc}$-$3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc}$-$2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc}$-V_{dc}	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$v_{a0}=5V_{dc}$ *(0 redundancy)*										
0	0	0	0	0	0	1	1	1	1	1

2.3 Structures of other multilevel three-phase converters

Apart from the three basic multilevel inverter structures discussed in previous sections, other multilevel converter configuration have been reported in literatures, specifically addressing to “hybrid” networks that are combinations of two basic multilevel structures or with slight variations. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic configurations. In the next section, some hybrid network based multilevel converters are surveyed from literatures and described in detail as point of interest towards optimal solution.

2.3.1 Generalized multilevel converter structure

Generalized converter structure by which traditional diode-clamped and/or capacitor-clamped multilevel converters can be derived and such structures so called P2 multilevel converter configuration and illustrated in Fig.2.5 given by [25]. The generalized multilevel converter can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Hence the structure provides a complete multilevel configuration that embraces existing multilevel converters in principle. Fig. 2.5 shows the P2 multilevel converter structure per phase leg. Voltages in each switching device, diode, or capacitor's are $1V_{dc}$, for instance, 1/ (n-1) of the dc-link voltage. Any converter with any number of levels, including the conventional bi-level converter could derive by this generalized structure proposed by [1, 25].

2.3.2 Mixed-level hybrid multilevel converter structure

In order to minimize the number of separate dc sources for high-voltage and high-power applications with respect to multilevel converters, diode-clamped or capacitor-clamped converters can replace the full-bridge cell in a cascaded converter and such configuration example is shown in Fig. 2.6 proposed by [26]. A nine-level cascade converter, incorporated a three-level diode-clamped converter as the cell. An original cascaded H-bridge multilevel converter needs 4 separate dc sources per phase leg and 12 for three-phase converter. So, if a five-level converter replaces the full-bridge cell, the voltage level is doubled effectively for each cell. Thus, to achieve the same nine-level voltages for each phase, only requires 2 separate dc sources per phase leg and 6 separate dc sources for a three-phase converter. This configuration as mixed-level hybrid network multilevel units as it incorporated multilevel cells as the building block of the cascade converter.

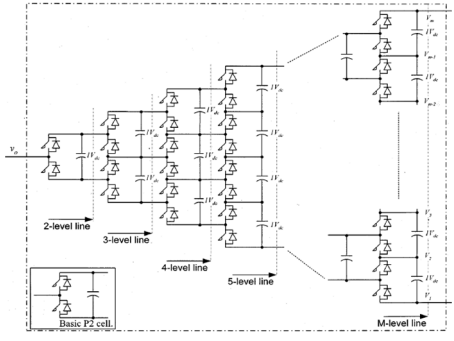


Fig. 2.5: Three-phase 6-level flying capacitor-clamped multilevel converter structure.

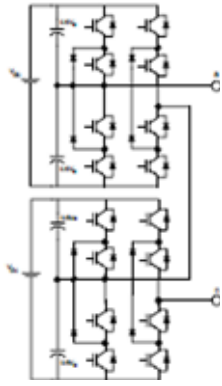


Fig. 2.6: Three-level diode-clamped converter as cascaded converter; (Mixed-level hybrid configuration for increasing output voltage levels).

Benefits:

- This configuration requires only less dc separate sources.

Drawbacks:

- Disadvantage leads to complex control of the configuration due to its hybrid network.

2.3.3 Multilevel converter with soft-switching configuration

In multilevel converters for minimizing the switching losses and to maximizing efficiency effectively, soft-switching techniques employed with additional L or L-C tank circuits. For instant in case, H-bridge cascaded converter, each converter cell is a bi-level circuit, employing the soft switching techniques in similar and with no difference that of conventional bi-level converter. Whereas in cases of capacitor-clamped or diode-clamped converters, soft-switching circuits needs different circuit combination. One such configuration of zero-voltage soft-switching with auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition

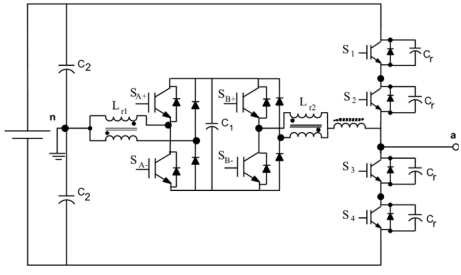


Fig. 2.7: Hybrid capacitor-clamped multilevel inverter with zero-voltage switching circuit.

(ZVT), and their combination leads to tank circuit is illustrated as shown in Fig. 2.7 found in [1, 27].

2.3.4 Diode-clamped multilevel converter as back-to-back converter

Two multilevel converters can be connected in a back-to-back combination and then can incorporated easily to the ac grid system as series-shunt compensators as shown in Fig. 2.8. In this way series-shunt multilevel compensators controlled simultaneously for the voltage delivered from the grid generator to the utility load and the current demanded from the utility grid. This series-shunt multilevel active power filter has been referred as a universal power conditioner (UPC), when considered from electrical distribution systems [28-34] and as universal power flow controller (UPFC) [35-39] when incorporated to ac transmission system, also generalized flexible ac transmission systems (FACTs) devices.

A back-to-back diode-clamped multilevel converter configuration shown in Fig. 2.9, for the purposes of high-voltage dc inter-connection between two asynchronous ac systems or as a rectifier/inverter for an adjustable speed drive for high-voltage motors was proposed and given in [2]. The diode-clamped multilevel inverter has been used, overcome the other two basic multilevel circuit structures with following benefits and to be used in a universal power conditioner.

Benefits:

- All six phases (three on each inverter) share common dc link.

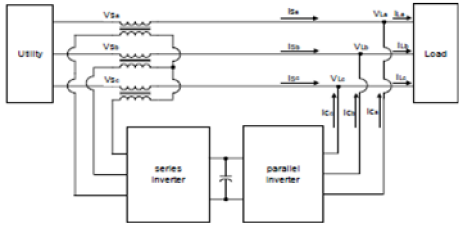


Fig. 2.8: Series-parallel combination of multilevel inverters for ac transmission system.

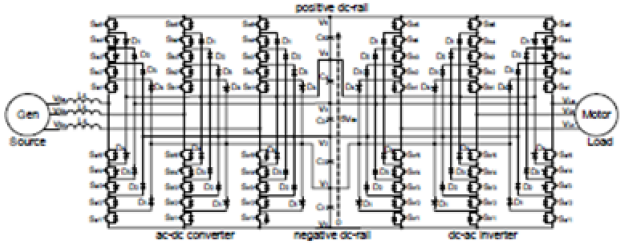


Fig. 2.9: Series-parallel combination of multilevel inverters for ac transmission system.

- Conversely, the cascade inverter requires that each dc level be separate, and this is not conducive to a back-to-back arrangement.
- The multilevel flying-capacitor converter also shares a common dc link; however, each phase leg requires several additional auxiliary capacitors. Substantially increase the cost and the size of the conditioner.

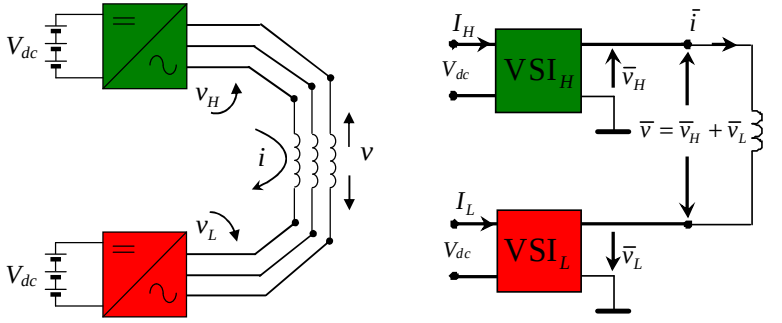
Drawbacks:

- Diode-clamped multilevel converter acting as a universal power conditioner expected to compensate harmonics and/or operate in low amplitude modulation index regions, a more sophisticated, higher-frequency switch control than the fundamental frequency switching method will be needed.

Finally, the majority of available work deals with the development of conventional multilevel converter structure modifications and focusing towards reducing dc separate sources or balancing the capacitor voltage across each cells and/or reducing the semi-conductor switches. This needs a more dedicated precise control schemes and leads to complex configurations. Moreover, for multilevel converters are used for reduced THD in their output voltage, for this purpose increasing high switching frequency leads increases the switching losses which become especially significant at high power levels. For this issue soft-switching multilevel converters are proposed by adding an LC resonant tank circuit to the basic configurations. But disadvantage of such configurations, inverter voltage or current peak values are considerably higher than that of basic multilevel converters, which leads to increases the required device ratings. Also the addition of resonant circuitry will increase the complexity and cost of the inverter control. In the next section, a possible solution with respect to cost and performances was discussed and provides an optimal survey of multilevel converter configuration.

2.4 Dual three-phase inverters as multilevel converter

Dual-inverters are derived from classical H-bridge cascaded configuration with slightly re-arranging the dc sources. A typical dual-inverter configuration and its corresponding equivalent circuit in three-phase space vectors representation are depicted in Fig.2.10a and Fig. 2.10.b [40-42]. This configuration can be framed by connecting two similar three-phase two-level inverters in ‘phase-opposition’ at the two ends of open-winding load, in order to get output voltages as a differences of two ingle inverter’s leg potentials as shown in Fig. 2.11. Correspondingly, dual-



(a) (b)

Fig. 2.10: Schematic diagram of dual –inverter. (a) Dual-inverter consists of two 2-level VSIs with open-winding load. (b) Equivalent circuit in terms of three-phase space vectors.

inverter output voltage with *l*-leg voltage levels with two 2-level inverters includes zero-level state given by $d = 2(4n\text{-}3)\text{-}1 = 8n\text{-}7$, where *d* gives the number of different output voltage levels. When each single inverter's modulated as a three-level inverter's, maximum of nine-level phase voltage can be generated across open-winding with different voltage levels as $-4V_{dc}/3, -V_{dc}, -2V_{dc}/3, -V_{dc}/3, 0, +V_{dc}/3, +2V_{dc}/3, +V_{dc}, +4V_{dc}/3$.

Dual-inverter with proper multilevel stepped waveforms (9-levels) output voltages based on modified multilevel space vector PWM techniques are proposed with experimental prototype model showing good power sharing with symmetrical and asymmetrical conditions in [42]. Advantages of this topology are has like traditional multilevel inverters reduced THD and lower *dv/dt* (leakage currents) at output voltages. An additional benefit includes no circulation of homo-polar or zero-sequence components, if the dc sources of the two inverters are insulated. Subsequently, no need of additional zero-sequence compensator circuits and/or additional compensation algorithm in the PWM techniques. Since two dc sources are insulated it provides additional degree of freedom to have two different power sources (fuel cells or batteries or photovoltaic cells) in such case power balancing of two sources become quite convenient. More recently such investigation carried out experimentally with dual-inverter fed from a photovoltaic system with maximum power point tracking (MPPT) algorithm under different irraditional conditions as active filter able to inject and/or absorbs reactive power flow connected to the grid given by [43] and it is an evident application of dual-inverter for renewable energy sources for future demands. In the next section, a detail analysis for determining output voltages expression is given briefly for three-phase dual-inverter.

2.4.1 Output phase voltage calculation

Expression for the output voltages of dual-inverter can be derived from standard two-level three-phase VSIs, taking into account that in case of dual-inverter there is no single inverter's (H and L) star point to express a leg phase voltages, i.e. line-to-neutral output. Hence, considering an artificial star point (N and M) between two series connected inverters as shown Fig.2.11, for expressing their individual (artificial phase voltage) line-to-neutral voltages.

Relation between the phase voltages and leg state can be determined for single inverter H (Fig. 2.11) from standard two-level three-phase inverter given by:

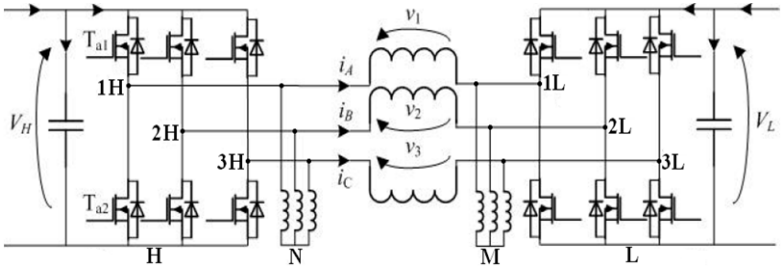


Fig. 2.11: Schematic diagram of the dual-inverter with star point for single inverter (H and L).

$$\begin{aligned} v_{1N} &= v_{1H} + v_{HN} \\ v_{2N} &= v_{2H} + v_{HN} \\ v_{3N} &= v_{3H} + v_{HN} \end{aligned} , \tag{3}$$

where 'H' is the negative pole of the dc link and presumed 'N' is the artificial star point of the single inverter H. To be noticed that v_{1H}, v_{2H}, v_{3H} takes the values either V_{dc} or zero. If the loads are unbalanced, then inherently contains zero-sequence voltage component independently from the connection of the star point and its components are given by:

$$v_{NH} = \frac{1}{3}\left[v_{1N} + v_{2N} + v_{3N}\right]. \tag{4}$$

Suppose the load is balanced and dc sources are insulated, then no circulation of zero-sequence component of the load voltages, it yields Eqs. 4 to zero.

Single inverter H its phase voltages (artificial line-to-neutral voltage) can illustrate by:

$$v_{1N} = \frac{1}{3}\left[2v_{1H} - v_{2H} - v_{3H}\right]$$
$$v_{2N} = \frac{1}{3}\left[-v_{1H} + 2v_{2H} - v_{3H}\right], \quad (5)$$
$$v_{3N} = \frac{1}{3}\left[-v_{1H} - v_{2H} + 2v_{3H}\right]$$

Eqs.5 can be expressed in terms switching states of 'leg' voltages as:

$$v_{1N} = \frac{1}{3}V_{dc}\left[2S_{1H} - S_{2H} - S_{3H}\right]$$
$$v_{2N} = \frac{1}{3}V_{dc}\left[-S_{1H} + 2S_{2H} - S_{3H}\right]. \quad (6)$$
$$v_{3N} = \frac{1}{3}V_{dc}\left[-S_{1H} - S_{2H} + 2S_{3H}\right]$$

where S_x={0, 1}.

Similar approaches can be made to single inverter L. Hence, the relation between the phase voltages and leg state can be given by:

$$v_{1M} = v_{1L} + v_{LM}$$
$$v_{2M} = v_{2L} + v_{LM}, \quad (7)$$
$$v_{3M} = v_{3L} + v_{LM}$$

where 'L' is the negative pole of the dc link and presumed 'M' is the artificial star point of the single inverter L.

To be noticed the same v_{1L}, v_{2L}, v_{3L} takes the values either V_{dc} or zero. If the loads are unbalanced, then inherently contains zero-sequence voltage component independently from the connection of the star point and its components are given by:

$$v_{ML} = \frac{1}{3}\left[v_{1M} + v_{2M} + v_{3M}\right]. \quad (8)$$

Suppose the load is balanced and dc sources are insulated, then no circulation of zero-sequence component of the load voltage, it yields Eqs. 8 to zero.

Hence, single inverter L its phase voltage (artificial line-to-neutral voltage) can be obtained by:

$$v_{1M} = \frac{1}{3}\left[2v_{1L} - v_{2L} - v_{3L}\right]$$
$$v_{2M} = \frac{1}{3}\left[-v_{1L} + 2v_{2L} - v_{3L}\right], \quad (9)$$
$$v_{3M} = \frac{1}{3}\left[-v_{1L} - v_{2L} + 2v_{3L}\right]$$

Eqs.9 can be expressed in terms switching states of 'leg' voltages as:

$$\begin{aligned} v_{1M} &= \frac{1}{3}V_{dc}\left[2S_{1L} - S_{2L} - S_{3L}\right] \\ v_{2M} &= \frac{1}{3}V_{dc}\left[-S_{1L} + 2S_{2L} - S_{3L}\right] \\ v_{3M} &= \frac{1}{3}V_{dc}\left[-S_{1L} - S_{2L} + 2S_{3L}\right] \end{aligned} \quad (10)$$

where S_x={0, 1}.

Finally, voltages across open-winding (phase voltage) of the dual-inverter can be expressed as the difference of single inverter voltage H and L:

$$\begin{aligned} v &= v_H - v_L \\ v_1 &= v_{1N} - v_{1M} \\ v_2 &= v_{2N} - v_{2M} \\ v_3 &= v_{3N} - v_{3M} \end{aligned} , \quad (11)$$

Taking into account Eqs. 5 and Eqs. 9, substituting in Eqs. 11 lead to the phase voltages across open-winding of the dual-inverter given by:

$$\begin{aligned} v_1 &= (2(v_{1H} - v_{1L}) - (v_{2H} - v_{2L}) - (v_{3H} - v_{3L})) \\ v_2 &= (-(v_{1H} - v_{1L}) + 2(v_{2H} - v_{2L}) - (v_{3H} - v_{3L})) \\ v_3 &= (-(v_{1H} - v_{1L}) - (v_{2H} - v_{2L}) + 2(v_{3H} - v_{3L})) \end{aligned} , \quad (12)$$

Eqs. 12 can be rewritten in the form of symmetrical matrix for emphasizes in simplified way as:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \underbrace{\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{1H} \\ v_{2H} \\ v_{3H} \end{bmatrix}}_{v_H} - \underbrace{\frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{1L} \\ v_{2L} \\ v_{3L} \end{bmatrix}}_{v_L} . \quad (13)$$

If the load is not properly balanced or/asymmetric and the corresponding zero-sequence component of the dual-inverter is given by:

$$v_{N-M} = \frac{1}{3}\left[v_{1N} + v_{2N} + v_{3N}\right] - \frac{1}{3}\left[v_{1M} + v_{2M} + v_{3M}\right], \quad (14)$$

If the load is symmetric Eqs. 14 leads to zero, and Eqs. 14 can be expressed in form of simplified matrix as:

$$\begin{bmatrix} v_{1-N-M} \\ v_{2-N-M} \\ v_{3-N-M} \end{bmatrix} = \underbrace{\frac{1}{3}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} v_{1H} \\ v_{2H} \\ v_{3H} \end{bmatrix}}_{v_{N-H}} - \underbrace{\frac{1}{3}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} v_{1L} \\ v_{2L} \\ v_{3L} \end{bmatrix}}_{v_{M-L}} . \quad (15)$$

Eqs. 13 and Eqs. 15 also can be expressed in term switching states of leg voltages as:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \underbrace{\frac{1}{3}V_{dc}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_{1H} \\ S_{2H} \\ S_{3H} \end{bmatrix}}_{v_H} - \underbrace{\frac{1}{3}V_{dc}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_{1L} \\ S_{2L} \\ S_{3L} \end{bmatrix}}_{v_L}. \tag{16}$$

$$\begin{bmatrix} v_{1-N-M} \\ v_{2-N-M} \\ v_{3-N-M} \end{bmatrix} = \underbrace{\frac{1}{3}V_{dc}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} S_{1H} \\ S_{2H} \\ S_{3H} \end{bmatrix}}_{v_{N-H}} - \underbrace{\frac{1}{3}V_{dc}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} S_{1L} \\ S_{2L} \\ S_{3L} \end{bmatrix}}_{v_{M-L}}. \tag{17}$$

where S_x={0, 1}. From Eqs. 3 to Eqs. 17 the dual-inverter can be analyzed in a simplified format for expressing its voltages and homo-polar components.

2.4.2 Output phase voltage calculation in terms of line-to-line voltages

As the fact dual-inverter posses no single inverter star point, the phase output voltages can also be calculated from their line-to-line voltages $v_{1H\text{-}2H}$, $v_{2H\text{-}3H}$, $v_{1L\text{-}2L}$, $v_{2L\text{-}3L}$ and can be obtained by:

$$\begin{aligned} v_{1H-1L} + v_{1L-2L} &= v_{1H-2H} + v_{2H-2L} \\ v_{2H-2L} + v_{2L-3L} &= v_{2H-3H} + v_{3H-3L} \end{aligned}, \tag{18}$$

Rearranging the Eqs. 18 lead to:

$$\begin{aligned} v_{1H-1L} - v_{2H-2L} &= v_{1H-2H} - v_{1L-2L} \\ v_{2H-2L} - v_{3H-3L} &= v_{2H-3H} - v_{2L-3L} \end{aligned}, \tag{19}$$

By subtracting above two equations, determines the phase voltage v_2 as:

$$\begin{aligned} &v_{1H-1L} - v_{2H-2L} = v_{1H-2H} - v_{1L-2L} \\ &v_{2H-2L} - v_{3H-3L} = v_{2H-3H} - v_{2L-3L} \\ &v_{1H-1L} - 2v_{2H-2L} + v_{3H-3L} = -3v_{2H-2L} = v_{1H-2H} - v_{1L-2L} - v_{2H-3H} + v_{2L-3L} \\ &v_2 = v_{2H-2L} = \frac{1}{3}\left[\left(v_{2H-3H} - v_{2L-3L}\right) - \left(v_{1H-2H} - v_{1L-2L}\right)\right] \end{aligned}, \tag{20}$$

Analogous way the representation of three-phase voltages can be expressed as:

$$\begin{aligned} v_1 &= v_{1H-1L} = \frac{1}{3}\left[\left(v_{1H-2H} - v_{1L-2L}\right) - \left(v_{3H-1H} - v_{3L-1L}\right)\right] \\ v_2 &= v_{2H-2L} = \frac{1}{3}\left[\left(v_{2H-3H} - v_{2L-3L}\right) - \left(v_{1H-2H} - v_{1L-2L}\right)\right] \\ v_3 &= v_{3H-3L} = \frac{1}{3}\left[\left(v_{3H-1H} - v_{3L-1L}\right) - \left(v_{2H-3H} - v_{2L-3L}\right)\right] \end{aligned}. \tag{21}$$

From Eqs. 21, it is to be noticed output phase voltages are measured or/calculated from four simultaneous voltages which leads to a complicated approach, but benefits avoid electromagnetic interferences (EMI) problem.

In next section, the advantageous of dual-inverter are detailed in comparison to classical three-phase and also with multilevel inverters.

2.4.3 Uniqueness of dual-inverter with other multilevel inverters

In comparison with other traditional multilevel inverters, dual-inverter posses own uniqueness for its merit shown by Fig. 2.10a and Fig. 2.12a, are briefly summarized as follow:

2.4.3A Comparison with standard 2-level inverter

When compare with standard 2-level inverter, dual-inverter can have maximum of nine-level multi-stepped output voltages leading to reduced THD and lowering *dv/dt*. For a standard two-level three-phase inverter with available dc bus voltage V_{dc} can provide phase voltage (line-to-neutral) in terms of peak and rms values as:

$$v_{peak} = \left(\frac{\sqrt{3}}{2} \cdot \frac{2}{3} V_{dc}\right) = 0.577 V_{dc} \rightarrow v_{rms} = 0.408 V_{dc} \tag{22}$$

Whereas in case of dual-inverter if the dc sources are insulated and of same amplitude, therefore with available dc bus voltage V_{dc} can provide phase voltage across the open-winding in terms of peak and rms values as:

$$v_{peak} = \underbrace{\left(\frac{\sqrt{3}}{2} \cdot \frac{2}{3} V_{dc}\right)}_{v_H} + \underbrace{\left(\frac{\sqrt{3}}{2} \cdot \frac{2}{3} V_{dc}\right)}_{v_L} = 1.15 V_{dc} \rightarrow v_{rms} = 0.816 V_{dc} \tag{23}$$

From Eqs. 22 and Eqs. 23 confirms the dual-inverter can provides the double the phase voltage of standard three-phase inverter [44], to be noted dual-inverter posses double the dc bus and also switch configuration.

2.4.3B Switch utilization factor comparison with standard 2-level inverter

The cost of switch depend on the voltage and current rating, for the required power level application and increases with required number of switch quantities for different converter configurations. Voltage of the switch are rated to reverse blocking voltage $V_{SW} = V_{dc}$ requirements and inverter current output related to the peak values $I_{SW} = 1.414 I_{rms}$. Switch utility ratio (*SUR*) is factor related to the converter output power S_C to the sum of power of the switches, for standard two-level three-phase inverter *SUR* given by considering the continuous peak current [45] as:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{6 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot V_{dc} \cdot I}{6 \cdot V_{dc} \cdot \sqrt{2} I_{ph}} = 0.144 \tag{24}$$

Since continuous peak current can not be applied, therefore the proper factor should take into account for continuous current rating. Moreover, due

to the physical reasons switch peak and continuous current ratings are usually proportional then:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{6 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot V_{dc} \cdot I}{6 \cdot V_{dc} \cdot I} = 0.204 \quad (25)$$

Similarly for the dual-inverter *SUR* calculation can be made with two sources having equal potential V_{dc} then:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{12 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot 2 \cdot V_{dc} \cdot I}{12 \cdot V_{dc} \cdot I} = 0.204 \quad (26)$$

From Eqs. 25 and Eqs. 26 observed that dual-inverter structure posses no advantages in comparison to standard three-phase inverter in term of the number of switches. The benefit of dual-inverter arises from the fact that use of components with lower voltage ratings enables bigger efficiency, since the MOSFETs on-state resistance is a strong function of the blocking drain-to-source (V_{DSS}) voltage rating. Hence MOSFETs can be good choice for low-voltage/high-current applications (less than 200v). Higher current rating can be achieved my connecting number of MOSFETs in parallel. The same power obtained by using single standard three-phase inverter with parallel switches, but this solution as few disadvantageous:

- The output current is doubled, which makes problems with load windings, losses and connections.
- Paralleling switches add additional problems, such as difficult current protection, different driver circuits, unsymmetrical current sharing.

2.4.3C Comparison with cascaded H-bridge inverter

Cascaded H-bridge multilevel inverter can easily scalable to higher number of levels but requires increasing insulated dc separate sources and also switches (Fig. 2.1). For example requires three dc separate sources and 12 switches for three-level version, but with oscillating power from each dc sources and requires additional compensations. A cascaded H-bridge inverter version with reduced switches proposed in [46] for five-levels and avoids the need of galvanic insulation. It is a scalable structure, but the bottom inverter has not a standard connection layout and all its switches must be rated to full dc voltage.

In this point, configuration shown in Fig. 2.10a and Fig. 2.12a could be simple connection of two standard 2-level inverters. Although it can not be scalable more than 9-levels but represents a viable solution to supply transformer and ac motors with two different insulated dc power sources (fuel cells or batteries or photovoltaic cells).

2.4.3D Comparison with diode-clamped and capacitor-clamped inverter

Switch requirement of diode-clamped three-level inverter (DCI) is same, but requires additional two diodes per each phase (six diodes in total) increases quadratically with increasing levels. DCIs require double the input with respect to same output provided by dual-inverter. Moreover, capacitors are to be incorporated for balancing the neutral point with single supply where as not need for dual-inverter. For the same input supply voltage and switch ratings rated power of the DCI is half of the rated power of the dual-inverter. For two separate power supplies neutral point clamped (NPC) inverter does not requires voltage balancing of the neutral point, it is the same for dual-inverter does not need to eliminate zero-sequence current. In case of single supply NPC, neutral point can be balanced by appropriate voltage vectors and capacitors. It applicable for dual-inverter for single inverter supply compensating the zero-sequence components by choosing appropriate vectors with the loss of lower voltage. Disadvantageous of DCI and capacitor-clamped three-level inverter (CCI) is same when compared with dual-inverter, additionally for CCI requires three flying capacitors per each phase (nine in total) and three capacitor for dc link. Advantages of CCI could be phase redundancy provided by each capacitor voltages with higher than 3-level when compared to dual-inverters. But consecutively which makes the CCI structure bulky and expensive.

2.4.3E Asymmetrical configuration for dual-inverter

Further dual-inverter has freedom to have two different single inverter's combination shown in Fig. 2.12b [47-48]. Restriction of the configuration could be no two current source inverter can be single inverters (H and L), since presumed both inverters posses the same current and it's the fact of the topology Fig. 2.10a.

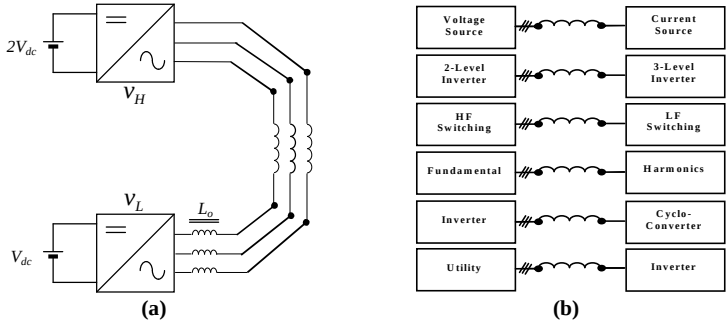


Fig. 2.12: Schematic diagram of dual-inverter. (a) Two single inverter with different potentials. (b) Different orientation of single inverter's combination.

2.4.3F Fault tolerance capability

Dual-inverter shown in Fig. 2.10a has fault tolerance capabilities when one single inverter (H or L) completely fails, but continue performing with half of the rated power as standard 2-level inverter. Consider that faulty inverter side of the winding, three-phase terminal should be short-circuited for current circulation. Additionally provides tolerance to open-phase fault [49], with addition of traic switch in each phase, this configuration is fault tolerant to single switch open or short and single-phase open-circuit.

2.5 Conclusion

In this chapter, a comprehensive study was made based on literature survey for multilevel converter topologies for identify an optimal solution. Among various configurations proposed dual-inverter posses its unique characteristics by simple combination of two standard 2-level three-phase inverter connected in 'phase-opposition' to an open-winding load. Even though it is not possible to have more than 9-level step phase voltages across open-winding when each single inverter's operated as 3-level inverter, but by its voltages output expression are discussed to show the degree of freedom to use two different insulated dc separate sources and significant to compensate zero-sequence components.

Furthermore, dual-inverter was compared with existing multilevel converter technologies, to show its merit and symmetric/asymmetrical power sharing capabilities with out additional price of expansion with in or outside the circuitry. Finally to conclude, dual-inverter can be better solution with performances and cost, applicable to ac motor, transformer and renewable energy sources keep open broad research studies and step to extend for multiphase power conversion application.

3. Review of multiphase inverters

3.1 Motivation for research

In this chapter provides a significant study based on literatures, analytically for multiple space vectors transformation focus towards a six-phase system and its corresponding orthogonal sub-spaces. In particular, multiple space vector transformation to describes a six-phase system was simplified by using two three-phase sub-systems by space vector decomposition method includes inverse transformation to get individual three-phase sub-systems from multiple space vectors. Increasing the phases of the converter allows exploit the degree of freedom, investigating the system when one, two or more phases under severer failure circumstances. In this point survey also made with respect available multiphase inverter technologies, their application and to identify optimal increases in inverter phases, which suitable for multiphase ac motor configurations.

3.2 Six-phase voltage source inverter

Increasing demands for multiphase inverter technologies (n>3) for high power ratings with current limited devices [50-51]. Multiphase inverter based on their configuration flexibility; easily incorporate to the multiphase ac motors which found many applications in electric ship propulsions, ac traction and 'more-electric' aircraft etc. Similar to multilevel inverters, multiphase inverters provides reduced THD and lowering *dv/dt* stress in the voltages output. Moreover multiphase inverter posses phase redundancy under faulty conditions, which is the predominant advantages of this technologies when compared to traditional (n=3) multi-level inverters. Also multiphase inverter provides facilities to split the dc sources and share the power for maximum modulation utilizations. Hence the voltage rating of switching devices can be significantly reduced with splitting the voltage dc-bus. In case, three-phase inverter holds only one load equivalent circuit, whereas multiphase inverter (n>3) has (n-1)/2 load equivalent circuits if n=odd number of phases and if n= even number of phases has n/2 load equivalent circuits. Each equivalent circuit could perform in an n-step mode to produce unique discrete ac or 'stair-step' voltage waveform and differ in terms of harmonic content and magnitude of the fundamental components. For example a six-phase inverter has 3 different load equivalent circuits.

Recently more literatures work found addressing a six-phase VSIs application for dual three-phase induction motor (symmetrical or asymmetrical configurations) [52-53]. Typical schematic diagram of six-

Keywords**:** *Multiple space vectors, six-phase inverter, three-space vector decomposition, inverse three-phase space vector decomposition, five-, seven- and nine-phase inverters, and multiphase conversion system.*

phase VSI is shown in Fig. 3.1a and Fig. 3.1b, showing the possibility to have star connected load or split-phase load with insulated neutral points. Fig. 3.1a topology as disadvantage by posses homo-polar components/or zero-sequence components since the neutral point are not insulated, requires additional compensation in the PWM algorithm or zero-sequences reactor is required, where as in Fig. 3.1b zero-sequence component exist null as insulated neutral point under balanced load conditions, it was analyzed theoretically and proposed in [52]. Six-phase inverter (Fig. 3.1b) configuration was built with two 2-level standard three-phase VSIs, with two separate dc sources fed to dual three-phase induction motor was proposed in [54]. Further steps six-phase inverter (Fig. 3.1b) keep it strength by providing possibility to investigate, by framed from two dual-inverters fed to a six-phase open-winding load in later cases, i.e. their exist no neutral point in two three-phase winding. Such multiphase inverter configuration could be good solution for multiphase induction motor with open-end winding stator configurations (multiple phases increased by n>3) having multi-stepped voltages across each winding.

In next section, a detailed multiple space vectors transformation analysis was illustrated for six-phase VSI for two three-phase winding insulated loads. In such case six-phase VSI able to arbitrarily regulates independently both the two multiple voltage space vectors, which in term control the two three-phase winding voltages of the loads with optimal exploitation of dc bus.

3.3 Multiple space vector transformation

In 1918 Fortescue published a milestone paper on the AIEE entitled "Method of symmetrical coordinates applied to the solution of polyphase Networks" [55]. The proposed transformation soon became generally known as the method of symmetrical components, and it greatly facilitated the analysis of unbalanced three-phase systems. The Fortescue's approach

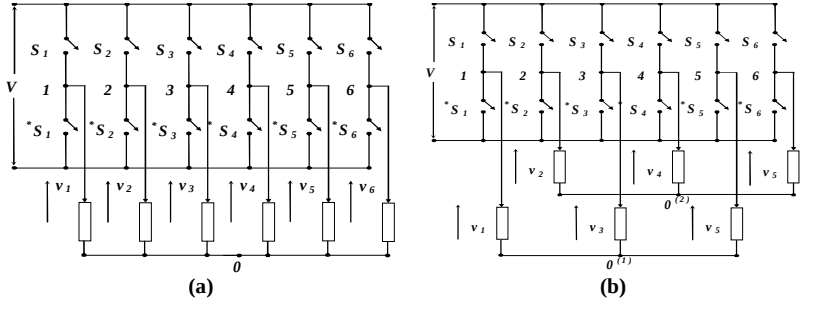


Fig. 3.1: Schematic diagram of six-phase converter feeding six-phase load. (a) Without insulated neutral point. (b) With insulated two neutral points.

considers phasors i.e., constant complex numbers representing, in a compact form, the amplitude and the phase angle of sinusoidal quantities. In past decades a similar transformation has been widely applied to three-phase instantaneous variables, leading to the definition of space vectors, i.e., complex numbers moving in a plane usually called *d-q* plane [56-57].

The space vector approach allows simplifying the modeling and regulation of both the converter and the machine in traditional three-phase motor drive application. However, when the machine is connected with an inverter supply, the need for a specific number of phases, such as three, disappears. On other hand, the development of modern power electronic devices, make it possible to consider the number of phases as a degree of freedom, i.e., as one of the design variables. In order to analyze multiphase system, Fortescue's and space vector transformation can be still valid.

As in the case of three phase systems, the Fortescue's method applied to multiphase system consider only steady-state conditions, whereas the space vector theory can be referred to arbitrary time-dependent variables. Then, by the space vector approach, real time analysis and regulation of both the multiphase converter and the multiphase machine can be performed with an elegant and effect vectorial approach. Space vector approach for multiphase systems is developed as a natural extension of the Fortescus's transformation, leading to the definition of multiple space vectors lying in different *d-q* planes [58].

3.3.1 Six-phase multiple space vector transformation

Space vector transformations are introduced in this section to represent the whole six-phase system consisting of two three-phase winding loads with insulated neutral point and supplied by a six-phase VSI shown in Fig. 3.1b. A possible space vector transformation for an asymmetric six-phase system leads to the following multiple space vectors [52-53] in orthogonal space dimension as (Fig. 3.2):

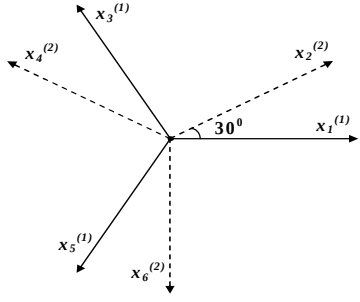


Fig. 3.2: Representation of six-phase asymmetrical system orientation in *d-q* axis**.**

$$\bar{x}_h = \frac{1}{3}\left[x_1 + x_2\alpha^h + x_3\alpha^{4h} + x_4\alpha^{5h} + x_5\alpha^{8h} + x_6\alpha^{9h} \right]. \quad (1)$$

being $\alpha = exp\,(j\pi/6)$ and h=1, 3, 5.

Where two three-phase winding loads spatially shifted by an electrical angle by 30^0 degree (asymmetrical $180^0/6=30^0$). By developing Eqs. 1 with respect to the index h yields:

$$\begin{cases} \bar{x}_1 = \frac{1}{3}\left[x_1 + x_2\alpha + x_3\alpha^4 + x_4\alpha^5 + x_5\alpha^8 + x_6\alpha^9 \right] \\ \bar{x}_3 = \frac{1}{3}\left[(x_1 + x_3 + x_5) + j(x_2 + x_4 + x_6) \right] \\ \bar{x}_5 = \frac{1}{3}\left[x_1 + x_2\alpha^5 + x_3\alpha^8 + x_4\alpha + x_5\alpha^4 + x_6\alpha^9 \right] \end{cases}. \quad (2)$$

Note that the space vector $\bar{x}_3$ has a singular expression since 3 is a factor of the number of phase n=6, which is not a prime. Inverse transformation of Eqs. 2 are given by:

$$\begin{cases} x_1 = \bar{x}_3 \cdot 1 + \left(\bar{x}_1 + \bar{x}_5^*\right)\cdot 1 \\ x_3 = \bar{x}_3 \cdot 1 + \left(\bar{x}_1 + \bar{x}_5^*\right)\cdot \alpha^4 \\ x_5 = \bar{x}_3 \cdot 1 + \left(\bar{x}_1 + \bar{x}_5^*\right)\cdot \alpha^8 \end{cases}, \begin{cases} x_2 = \bar{x}_3 \cdot j + \left(\bar{x}_1 - \bar{x}_5^*\right)\cdot \alpha \\ x_4 = \bar{x}_3 \cdot j + \left(\bar{x}_1 - \bar{x}_5^*\right)\cdot \alpha^5 \\ x_6 = \bar{x}_3 \cdot j + \left(\bar{x}_1 - \bar{x}_5^*\right)\cdot \alpha^9 \end{cases}. \quad (3)$$

where the symbols "$*$" and "$\cdot$"denote complex conjugate and scalar (dot) product, respectively. The multiple space vectors $\bar{x}_1$, $\bar{x}_3$, and $\bar{x}_5$ lie in the planes here called d_1- q_1, d_3- q_3 , and d_5- q_5, respectively.

3.3.2 Three-phase space vector decomposition

The six-phase system can be seen as the composition of two three-phase sub-systems {1} and {2} according to:

$$\{1\}\begin{cases} x_1^{(1)} = x_1 \\ x_2^{(1)} = x_3 \\ x_3^{(1)} = x_5 \end{cases}, \quad \{2\}\begin{cases} x_1^{(2)} = x_2 \\ x_2^{(2)} = x_4 \\ x_3^{(2)} = x_6 \end{cases}. \quad (4)$$

The space vectors, $\bar{x}^{(1)}$, $\bar{x}^{(2)}$ and the zero-sequence components $x_0^{(1)}$, $x_0^{(2)}$ can be defined for each three-phase sub-system {1}, {2}, leading to:

$$\begin{cases} \overline{x}^{(1)} = \dfrac{2}{3}\left[x_1^{(1)} + x_2^{(1)}\alpha^4 + x_3^{(1)}\alpha^8 \right] \\ x_0^{(1)} = \dfrac{1}{3}\left[x_1^{(1)} + x_2^{(1)} + x_3^{(1)} \right] \end{cases} . \quad (5)$$
$$\begin{cases} \overline{x}^{(2)} = \dfrac{2}{3}\left[x_1^{(2)} + x_2^{(2)}\alpha^4 + x_3^{(2)}\alpha^8 \right] \\ x_0^{(2)} = \dfrac{1}{3}\left[x_1^{(2)} + x_2^{(2)} + x_3^{(2)} \right] \end{cases}$$

The relationships between multiple space vectors and two three-phase space vectors are obtained by introducing Eqs. 4 and Eqs. 5 in Eqs. 1, leading to:

$$\begin{cases} \overline{x}_1 = \dfrac{1}{2}\left[\overline{x}^{(1)} + \alpha\, \overline{x}^{(2)} \right] , \quad \overline{x}_3 = x_0^{(1)} + j\, x_0^{(2)} \\ \overline{x}_5^* = \dfrac{1}{2}\left[\overline{x}^{(1)} - \alpha\, \overline{x}^{(2)} \right] \end{cases} . \quad (6)$$

3.3.3 Inverse three-phase space vector decomposition

The space vectors $\overline{x}^{(1)}$, $\overline{x}^{(2)}$ and the zero-sequence components $x_0^{(1)}$, $x_0^{(2)}$ of the three-phase sub-system expressed below on the basis of the multiple space vectors $\overline{x}_1$, $\overline{x}_5^*$, and $\overline{x}_3$ as:

$$\begin{cases} \overline{x}^{(1)} = \overline{x}_1 + \overline{x}_5^* \\ x_0^{(1)} = \overline{x}_3 \cdot 1 \end{cases}, \begin{cases} \overline{x}^{(2)} = \alpha^{-1}\left(\overline{x}_1 - \overline{x}_5^* \right) \\ x_0^{(2)} = \overline{x}_3 \cdot j \end{cases} . \quad (7)$$

Space vector decomposition method provides a simplified approach to represent multiple space vectors of a six-phase asymmetrical system with following advantageous:

- The fundamental components of the system variables and the harmonics of the order $k=6.n\pm1$, (n=0, 2, 4…) are mapped in the first sub-space $\overline{x}_1$.
- The harmonics of order $k=6.n\pm1$, (n=1, 3, 5…) are mapped in the fifth sub-space $\overline{x}_5^*$, which orthogonal to the first sub-space $\overline{x}_1$ and first sub-space posses free of odd harmonics order.
- The homo-polar components or zero-sequences components of order $k=3.n$, (n=0, 1, 2, 3…) are mapped in the third sub-space $\overline{x}_3$.

Hence from Eqs.6, the behavior of the system can be described in terms of two independent multiple space vectors $\overline{x}_1$ and $\overline{x}_5^*$, moving arbitrarily in, d_1- $q_1$and d_5- q_5 planes, easily regulated simultaneously.

3.4 Other multiphase voltage source inverter configuration

Apart from six-phase converters other topologies available having phases (n>3) and such configuration described in literatures are shown in Fig. 3.3-3.5. First version of multiphase inverters technology are five-phase VSI fed to star connected five-phase load and its schematic configuration is shown in Fig. 3.4 [50]. Five-phase VSI configuration found application for five-phase induction machine (consecutive windings spatially shifted by 72^0 degree electrical angle) and synchronous machines drives with third space stator current harmonic injection for torque enhancement and also hysteresis based direct torque control purposes well reported with experimental results in [50-51].

Seven-phase VSI fed to star connected seven-phase load based on multiple space vector modulation approach was proposed in [59] and its schematic configuration is shown in Fig. 3.4. Seven-phase VSI configuration found applications for seven-phase permanent magnet synchronous and synchronous reluctance motor drives (consecutive windings spatially shifted by 51.42^0 degree electrical angle) and investigated intensively and experimental results are given by [60]. By third and fifth space stator current harmonic injection the torque was enhanced in a seven-phase machine.

Nine-phase VSI fed to star connected nine-phase load based on space vector modulation was proposed in [61] and its schematic configuration is shown in Fig. 3.5a and connected to split-phase load, three-phase windings (three numbers) with insulated neutral point is shown in Fig. 3.5b based on three-phase space vector decomposition approach proposed in [62].

Nine-phase VSI found application for nine-phase induction machine with symmetrical (consecutive windings spatially shifted by 40^0 degree electrical angle) detailed in [63] and asymmetrical configurations (any two three-phase windings sets spatially shifted by 20^0 degree electrical angle) given

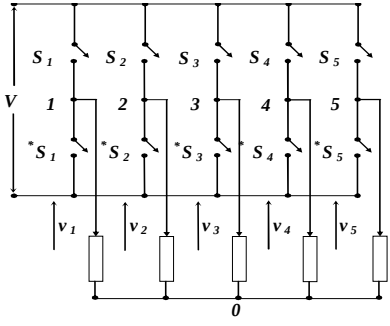


Fig. 3.3: Schematic diagram of five-phase converter feeding five-phase load.

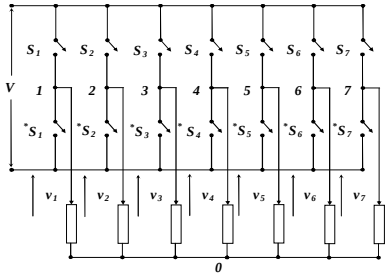


Fig. 3.4: Schematic diagram of seven-phase converter feeding seven-phase load.

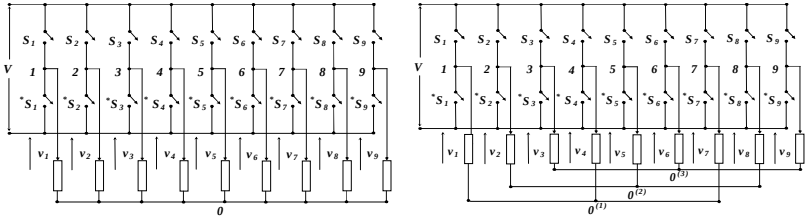


Fig. 3.5: Schematic diagram of nine-phase converter feeding nine-phase load. (a) With out insulated neutral point. (b) With insulated three neutral points.

by [64]. By third, fifth and seventh space stator current harmonic injection the torque was enhanced in a nine-phase machines.

3.5 Conclusion

In this chapter, a significant study was carried out on multiple space vectors transformation for six-phase system based on three-phase space vector decomposition approach analytically. By this technique an asymmetrical six-phase VSI, easily controlled based on two arbitrary rotating reference modulating space vector in *d-q* plane simultaneously and more suitable for dual three-phase asymmetrical induction motor applications. Literature survey was also made for multiphase converter topologies (n>3), identify an optimal increases in phase redundancy. In particular five-, seven-, and nine-phase VSIs are addressed in articles more suitably for multiphase ac drive systems. Among these configurations six-phase VSI posses its characteristics by simple combination and could suitable for six-phase star connected load and/or also to neutral point insulated with two separate three-phase loads.

Further step for research studies six-phase VSI keep its merit open by constructed from three-phase dual-inverter with open-winding loads. Also provides optimized multi-stepped output waveform across each winding

with multilevel space vector PWM techniques. This configuration could be good solution for extending the phases in multiple of three for multiphase induction machine (n=9, 12...) drive systems.

4. Quad-inverter based multiphase-multilevel inverter configuration

4.1 Introduction

Exploiting advantages of multilevel and multiphase inverters discussed in chapters 2 and 3, in this chapter a novel multiphase-multilevel inverter configuration was proposed. The proposed configuration essentially consist of four standard 2-level three-phase voltage source inverters (VSIs) supplying the two three-phase passive loads in open-winding configuration. Based on three-phase inverse space vector decomposition approach the converter modulated with two arbitrarily rotating space vectors reference signals, which in turn control output voltages of two three-phase open-winding loads. The proposed control scheme is able to generate multilevel voltage waveforms, equivalent to the ones of a 3-level inverter, and to share the total motor power among the four dc sources in each switching period with three degree of freedom. Detailed theoretical descriptions of the proposed converter system are given and some carrier based modulation approaches are discussed along with implementation in numerical simulation software.

4.2 Proposed multiphase-multilevel inverter

Multilevel inverters recognized as a viable solution for high power rating with voltage-limited devices [1, 65-66] and discussed in detail chapter 2. It is evident that the combination of multiphase and multilevel inverter technologies [67], details provided by chapter 3 to obtain high power ratings with both voltage- and current-limited devices. In this point, a novel multiphase-multilevel inverter is proposed in this section and shown in Fig. 4.1. The configuration is basically derived and extension from a dual-inverter topology discussed in chapter 3, for utilizing its abundant advantages as multilevel converter [42-43]. In detail, the power supply consists of four standard 2-level three-phase VSIs having insulated dc sources to prevent circulation of zero-sequence components in the whole system. Quad-inverter configuration characterized by power sharing among the four VSIs in each switching period with three degree of freedom. Where first one concern with current sharing between two three-phase open-windings {1} and {2}. The second degree of freedom relates to the voltage sharing between inverters (H and L) of the first three-phase winding {1} and where as third relates to voltage sharing between inverters (H and L) of

Keywords**:** *Multiple space vectors, three-space vector decomposition, inverse three-phase space vector decomposition, multiphase-multilevel inverter, quad-inverter, dual three-phase open-winding loads, power sharing and carrier based PWM techniques.*

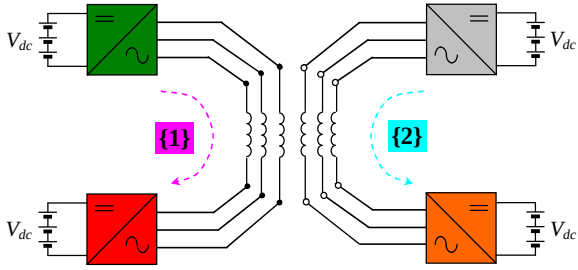


Fig. 4.1: Schematic diagram of the proposed multiphase-multilevel inverter system consisting in four VSIs supplying two three-phase open-winding loads (passive load).

the second three-phase winding {2}. By adopting proper modified multilevel space vector pulse modulation (SVPWM), phase voltages across each open-winding can have multi-stepped waveform (maximum 9-levels). As like multilevel inverter, quad-inverter posses merit to its structure having reduced THD and lower *dv/dt* at the output. Even though two three-phase windings are isolated from each other, mechanically as well as electrically, phase redundancy could be the additional price of the quad-inverter system even one three-phase winding completely suffered with fault, being operable with half rated power, when suitably connected with multiphase ac motor. Note that this structure can be easily scalable to higher number of phases (n=9, 12,) as multiple of three, which in turn can be prominent solution for multiphase ac motor drives. Switch utility ratio for the proposed quad-inverter system is the same has dual-inverter discussed in section 2.3.3b in chapter 2 and increasing switches as no effect and given by:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{24 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot 4 \cdot V_{dc} \cdot I}{24 \cdot V_{dc} \cdot I} = 0.204 \qquad (1)$$

Summarizing the special feature of the proposed quad-inverter as:

- Low-voltage high-current application.
- Good electromagnetic compatibility, increased efficiency and intensive fault tolerance capability.
- Quadrupling the power capability with four standard 2-level VSIs.

In the next section, equivalent three-phase space vector representation of the quad-inverter system is discussed with power sharing capabilities for single inverter's (H and L) (quad VSIs).

4.3 Space vector representation for quad-inverter

The proposed quad-inverter is represented in three-phase space vectors equivalent circuit in Fig. 4.2. In this configuration dual-inverters {1} and {2} as individually 8x8=64 switching states each of them. The space vectors $\bar{v}^{(1)}$ and $\bar{v}^{(2)}$ corresponds to the output voltage space vectors of two three-phase dual-inverters as represented in the Fig. 4.2 and based on Eqs. 11 given by chapter 2 output voltage of two dual-inverter {1} and {2} are given by:

$$\begin{aligned} \bar{v}^{(1)} &= \bar{v}_H^{(1)} + \bar{v}_L^{(1)} \\ \bar{v}^{(2)} &= \bar{v}_H^{(2)} + \bar{v}_L^{(2)} \end{aligned} . \tag{2}$$

where, load voltages based on individual space vector components of the each inverter H and L given as:

$$\begin{aligned} \bar{v}_H^{(1)} &= (2/3)V_{dc} \cdot \left(S_{1H} + S_{2H} e^{(j2/3)\pi} + S_{3H} e^{(j4/3)\pi} \right) \\ \bar{v}_L^{(1)} &= -(2/3)V_{dc} \cdot \left(S_{1H} + S_{2H} e^{(j2/3)\pi} + S_{3H} e^{(j4/3)\pi} \right) \\ \bar{v}_H^{(2)} &= (2/3)V_{dc} \cdot \left(S_{1H}^{(j1/6)\pi} + S_{2H} e^{(j5/6)\pi} + S_{3H} e^{(j3/2)\pi} \right) \\ \bar{v}_L^{(2)} &= -(2/3)V_{dc} \cdot \left(S_{1H}^{(j1/6)\pi} + S_{2H} e^{(j5/6)\pi} + S_{3H} e^{(j3/2)\pi} \right) \end{aligned} . \tag{3}$$

Since there is no star point in two three-phase winding and the four dc sources are insulated, the zero sequence component $v_0^{(1)}=v_0^{(2)}=0$. Based on inverse three-phase decomposition approach (Eqs.7 by chapter 3) can used to determine the reference voltage space vector for the two three-phase open-windings loads as:

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_{S1,ref} + \bar{v}_{S5,ref}^{*} \\ \bar{v}^{(2)} = \alpha^{-1} \left(\bar{v}_{S1,ref} + \bar{v}_{S5,ref}^{*} \right) \end{cases} . \tag{4}$$

The space vector determined by the Eqs. 4, can be independently synthesized by using well know three-phase SVM technique and shown Fig. 4.3a and Fig. 4.3b for inverters H and L, applicable for both dual-inverters

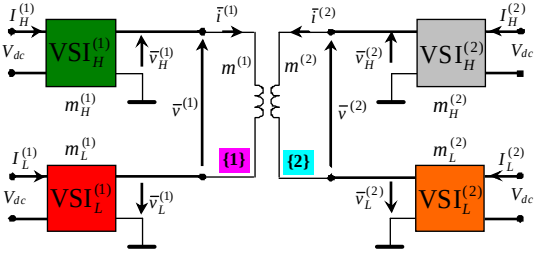
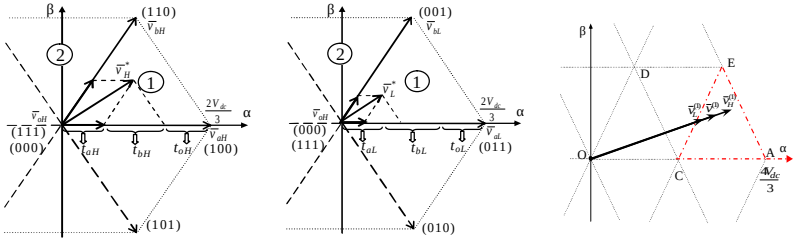


Fig. 4.2: Equivalent circuit of multiphase-multilevel inverter with open-winding loads in terms of three-phase space vectors.

{1} and {2}. In case of balanced sinusoidal voltages, the voltage limit is determined by the space vector $\overline{v}_{S1,ref}$, with the condition $\overline{v}_{S3,ref} = \overline{v}_{S5,ref} = 0$, this leads to the following voltage space vectors for the two three-phase open-windings loads also corresponds to the inverters H and L by:

$$\begin{cases} \overline{v}^{(1)} = \overline{v}_{S1,ref} \\ \overline{v}^{(2)} = \alpha^{-1} \cdot \overline{v}_{S1,ref} \end{cases} . \tag{5}$$

Two three-phase dual-inverter supplying two three-phase open-winding loads are independent from each other; the voltage limit for each three-phase dual-inverter voltage space vector are represented by the regular hexagon having $4/3\,V_{dc}$ and shown in Fig. 4.4. Having sinusoidal balanced voltages, the voltage limits corresponds to the outer circle radius of $2/\sqrt{3}V_{dc}$ as shown clearly in Fig. 4.4 and due to the symmetric of the triangles the analysis can be restricted to triangle OAB (shaded area) [42-43]. To have proper power sharing with multilevel waveform, the arbitrarily rotating reference vector of two dual-inverter {1} and {2} should be collinear vectors, sharing principle of single inverter's ($H^{(1)}$ and $L^{(1)}$) are shown in Fig. 4.3c [43].



(a) (b) (c)

Fig. 4.3: Space vector representation for two inverter forming dual-inverter {1} and {2} (a) Inverter H. (b) Inverter L. (c) Power sharing between inverter H and L.

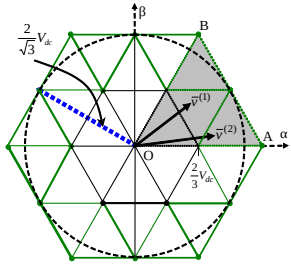


Fig. 4.4: Voltage space vectors generated by inverters H and L for the open-winding loads {1} and {2}.

4.4 Output power calculation and open-loop control scheme (Inverse space vector decomposition)

The total power P provided by the quad-inverter fed two three-phase open-winding loads expressed below as:

$$P = P^{(1)} + P^{(2)} = \frac{3}{2}\left[\bar{v}^{(1)} \cdot \bar{i}^{(1)} + \bar{v}^{(2)} \cdot \bar{i}^{(2)} \right] \tag{6}$$

The power $P^{(1)}$ and $P^{(2)}$ being provided by individual two three-phase dual-inverter {1} and {2} can be given by:

$$\begin{cases} P^{(1)} = P_H^{(1)} + P_L^{(1)} = \frac{3}{2}\bar{v}^{(1)} \cdot \bar{i}^{(1)} \\ P^{(2)} = P_H^{(2)} + P_L^{(2)} = \frac{3}{2}\bar{v}^{(2)} \cdot \bar{i}^{(2)} \end{cases}. \tag{7}$$

Two three-phase open-windings voltages $\bar{v}^{(1)}$ and $\bar{v}^{(2)}$ can be written as the sum of individual inverter voltages H and L as below:

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_H^{(1)} + \bar{v}_L^{(1)} \\ \bar{v}^{(2)} = \bar{v}_H^{(2)} + \bar{v}_L^{(2)} \end{cases}. \tag{8}$$

By imposing the first degree of freedom k_i concerns with the power (current) sharing between two three-phase open-windings {1} and {2} Eqs. 7 lead to:

$$\begin{cases} \{1\} \rightarrow P^{(1)} \cong k_i P \\ \{2\} \rightarrow P^{(2)} \cong (1 - k_i) P \end{cases}. \tag{9}$$

By imposing the second $k_v^{(1)}$ and third $k_v^{(2)}$ degree of freedoms related to power (voltage) sharing between the two inverters "H" and "L" which supply each three-phase open-windings {1} and {2} Eqs. 8 lead to:

$$\begin{cases} \bar{v}_H^{(1)} = k_v^{(1)} \bar{v}^{(1)} \\ \bar{v}_L^{(1)} = \left(1 - k_v^{(1)}\right) \bar{v}^{(1)} \end{cases} \rightarrow \{1\}; \begin{cases} \bar{v}_H^{(2)} = k_v^{(2)} \bar{v}^{(2)} \\ \bar{v}_L^{(2)} = \left(1 - k_v^{(2)}\right) \bar{v}^{(2)} \end{cases} \rightarrow \{2\}, \tag{10}$$

Then Eqs. 7 becomes by considering the voltage sharing coefficients:

$$\{1\} \rightarrow \begin{cases} P_H^{(1)} = k_v^{(1)} P^{(1)} \\ P_L^{(1)} = \left(1 - k_v^{(1)}\right) P^{(1)} \end{cases}. \tag{11}$$

$$\{2\} \rightarrow \begin{cases} P_H^{(2)} = k_v^{(2)} P^{(2)} \\ P_L^{(2)} = \left(1 - k_v^{(2)}\right) P^{(2)} \end{cases}. \tag{12}$$

By combining Eqs.9 with Eqs.11 and Eqs.12, lead to express the total power sharing of the proposed quad-inverter as:

$$\begin{cases} P_H^{(1)} \cong k_i k_v^{(1)} P^{(1)} \\ P_L^{(1)} \cong k_i \left(1-k_v^{(1)}\right) P^{(1)} \end{cases}$$

$$\Rightarrow P^{(1)} \cong \frac{3}{2}\left[k_i \cdot \left(k_v^{(1)} \cdot \bar{v}_H^{(1)} + \left(1-k_v^{(1)}\right) \cdot \bar{v}_L^{(1)}\right) \cdot \bar{i}^{(1)}\right] \quad .$$

$$\begin{cases} P_H^{(2)} \cong (1-k_i) k_v^{(2)} P^{(2)} \\ P_L^{(2)} \cong (1-k_i)\left(1-k_v^{(2)}\right) P^{(2)} \end{cases} \tag{13}$$

$$\Rightarrow P^{(2)} \cong \frac{3}{2}\left[(1-k_i) \cdot \left(k_v^{(2)} \cdot \bar{v}_H^{(2)} + \left(1-k_v^{(2)}\right) \cdot \bar{v}_L^{(2)}\right) \cdot \bar{i}^{(2)}\right]$$

Hence with reference to the schematic diagram shown in Fig. 4.2, individual modulation indexes of the inverters (H and L) of two three-phase windings {1} and {2} can be defined as:

$$m^{(1)} = \frac{\sqrt{3}}{2}\frac{\bar{v}^{(1)}}{V_{dc}}; m_H^{(1)} = \sqrt{3}\frac{\bar{v}_H^{(1)}}{V_{dc}}; m_L^{(1)} = \sqrt{3}\frac{\bar{v}_L^{(1)}}{V_{dc}} \cdot \tag{14}$$

$$m^{(2)} = \frac{\sqrt{3}}{2}\frac{\bar{v}^{(2)}}{V_{dc}}; m_H^{(2)} = \sqrt{3}\frac{\bar{v}_H^{(2)}}{V_{dc}}; m_L^{(2)} = \sqrt{3}\frac{\bar{v}_L^{(2)}}{V_{dc}} \cdot \tag{15}$$

From Fig. 4.4, being $2/\sqrt{3}V_{dc}$ and $1/\sqrt{3}V_{dc}$ the maximum amplitude of sinusoidal balanced output voltages for dual three-phase inverters and single three-phase inverters, respectively [42]. Introducing the definition of current, voltage ratios k_i, $k_v^{(1)}$, and $k_v^{(2)}$, by taking account Eqs. 14 and Eqs. 15 the relationships among individual modulation indices of four VSIs can be determined as follows:

$$m_H^{(1)} = 2m^{(1)} k_i \cdot k_v^{(1)}, \; m_L^{(1)} = 2m^{(1)} k_i \cdot (1-k_v^{(1)}) . \tag{16}$$

$$m_H^{(2)} = 2m^{(2)} (1-k_i) \cdot k_v^{(2)}, \; m_L^{(2)} = 2m^{(2)} (1-k_i) \cdot (1-k_v^{(2)}) . \tag{17}$$

With reference to Eqs. 4 based on inverse three-phase space vector decomposition and taking into account Eqs. 9 and Eqs.10, leads to frame an open-loop control scheme for the modulation of quad-inverter configuration and clearly emphasized with block diagram shown in Fig. 4.5. Note that modulation index of the quad-inverter can determined by arbitrary rotating vector in d_1-q_1 and d_5-q_5 planes in synchronous frame. The reference voltage vectors for two three-phase dual-inverter are derived by converting the synchronous frame to stationary reference frame, then by introducing the inverse three-phase decomposition expression to obtain vector $\bar{v}^{(1)}$ and $\bar{v}^{(2)}$, where ϑ determines the fundamental frequency of the output voltages.

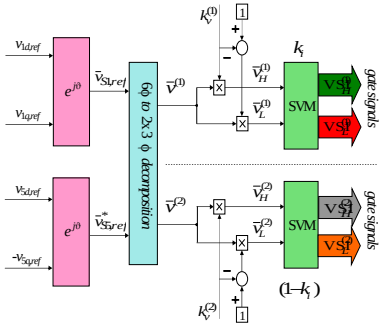


Fig. 4.5: Block diagram of the proposed inverse three-phase space vector decomposition approach with power sharing capability regulation scheme for quad-inverter system.

Then, by adopting proper scaling of voltage, and current sharing coefficients the individual reference voltage vectors of each single inverter's ($\bar{v}_H^{(1)}$, $\bar{v}_L^{(1)}$) and ($\bar{v}_H^{(2)}$, $\bar{v}_L^{(2)}$) can be determined.

Eqs. 16 and Eqs. 17 along with control scheme shown in Fig. 4.5 will be used for the implementation in numerical simulation and also later for experimental investigations. In the next section, redundancy of the quad-inverter is discussed under some possible failure conditions with theoretical development to exploit the performances.

4.5 Fault-tolerance capabilities

The proposed quad-inverter posses the property of phase redundancy under emergency conditions and operable with one, two or three VSI completely suffered with failure. Condition pertains that if one VSI fail the total power of quad-inverter system reduced to half and loss of multilevel operation with available dc sources, could be the drawback but price of operating in degraded mode for its performances as standard two-level with available inverters. To characterize the performance by the following expressions with total power of the converter under healthy state with full rated power can be given by:

$$P = P^{(1)} + P^{(2)} = \frac{3}{2}\left[\left(\bar{v}_H^{(1)} + \bar{v}_L^{(1)}\right) \cdot \bar{i}^{(1)} + \left(\bar{v}_H^{(2)} + \bar{v}_L^{(2)}\right) \cdot \bar{i}^{(2)} \right] \rightarrow 100\% \tag{18}$$

As illustrate before and suppose $VSI_L^{(1)}$ suffered with severer failure, then the power expression of the converter system will be reduced to:

$$P = P^{(1)} + P^{(2)} = \frac{3}{2}\left[\left(\bar{v}_H^{(1)}\right) \cdot \bar{i}^{(1)} + \left(\bar{v}_H^{(2)} + \bar{v}_L^{(2)}\right) \cdot \bar{i}^{(2)} \right] \rightarrow 50\% \tag{19}$$

Switch utility ratio under this condition can be given by:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{18 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot 3 \cdot V_{dc} \cdot I}{18 \cdot V_{dc} \cdot I} = 0.204 \quad (20)$$

Under the circumstances if $VSI_H^{(2)}$ and $VSI_L^{(2)}$ suffered with severer failure condition, taken in account under this condition dual-inverter {1} can provide multilevel waveform, and then the power expression under this situation is given by:

$$P = P^{(1)} = \frac{3}{2}\left[\left(\bar{v}_H^{(1)} + \bar{v}_L^{(1)}\right) \cdot \bar{i}^{(1)}\right] \rightarrow 50\% \quad (21)$$

Switch utility ratio for this condition can be given by:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{12 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot 2 \cdot V_{dc} \cdot I}{12 \cdot V_{dc} \cdot I} = 0.204 \quad (22)$$

Maximum redundancy operation of proposed quad-inverter can be illustrated, if $VSI_H^{(1)}$, $VSI_H^{(2)}$ and $VSI_L^{(2)}$ suffered with severer failure condition, then the power expression further reduced and given by:

$$P = P^{(1)} = \frac{3}{2}\left[\left(\bar{v}_H^{(1)}\right) \cdot \bar{i}^{(1)}\right] \rightarrow 25\% \quad (23)$$

Switch utility ratio for this condition can be given by:

$$SUR = \frac{S_C}{N \cdot V_{SW} \cdot I_{SW}} = \frac{3VI}{6 \cdot V_{SW} \cdot I_{SW}} = \frac{3 \cdot 0.408 \cdot V_{dc} \cdot I}{6 \cdot V_{dc} \cdot I} = 0.204 \quad (24)$$

Eqs. 20, Eqs. 22, Eqs. 24 show the switch utility factor has no effect on reducing the switch configuration when all the dc sources with balanced conditions. Based on above expressions the fault tolerance capabilities are intensively investigated when the proposed quad-inverter fed to ac induction motor in later chapters, provided with both numerical simulation and experimental results to show effectiveness of the quad- inverter more suitably applicable for multiphase ac motor. In the next section, some carrier based modulation for quad-inverter is discussed.

4.6 Carrier based PWM techniques for quad-inverter

Pulse width modulations (PWM) based on carrier approach are more simple and easy to implement in real time processor with FPGA, but like DSP, not more than three-levels else with one carriers could be possible. Switching states of inverter legs relates to the comparison between modulating reference signal with the carrier signal. Where modulating reference signal provides the information on output voltage and carrier signal provides the information on switching period of inverter legs.

The proposed quad-inverter system was derived from two three-phase dual-inverter, hence quad-inverter stands between the simplest two-level and multilevel inverters that more complex, the carrier-based modulation

methods can be adopted both by extending two-level methods (independent two-level space vector modulation) or applying true multilevel methods, such are level-shifted and phase-shifted modulation are discussed below with implementation in PLECS numerical simulation software working with MATLAB environments [121].

4.6.1 Independent modulation

Modulation technique method is the direct extension of standard two-level sinusoidal pulse width modulation (SPWM) with third-harmonic injection to the reference sinusoidal signals. This modulation leads the quad-inverter system each single inverter's (H and L) are modulated as two-level standard modulation. The modulation reference voltage of quad-inverter can be expressed as:

$$\begin{cases} \bar{v}_H^{(1)} = \bar{v}^{(1)}/2 \\ \bar{v}_L^{(1)} = -\bar{v}^{(1)}/2 \end{cases} \Rightarrow \{1\}$$
$$\begin{cases} \bar{v}_H^{(2)} = \bar{v}^{(2)}/2 \\ \bar{v}_L^{(2)} = -\bar{v}^{(2)}/2 \end{cases} \Rightarrow \{2\} \qquad (22)$$

$$\begin{cases} v_1^{(1)} = v_1^{(1)} - \left(\max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\} + \max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\}\right)/2 \\ v_2^{(1)} = v_2^{(1)} - \left(\max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\} + \max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\}\right)/2 \\ v_3^{(1)} = v_3^{(1)} - \left(\max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\} + \max\left\{v_1^{(1)}, v_2^{(1)}, v_3^{(1)}\right\}\right)/2 \end{cases} \Rightarrow \{1\}$$
$$\begin{cases} v_1^{(2)} = v_1^{(2)} - \left(\max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\} + \max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\}\right)/2 \\ v_2^{(2)} = v_2^{(2)} - \left(\max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\} + \max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\}\right)/2 \\ v_3^{(2)} = v_3^{(2)} - \left(\max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\} + \max\left\{v_1^{(2)}, v_2^{(2)}, v_3^{(2)}\right\}\right)/2 \end{cases} \Rightarrow \{2\} \qquad (23)$$

Numerical simulation implementation of the PWM scheme for single inverter $H^{(1)}$ shown in Fig. 4.6a and switching pattern in theoretical representation depicted in Fig. 4.6b.

Fig. 4.7 shows the voltages of first-phase of two three-phase winding {1} (top: purple trace) and {2} (bottom: turquoise trace) and it can be notify there is large excursion from maximum to minimal voltage level results in improper multilevel waveforms. The vectors $\bar{v}_{oH}^{(1)}$, $\bar{v}_{oH}^{(2)}$, and $\bar{v}_{oL}^{(1)}$, $\bar{v}_{oL}^{(2)}$ overlaps at the beginning and the end of the switching period, thus forming the total zero vector $\bar{v}_o^{(1)}$, $\bar{v}_o^{(2)}$ even for a relatively large modulating index values.

Simple modulation method and having large degree of freedom most suitable for two-level single inverters. The voltage references can be given independently regarding both amplitude and phase (within available dc

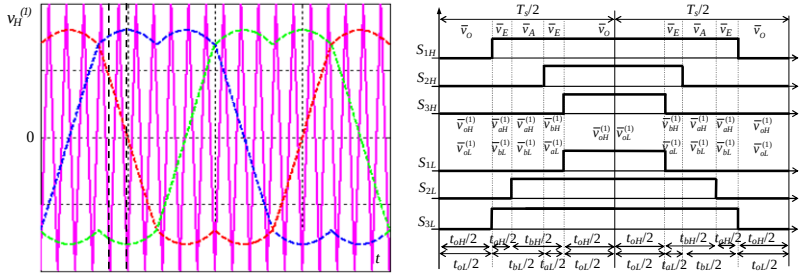


Fig. 4.6: Independent modulation $m^{(1)} = m^{(1)} = 0.75$, f_s=1KHz. (a) Modulation signals for single inverter $H^{(1)}$ of the three-phase open-winding {1}. (b) Switching pattern.

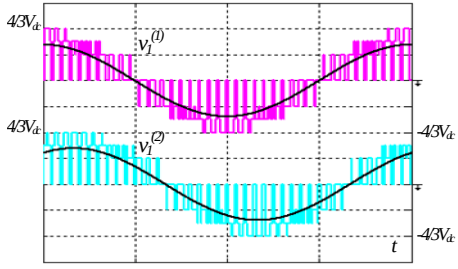


Fig. 4.7: First-phase output voltages with time scaled average components of two three-phase open-winding loads: top-trace: dual-inverter {1}; bottom -trace: dual-inverter {2}. [100V/div].

voltage limits) [45]. This approach has been proposed for automotive applications [68-69], setting one inverter to supply only active power whereas the other provides necessary reactive power for the drive. As a benefit, only one supply can be used since inverter providing reactive power does not need dc source.

4.6.2 Level-shifted modulation

Level-shifted pulse width modulation is a general principle applied to all multilevel inverters in general, where for *l*-levels there are (*l*-1) carriers shifted by *l*/(*l*-1) of the V_{dc}, so each carrier occupies its own trace. Common modulation signals passes gradually to every carrier and in this way modulates corresponding part of the multilevel inverter, while all lower switches are on and higher are off.

In practical implementation (e.g. DSP) it is more convenient to produced level-shifted modulating signals and use common carrier. With respect to Fig. 2.11 and section 2.3.1 in chapter 2, modulating signal $v_1^{(1)}$, $v_1^{(2)}$ of the ($1H^{(1)}$, $1L^{(1)}$) and ($1H^{(2)}$,$1L^{(2)}$)-legs switches will be determined taking into account that leg voltage $v_{1N}^{(1)}$, $v_{1N}^{(2)}$ is always negative:

$$\begin{cases} v_{1N}^{(1)}; v_{1M}^{(1)} \in \left[v_H^{(1)}, 0 \right] \\ v_{1N}^{(2)}; v_{1M}^{(2)} \in \left[v_H^{(2)}, 0 \right] \end{cases} \tag{24}$$

To obtain the positive values only way for $v_1^{(1)}$, $v_1^{(2)}$ is:

$$\begin{cases} v_{1N}^{(1)}; v_{1M}^{(1)} \in \left[0, -v_L^{(1)} \right] \\ v_{1N}^{(2)}; v_{1M}^{(2)} \in \left[0, -v_L^{(2)} \right] \end{cases} \tag{24}$$

Therefore, for given voltage reference the obtained leg voltages need to be:

$$\begin{aligned} \left(v_{1N}^{(1)}, v_{1M}^{(1)} \right) &= \begin{cases} \left(0, -v_L^{(1)} \right), v_1^{(1)} > 0 \\ \left(v_H^{(1)}, 0 \right), v_1^{(1)} < 0 \end{cases} \\ \left(v_{1N}^{(2)}, v_{1M}^{(2)} \right) &= \begin{cases} \left(0, -v_L^{(2)} \right), v_1^{(2)} > 0 \\ \left(v_H^{(2)}, 0 \right), v_1^{(2)} < 0 \end{cases} \end{aligned} \tag{25}$$

The modulation can be achieved by using common triangular carrier and references:

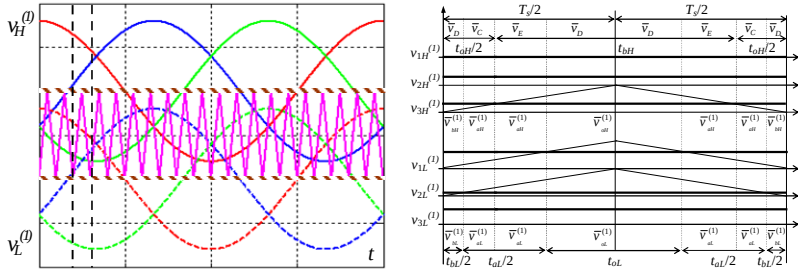
$$\begin{aligned} &\begin{cases} \bar{v}_H^{(1)} = m^{(1)} V_{dc} \cos(\theta - \pi) - V_{dc}/2 \\ \bar{v}_L^{(1)} = m^{(1)} V_{dc} \cos\theta - V_{dc}/2 \end{cases} \Rightarrow \{1\} \\ &\begin{cases} \bar{v}_H^{(2)} = m^{(2)} V_{dc} \cos(\theta - 5\pi/6) - V_{dc}/2 \\ \bar{v}_L^{(2)} = m^{(2)} V_{dc} \cos(\theta + \pi/6) - V_{dc}/2 \end{cases} \Rightarrow \{2\} \end{aligned} \tag{26}$$

Numerical simulation implementation of the level-shifted PWM scheme for dual-inverter {1} shown in Fig. 4.8a and switching pattern in theoretical representation depicted in Fig. 4.8b (OCD triangle). Due to the symmetry, analogous way valid for the remaining modulating signals $v_2^{(1)}$, $v_3^{(1)}$,and $v_2^{(2)}$, $v_3^{(2)}$ of ($2H^{(1)}$, $2L^{(1)}$), ($3H^{(1)}$, $3L^{(1)}$)and ($2H^{(2)}$, $2L^{(2)}$), ($3H^{(2)}$, $3L^{(2)}$) of the phases respectively.

Fig. 4.8 shows the resulting proper multilevel voltages of first-phase of two three-phase winding {1} (top: purple trace) and {2} (bottom: turquoise trace). Note that inverter ($H^{(1)}$, $H^{(2)}$), applies all three NTVs ($\bar{v}_{aH}^{(1)}$, $\bar{v}_{bH}^{(1)}$, $\bar{v}_{oH}^{(1)}$) and ($\bar{v}_{aH}^{(2)}$, $\bar{v}_{bH}^{(2)}$, $\bar{v}_{oH}^{(2)}$), whereas inverter ($L^{(1)}$, $L^{(2)}$), just ($\bar{v}_{bL}^{(1)}$, $\bar{v}_{oL}^{(1)}$) and ($\bar{v}_{bL}^{(2)}$, $\bar{v}_{oL}^{(2)}$). Meanwhile that period averaged vectors ($\bar{v}_H^{(1)}$, $\bar{v}_L^{(1)}$) and ($\bar{v}_H^{(2)}$, $\bar{v}_L^{(2)}$) cannot be collinear as shown in Fig. 4.3c.

4.6.3 Phase-shifted carrier modulation

Phase-shifted modulation is similar to previous method but the carriers



(a) (b)

Fig. 4.8: Level-shifted modulation $m^{(1)} = m^{(1)} = 0.75$, f_s=1KHz. (a) Modulation signals for the three-phase open-winding {1}. (b) Switching pattern.

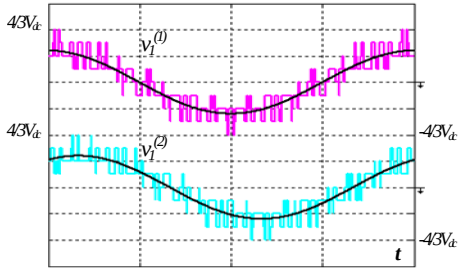


Fig. 4.9: First-phase output voltages with time scaled average components of two three-phase open-winding loads: top-trace: dual-inverter {1}; bottom -trace: dual-inverter {2}. [100V/div].

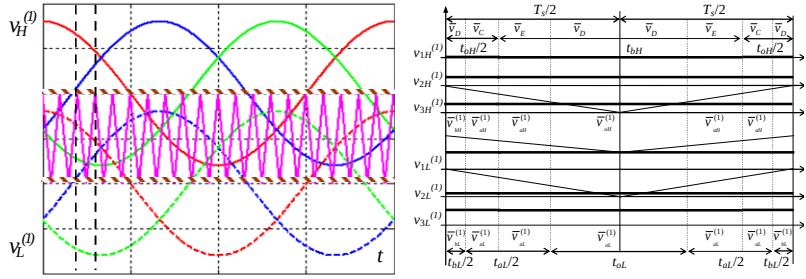
are shifted by 180^0, in phase opposition to the level-shifted PWM. Phase-shifted modulation is based on the harmonic analysis of PWM signals, the principle of the method is to phase shift carrier by $2\pi/(l\text{-}1)$, where l is the number of voltage levels by each leg.

Using harmonic result for single two-level inverter:

$$v(\theta_r,\theta_c) = \frac{E}{2} m\cos\theta_f + \frac{E}{\pi}\sum_{c=1}^{\infty}\frac{1}{c}(\cos c\pi - J_0(c\pi m))\sin c\theta_c + \frac{E}{\pi}\sum_{c=1}^{\infty}\sum_{\substack{f=-\infty \\ f\neq 0}}^{\infty} J_f(c\pi m)\sin\left(f\frac{\pi}{2} - (c\theta_c + f\theta_f)\right) \quad (27)$$

Numerical simulation implementation of the phase-shifted PWM scheme for dual-inverter {1} shown in Fig. 4.10a and switching pattern in theoretical representation depicted in Fig. 4.10b (ACE triangle). Fig. 4.11 shows the resulting proper multilevel voltages of first-phase of two three-phase winding {1} (top: purple trace) and {2} (bottom: turquoise trace).

Fig. 2.11 and section 2.3.1 in chapter 2, the output voltage expression it is possible to set phase shift in order to obtain output voltage free of some harmonics that existed in single inverter cases. For example, phase shifted



(a) (b)

Fig. 4.9: Phase-shifted modulation $m^{(1)} = m^{(1)}$=0.75, f_s=1KHz. (a) Modulation signals for the three-phase open-winding {1}. (b) Switching pattern.

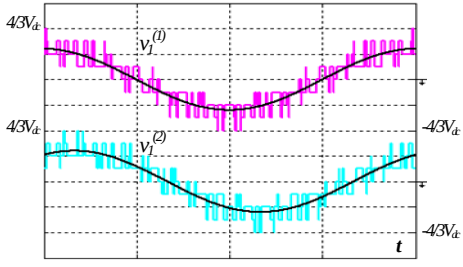


Fig. 4.10: First-phase output voltages with time scaled average components of two three-phase open-winding loads: top-trace: dual-inverter {1}; bottom -trace: dual-inverter {2}. [100V/div].

by 180^0, (phase opposition [70]) cancels sideband harmonics around even *c* values. However, the harmonic analysis is behind the scope of work, concentration is to obtain proper multilevel waveform rather than this method.

4.7 Conclusion

A new version of multiphase-multilevel inverter was proposed in this chapter with power sharing and redundancy capabilities. The proposed quad-inverter system essentially comprises of four standard 2-level three-phase voltage source inverters with insulated dc source for preventing zero-sequence components in whole system. The conversion system characterized by power sharing among the four VSIs within each switching period with three degree of freedom. Where first one concern with current sharing between two three-phase open-windings {1} and {2}. The second degree of freedom relates to the voltage sharing between inverters (H and L) of the first three-phase winding {1} and whereas third relates to voltage sharing between inverters (H and L) of the second three-phase winding {2}. By adopting proper modified multilevel space vector pulse modulation

(SVPWM), phase voltages across each open-winding can have multi-stepped waveform (maximum 9-levels). Complete theoretical developments are provided to express the voltages output characteristics and fault tolerance performances of the proposed multiphase-multilevel conversion system.

Some carrier based pulse width modulations are performed with quad-inverter system to show its multilevel output waveforms based on developed inverse three-phase space vector decomposition approach in open-loop control scheme. To understand the effectiveness, the quad-inverter system was completely implemented in PLECS numerical simulation software working MATLAB environments and results are provided to match with theoretical aspects. Note that this structure can be easily scalable to higher number of phases (n=9, 12,) as multiple of three, which in turn can be prominent solution for multiphase ac motors with asymmetrical configuration for later investigations.

5. Quad-inverter configuration for multiphase-multilevel AC motor drive

5.1 Introduction

In this chapter, multiphase ac motor drives and its modeling approaches, control schemes and applications are discussed elaborately from literature survey and proposed a novel multiphase-multilevel ac motor drive system. Control algorithm based on synchronous rotating frame was developed and proposed, which able to generate multilevel voltage waveforms, equivalent to the ones of a 3-level inverter, and to share the total motor power among the four dc sources with in each switching period. Complete model based ac motor drive system has been implemented numerically in software and set of simulation results are provided to show the most effectiveness in symmetrical and asymmetrical power sharing conditions references to the theoretical developments.

5.2 Multiphase AC motor drives

The first record of a multiphase motor drive came to the literatures view in back to 1969, as five-phase voltage source inverter (VSI) fed induction motor was proposed and given by [71]. In particular, multiphase motor drives is advantageous over the traditional three-phase motors, by reducing the amplitude and increasing the frequency of torque pulsations, lowering the rotor harmonic current losses and lowering the dc link current harmonics. In addition, owing to their redundant structure, multiphase motor drives improve the system reliability and intensively utilized in ac traction systems, electric/hybrid vehicles, high-power pumps and aerospace applications [72-73, 50-51, 58]. Last years, the importance of multiphase drives has considerably grown and more published research works are presented in specific addressing to five-phase and six-phases employing the induction, synchronous permanent magnet or synchronous reluctance motors [72].

Advantages of multiphase machines when compared to three-phase counterparts are valid for all stator winding design with sinusoidal distributions characteristics are [74-78]:

- Fundamental stator currents produce a field with a lower space-harmonic content.
- The frequency of the lower torque ripple components, being proportional to $2n$, increases with number of phases.

Keywords**:** *Multiphase-multilevel ac motor, dual three-phase induction motor, control technique, multiple space vectors, space vector modulation and power sharing.*

- Since two currents is required for flux/torque control of ac machine, regardless of the number of phases, remaining degrees of freedom utilized for other purposes. One such purpose, available only if the machine is with sinusoidal m.m.f distribution, is the independent control of multi-motor multiphase drive system with a single power electronic converter supply.

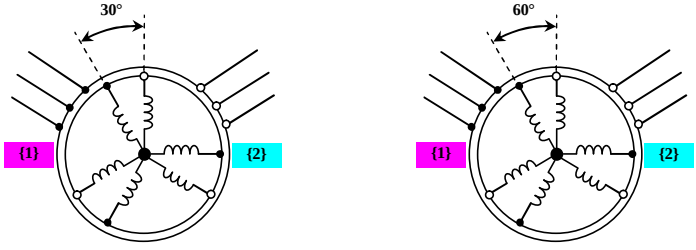
Multiphase motor has greater fault tolerance capabilities than their three-phase counterparts. If one phase of the three-phase induction motor becomes open-circuited the motor becomes single-phase motor, but it may continue to run but need external means of starting for getting revolving flux and must be massively de-rated. If one phase of multiphase motor becomes open-circuited, still continue to run with remaining phases, contributes the revolving flux and with minimal de-ratings.

In next section, a special configuration of multiphase motor was discussed in detail from literature survey and proposed a novel configuration for multiphase ac motor drives.

5.3 Six-phase induction motor

A six-phase induction machine supplied from a six-phase inverter was examined in [79-80]; application by splitting the phase can impose high-current without increasing the voltage per phase. More commonly this machines reported in the literature with different nomenclatures has split-phase, dual-star, double-star, quasi six-phase, or dual three-phase induction motor. Fault tolerance is one of the main reasons behind the application of six-phase motor drives in locomotives [81-82]. It is advantageous, asymmetrical stator winding structure with two three-phase windings spatially shifted by 30° electrical degree and typical configuration shown in Fig. 5.1a.

A traditional three-phase induction motor can generate an electromagnetic torque having a dominant time harmonics of frequency six-times the supply fundamental frequency, when supplied with square-wave either by voltage source inverter (VSI) or current source inverter (CSI). In this situation, dual three-phase induction motor due to the winding configuration results the elimination of all air-gap flux time harmonics significantly and induced rotor current harmonics of order $k=6.n\pm1$, (n=1, 3, 5,….) and all torque harmonic of order $k=6.n$, (n=1, 3, 5,….) are eliminated, significantly improves the torque ripples and the rotor losses are reported experimentally in [79-80, 83]. For a dual three-phase induction motor the torque ripples are reduced by one-half in contrast with the traditional counter part three-phase induction motor are examined in [84].



(a) **(b)**

Fig. 5.1: Dual three-phase induction motor configuration. (a) Asymmetrical. (b) Symmetrical.

Possibility of increasing the torque-per-amperes ratio for the same machine volume using spatial m.m.f forces other than the fundamental component was investigated in [85] for dual three-phase motor and reported almost 40% of the torque density improvement obtained (in comparison to three-phase induction motor with same flux peak value) by injection of third harmonic zero sequence components in the phase currents and this was achieved by connecting the machine winding neutral points to the midpoint of the inverter dc link.

Investigation on speed variation by modifying the number of machine pole-pair, when the supply frequency kept constant and extend to the constant power operation for dual three-phase induction machine having 60° electrical displacement between stator sets (true six-phase machine) with advantage of reduction in acoustic noise and ripple current are addressed in [86-87] and configuration shown in Fig. 5.1b. For high-power application, two dual three-phase induction machines supplied by a single VSI with appropriate series connection of the stator winding of these two machines reported in [87]. In the next section, different modeling based approaches addressing to this ac machine was discussed from literatures.

5.3.1 Six-phase asymmetrical induction motor modeling approaches

Construction principle of a dual three-phase induction motor is similar to a conventional three-phase induction motor, having the same rotor, magnetic core but the stator windings are split into two three-phase windings. In literatures there are different mathematical modeling approaches of dual three-phase induction motor usually obtained by the following assumptions:

- Sinusoidally distributed winding configuration.
- Unity stator and rotor turns ratio, constant air-gap.
- Magnetic saturation and core losses are neglected.

Also, modeling considering the m.m.f spatial harmonics as for pole-changing control examined in [86-87]. Different modeling methods reported in [83, 53, 88-89] and more recently a novel method based on three-phase space vector decomposition approach was reported in [52] and its six-phase orthogonal transformation techniques are clearly explained in detail chapter 3:

- Vector Space Decomposition Theory (VSD).
- Dual Three-Phase Modeling Theory (DTP).
- Three-Phase Space Vector Decomposition Approach.

The VSD theory was introduced for transform the original six-dimensional space of the machine into three two-dimensional orthogonal sub-spaces by using proper [6x6] transformation matrix reported first time in [53, 88] with power invariant form and non-power invariant form [89]. Machine modeling approach based on [52] as the same advantages [53] and more simplified form stated in the literatures, equivalent circuit and orthogonal sub-spaces are show in Fig. 5.2.

- The fundamental components of the machine variables and the harmonics of the order k=6.n±1, (n=0, 2, 4…) are mapped in the first sub-space. There components contributes the air-gap flux for the machine (Fig. 5.2.a).
- The harmonics of order k=6.n±1, (n=1, 3, 5…) are mapped in the

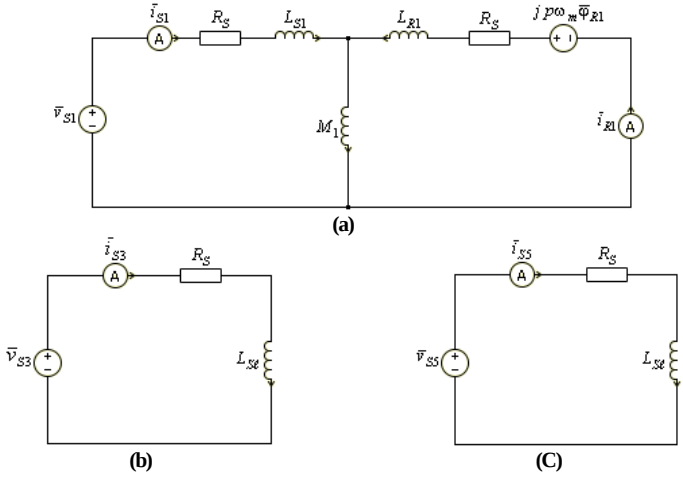


Fig. 5.2: Dual three-phase induction motor equivalent circuit in terms of stationary reference frame (α, β). (a) First (b) Third and (c) Fifth sub-spaces. Based on [53].

fifth sub-space, which orthogonal to the first sub-space and hence do not contribute the air-gap flux (Fig. 5.2.b).

- The homo-polar components or zero-sequences components of order $k=3.n$, (n=0, 1, 2, 3…) are mapped in the third sub-space (Fig. 5.2.c).

Hence from the point of view flux/torque production, the analysis and control of machine being simplified, since machine model is identical to the model of the three-phase machine. If the two stator winding sets had isolated neutral points, no current components flow in third sub-space, consequently the machine model referred to the stationary reference frame reduced to first and fifth sub-spaces. To utilize the above benefit in this chapter, the proposed novel ac motor drive was modeled based on three-phase space vector decomposition approach [52] and transformation details already discussed in chapter 3.

Another approach based on modified VSD for short-pitch machine, taking into consideration the mutual leakage inductance, presented in [90] and leakage inductance values for the first, fifth and third sub-space circuits are different and full-pitch coils maximize the impedance in the fifth and third sub-spaces and applicable better for inverter fed operations, testing performances for the machine leakage inductances are reported in [90]. Modeling based on DTP approach was first reported in [83], the magnetizing inductance and the rotor parameters are to be one-half respect to be equivalent to VSD or three-phase space vector decomposition approach and complete description of the DTP machine state-space model in synchronous reference frame aligned to the rotor flux are reported in [91]. However, if the star connection is used and the neutral points of the two stator sets are connected, the zero-sequence current will be automatically nullify even when the two sets of supply voltages have zero-sequence components. In the next section, various control aspects for this machine were discussed from reporting literatures.

5.3.2 Six-phase asymmetrical induction motor control schemes (State-of-art-in research)

In literatures, the control aspect of dual three-phase induction motor are mainly dedicated to the vector control techniques (field oriented and/or direct torque control) with less interest is devoted towards scalar control [92]. Vector control schemes for the asymmetrical six-phase induction motor with sinusoidally distributed windings, obtained by referring the α, β (stationary reference frame) machine model as in Fig. 5.2 to a rotating d-q reference frame normally aligned with rotor flux [50, 92].

An indirect rotor FOC scheme was presented in [93], however for application requires high fundamental frequencies and/or when the speed sensor does not provide sufficient accuracy of rotor position, direct rotor field oriented control (DRFOC) is usually preferred [89]. The rotating *d-q* reference frame is aligned with the rotor flux space vector whose magnitude ψ_r and position φ_r are provided by a flux estimator, as shown in Fig. 5.3 [50, 92]. The flux estimation required for field orientation is based on either VSD or three-phase space vector decomposition approaches, the FOC scheme adopts the flux estimators normally employed for the three-phase induction machines since the α, β machine model is identical to the model of a three-phase machine. In contrast to this, the extension of current control strategies from the three-phase to the asymmetrical six-phase drive is less straightforward since it must consider some machine-specific aspects. In particular, small inherent asymmetries between the two three-phase power sections can lead to current imbalance between the two stator winding sets, as provided by [85, 89, 92]. This problem can appear when the machine is supplied from two independent three-phase inverters, a natural choice for industry applications. In such a case the scheme with only two current controllers as shown in Fig. 5.12, cannot guarantees a satisfactory performance.

In principle current control aspect are implemented either in stationary reference or in synchronous reference frame, depending on the required current control performance for the considered specific applications. However, a minimum of four current controller (assuming isolated neutral points) is necessary [50]. A DRFOC scheme, based on DTP machine modeling, is discussed in [94] in conjunction with a GTO inverter-fed high-power machine. The current control uses a double *d-q* reference frame approach (i.e. two pairs of *d-q* reference current controllers) to simultaneously control the flux-producing stator current and the torque-producing components that correspond to the two three-phase stator winding sets. A decoupling scheme for current regulation based machine's

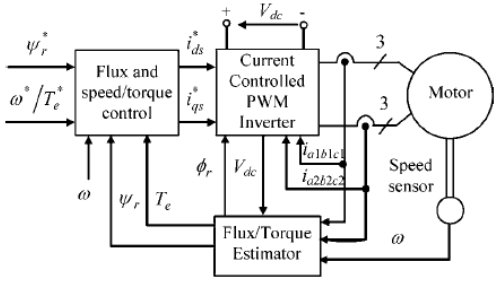


Fig. 5.3: DRFOC scheme for asymmetrical six-phase induction machine.

state-space model, proposed in [89]. Another DRFOC scheme, based on the VSD theory (which gives simpler rotor flux estimation) and also using *d-q* reference current control are examined in [89], while a comparison of different *d-q* synchronous reference frame current regulation schemes is available in [91].

The basic double *d-q* reference current control scheme shown in Fig. 5.4, when the neutral points of the two three-phase stator sets are connected, the control scheme must be complemented with additional PI current regulator since the system order increases from 4 to 5, as described in [85]. The double *d-q* reference frame current control for the asymmetrical six-phase drives has the disadvantage of the multiple speed-dependent coupling terms, which have to be compensated [91]. For this reasons, a straight forward current control scheme in stationary α, β reference frame has been proposed in [95]. This scheme shown in Fig. 5.5 does not require coupling circuits and it is able to cope with the current imbalance between the two three-phase stator winding sets. The α, β current components are regulated by means of a stationary reference frame regulator being equivalent to a PI regulator in the *d-q* reference frame. If there is some imbalance and only α, β current controllers are utilized, fundamental current components appear in first sub-space [50]. These components can be forced towards zero (thus canceling the current imbalance) by two resonant regulators tuned on the fundamental frequency and controlling the first sub-space current components. This scheme requires online electrical angular speed estimation; that can be done for example, by means of a phase-locked loop scheme (PLL) [95].

Other control aspect are dedicated direct torque control (DTC) to get fast, decoupled control of the stator flux and the electromagnetic torque without inner current control loops [96]. From literature survey, the DTC solutions for the three-phase machines can be divided into two main groups:

- Direct Self-Control (DSC) and Switching-Table based DTC (ST-DTC) techniques; these solutions give variable switching frequency.
- Pulse Width Modulation based DTC (PWM-DTC) techniques; these solutions provide constant inverter switching frequency.

The DSC and ST-DTC schemes are extended for dual three-phase drives [96-98], considering the larger number of non-zero voltage vectors that can be provided by the six-phase inverters. General consideration is that lack of current control imposes a dedicated design of the drive power units in order to avoid unbalanced current sharing between two three-phase stator sets

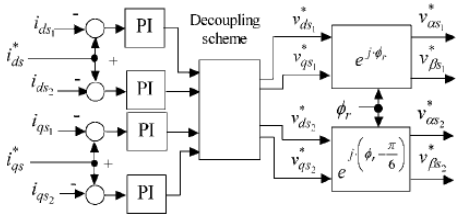


Fig. 5.4: Double (*d*, *q*) synchronous frame current control scheme for asymmetrical six-phase induction machine.

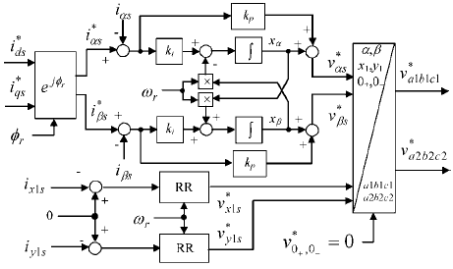


Fig. 5.5: Stationary reference frame current control scheme for asymmetrical six-phase induction machine.

[99]. The basic DSC scheme for dual three-phase induction motor drives is shown in Fig. 5.6. By using the voltage vectors corresponding to the external layer of the 12-side polygon in the first sub-space, the DSC imposes a 12-side polygon trajectory of the stator flux.

However, that is achieved by generating 5th and 7th voltage harmonics; these voltages will produce large current harmonics in the fifth sub-space, as shown by the numerical simulation results of a DSC scheme described in [99]. That will result in the increase of size and cost of both machine and inverter. However, the DSC strategy can be used in high-power, low

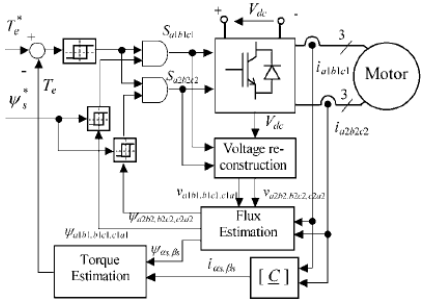


Fig. 5.6: Direct self-control (DSC) scheme for asymmetrical six-phase induction machine.

switching frequency applications, such as traction drives [100].

In ST-DTC basic scheme for dual three-phase induction motor drives is shown in Fig. 5.7, based on estimated stator flux position, a torque three-level hysteresis regulator and a flux two-level regulator are used to generate the inverter switching functions through an optimal switching table. The key issue for ST-DTC is the ST design order to get sinusoidal machine phase current, by minimizing the current components in the fifth sub-space. Different ST design solutions are discussed and experimented in [101] with good torque and flux regulation performance but with some problems regarding the phase currents distortion. Other ST-DTC strategies, involving voltage vectors from internal layers of the 12-side polygon in the first sub-space have been numerically tested and simulation result provided by [102].

In several applications such as EV, it is preferred to have constant switching frequency to obtain quasi sinusoidal phase using PWM operation. The problem of phase current distortion can only be completely solved for the asymmetrical six-phase machine by keeping the switching frequency constant and imposing the direct mean torque control approach. In such case, an average stator voltage command vector over a sampling period must be computed, to get the required stator flux and electromagnetic torque. The basic PWM-DTC scheme for dual three-phase induction motor drives is shown in Fig. 5.8 [50]. Predictive PWM-DTC schemes, using the VSD theory for machine modeling proposed in [34] and obtain sinusoidal machine currents. The algorithm has been implemented in stator flux oriented reference frame. Another PWM-DTC scheme based on VSD theory is presented in [103], where voltage vector reference is obtained through simple PI regulators implemented in the stator flux oriented reference frame. The stator flux is estimated by means of a full-order Luenberger observer, which provides also stator current estimation. The estimated currents (that are less noisy than the real ones) are used to successfully compensate the inverter dead-time effects, improving significantly the drive performance at very low-speed [103].

To conclude the state-of-art-in research for six-phase asymmetrical induction motor, the majority of the available work deals with the development of control schemes starting from the well-known three-phase solutions. The transition from three-phase to asymmetrical six-phase machine control requires more dedicated solutions and this is well recognized nowadays. In particular, to avoid possible stator current distortion and unbalanced current sharing between the two stator three-phase winding sets, specific approaches regarding machine modeling, inverter modulation techniques in specific to six-phase VSI (discussed in

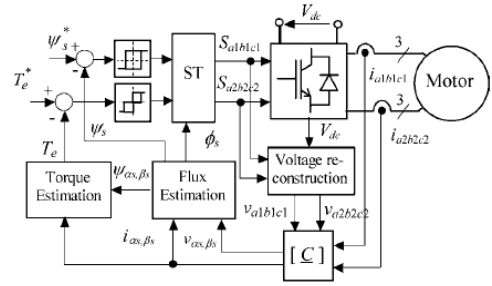


Fig. 5.7: Switching-able based direct torque control (ST-DTC) scheme for asymmetrical six-phase induction machine.

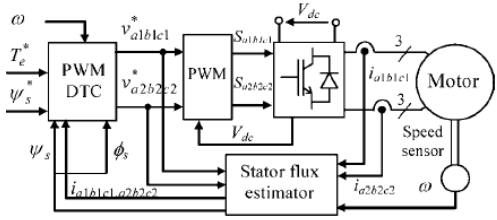


Fig. 5.8: PWM based direct torque control (PWM-DTC) scheme for asymmetrical six-phase induction machine.

detail chapter 4), current control schemes have been developed and experimental results are reported in several published literature works.

No more novel realizable with three-phase machines and therefore specific only to multiphase drives, are related to the employment of asymmetrical six-phase machines in particular application such as single-inverter two-motor drives with independent control [104] and dual-source motor drives [105]. In the later case, two three-phase inverters with separate dc links supply an asymmetrical six-phase machine. This drive topology allows the addition, directly at the machine level of the power generated by independent dc voltage sources without employing additional dc-dc converters. In this case, different amounts of power can be drawn from the two independent dc links, depending on the working conditions and the rated power of these two sources [105]. Endings of asymmetrical six-phase induction motor, by keeping stator windings deliberately open rather than connected into star-points, resulting structure so called open-end winding configuration. This enables supply of the machine's stator winding from both sides and requires two asymmetrical six-phase VSIs. Advantage of such solution is that suppression of low-order voltage harmonics becomes relatively easy. Perspective application, such topology large relay on control algorithm modification and post-fault conditions when one or two inverters

fails still operable with healthy inverters. Finally, there is lack of significant work related to the power balancing of six-phase asymmetrical induction motor with unbalanced voltage and/or current operating conditions. In the next section, this research work devoted for the possible solution in focusing power balancing of proposed a novel multiphase-multilevel ac motor drive system.

5.4 Proposed novel multiphase-multilevel AC motor

A novel dual three-phase induction motor with open-end winding configuration (asymmetric six-phase induction machine) has been proposed in this section. This configuration can easily derived from a three-phase induction machine by splitting the phase into two set of windings, having spatially shifted by 30° electrical angle (windings{1} and {2}) and keeping deliberately open-end stator windings, typical schematic layout is shown in Fig. 5.9.

5.4.1 Quad-inverter based six-phase open-end winding induction motor

In order to exploit all the previous illustrated advantages discussed in chapter 4 and section [5.2-5.3], the usage of multiphase inverters together with multiphase ac machines becomes an effective method to group and to obtain high-power ratings with low-voltage- and current-limited devices. Several conversion structures have been introduced in last decades for multiphase and multilevel inverters. Among these structures, there are topologies based on a proper arrangement of conventional 2-level three-phase voltage source inverters (VSIs) to realize both multiphase [52-53], [92, 104, 106] and multilevel inverters [107-109, 68, 42].

A novel quad-inverter (discussed in chapter 4) based dual three-phase induction motor with open-end stator winding configuration has been proposed in this section. The power supply consists of four standard 2-level three-phase VSIs having insulated dc sources to prevent circulation of zero-

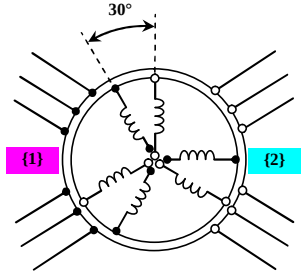


Fig. 5.9: Dual three-phase asymmetrical induction motor with open-winding configuration.

sequence components in the whole system. A schematic diagram of entire ac drive shown in Fig. 5.10 and equivalent circuit in terms of three-phase space vectors representation given by Fig. 5.11. Note that the structure is easy scalable to nine, twelve or higher number of phases multiple of three. An original modulation strategy has been proposed to regulate each couple of 2-level VSIs such as a 3-level inverter, providing proper multilevel voltage waveforms for each three-phase stator windings. Further, the proposed synchronous reference frame control algorithm allows the total motor power to be shared among the four dc sources with three degrees of freedom, leading to a combination/extension of the power sharing principles given in [105, 42].

Advantages of proposed multiphase-multilevel ac drives include:

- Possibility to quad-rippling the power capability with four conventional two-level inverters and suppressing low-order voltage harmonics becomes relatively easy.
- Highly reliable under post-fault conditions due to redundant structure with optimal degrading.

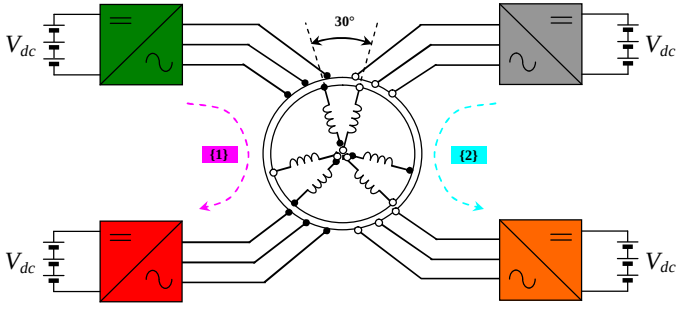


Fig. 5.10: Schematic diagram of the proposed multiphase-multilevel ac motor drive consisting in four 2-level VSIs supplying a dual three-phase motor with open-end windings.

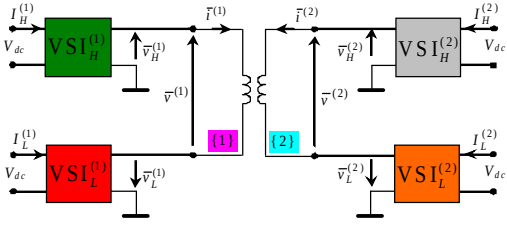


Fig. 5.11: Equivalent circuit of the whole multiphase-multilevel ac motor drives in terms of three-phase space vectors.

5.4.2 Modeling of machine based on multiple space vector

The behavior of the dual three-phase induction machine having sinusoidal distributed stator windings can be described in terms of multiple space vectors (three-space vector decomposition approach provided by chapter 3) by the following equations, written in a stationary reference frame based on section 5.3.1 (Fig. 5.2):

$$\bar{v}_{S1} = R_S \bar{i}_{S1} + \frac{d\bar{\varphi}_{S1}}{dt}, \bar{\varphi}_{S1} = L_{S1} \bar{i}_{S1} + M_1 \bar{i}_{R1}, \quad (1)$$

$$0 = R_R \bar{i}_{R1} - j p \omega_m \bar{\varphi}_{R1} + \frac{d\bar{\varphi}_{R1}}{dt}, \bar{\varphi}_{R1} = M_1 \bar{i}_{S1} + L_{R1} \bar{i}_{R1}, \quad (2)$$

$$\bar{v}_{S5} = R_S \bar{i}_{S5} + \frac{d\bar{\varphi}_{S5}}{dt}, \bar{\varphi}_{S5} = L_{S\ell} \bar{i}_{S5}, \quad (3)$$

$$T = 3 p M_1 \bar{i}_{S1} \cdot j \bar{i}_{R1}, \quad (4)$$

where p is the pole pair's number, ω_m is the rotor angular speed, and the subscripts S and R denote stator and rotor quantities, respectively. It should be noted that $\bar{i}_{S1}$ and $\bar{i}_{R1}$ are responsible for the sinusoidal spatial distribution of the magnetic field in the air gap, whereas $\bar{i}_{S5}$ does not contribute to the air gap field.

5.4.3 Synchronous frame control scheme

In dual three-phase induction motor drives, the reference values of the d_1-q_1 components of the stator currents in a synchronous reference frame, $i_{1d,ref}$ and $i_{1q,ref}$, are determined on the basis of flux and torque commands, respectively [92]. The d-axis of synchronous reference frame is aligned with the rotor flux, displaced by angle ϑ with respect to the d-axis stationary reference frame. Then, the reference values of the stator voltage space vectors in a stationary reference frame, $\bar{v}_{S1,ref}$ and $\bar{v}_{S5,ref}$ can be determined by the typical block diagram represented in Fig. 5.12. Note that the condition $\bar{v}_{S5,ref} = 0$ leads to balanced power sharing between the two three-phase stator windings.

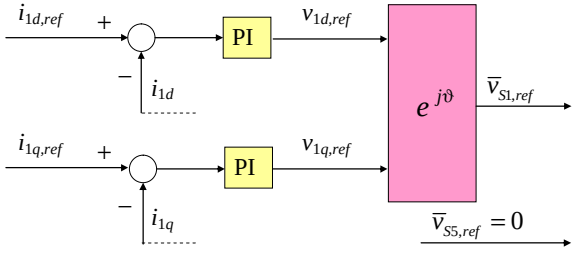


Fig. 5.12: Block diagram of a typical current controller in the synchronous reference frame for dual three-phase induction motor drives.

5.5 Power sharing management

In the proposed system, the power sharing among the four dc sources is characterized by three degrees of freedom. First one concern with current sharing between two three-phase open-end stator windings {1} and {2}. The second degree of freedom relates to the voltage sharing between single inverter's ($H^{(1)}$ and $L^{(1)}$) of the first three-phase stator winding {1} and where as third relates to voltage sharing between inverters ($H^{(2)}$ and $L^{(2)}$) of the second three-phase stator winding {2}.

5.5.1 Power sharing between two windings {1} and {2}

According to (chapter 3, Eqs. 6), the stator current space vector $\bar{i}_{S1}$, which is determined on the basis of torque and flux demands, can be expressed as:

$$\bar{i}_{S1} = \frac{1}{2}\left(\bar{i}^{(1)} + \alpha \bar{i}^{(2)}\right), \tag{5}$$

In order to minimize the currents in the two three-phase windings, the space vectors $\bar{i}^{(1)}$ and $\alpha\bar{i}^{(2)}$ have to be in phase, therefore the following assumption can be made:

$$\begin{cases} \frac{1}{2}\bar{i}^{(1)} = k_i \bar{i}_{S1} \\ \frac{1}{2}\alpha \bar{i}^{(2)} = (1-k_i)\bar{i}_{S1} \end{cases}, \tag{6}$$

where k_i represents a currents ratio between the windings {1} and {2}. The expressions of $\bar{i}^{(1)}$ and $\bar{i}^{(2)}$ can be readily obtained from Eqs. 6, leading to:

$$\begin{cases} \bar{i}^{(1)} = 2k_i \bar{i}_{S1} \\ \bar{i}^{(2)} = 2(1-k_i)\alpha^{-1}\bar{i}_{S1} \end{cases}, \tag{7}$$

Once the three-phase current space vectors are known, the stator current space vector $\bar{i}^{*}_{S5}$ can be determined by introducing Eqs. 7 in (chapter 3, Eqs. 6):

$$\bar{i}^{*}_{S5} = \frac{1}{2}\left(\bar{i}^{(1)} - \alpha \bar{i}^{(2)}\right) = (2k_i - 1)\bar{i}_{S1}. \tag{8}$$

Rewriting Eqs. 8 in the synchronous reference frame, the relationship in terms of *d-q* components becomes:

$$\begin{cases} i_{5d} = (2k_i - 1)i_{1d} \\ i_{5q} = -(2k_i - 1)i_{1q} \end{cases}. \tag{9}$$

Complete current control algorithm empathized in the block diagram shown in Fig. 5.13 and according to Eqs. 9, the d_5- q_5 components of the reference current can be directly determined on the basis of the corresponding d_1- q_1 components and the current ratio.

The related reference stator voltages in the synchronous reference frame are then obtained by means of conventional PI regulators, acting on the

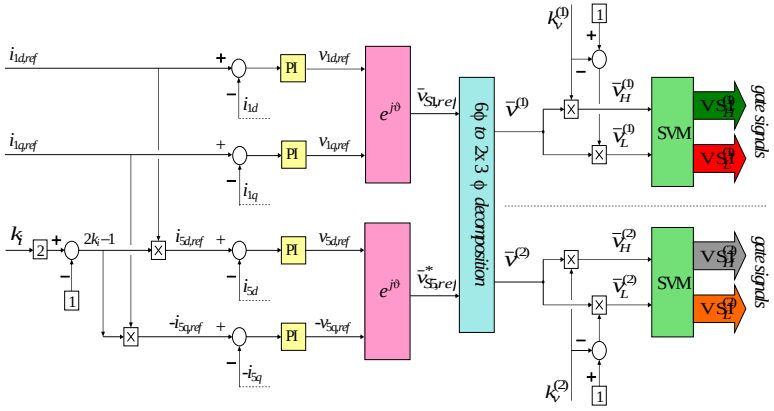


Fig. 5.13: Block diagram of the proposed regulation scheme with power sharing capabilities for dual three-phase induction motor drives.

error signals. Finally, the reference stator voltages in the stationary reference frame, $\bar{v}_{S1,ref}$ and $\bar{v}^{*}_{S5,ref}$, which represent the inputs of the modulation process, are determined through an opportune angular rotation. It can be shown that the current ratio k_i introduced in Eqs. 6 correspond, with a good approximation, to a sharing coefficient of the motor power P between the two three-phase windings. In particular, the total electric power supplied to the motor can be written as [58] and illustrated in detail chapter 3 and 4:

$$P = P^{(1)} + P^{(2)} = 3\bar{v}_{S1} \cdot \bar{i}_{S1} + 3\bar{v}_{S5} \cdot \bar{i}_{S5} \,. \tag{10}$$

$$\begin{cases} P^{(1)} = \dfrac{3}{2}\left[\left(\bar{v}_H^{(1)} + \bar{v}_L^{(1)}\right) \cdot \bar{i}^{(1)}\right] = \dfrac{3}{2}\bar{v}^{(1)} \cdot \bar{i}^{(1)} \\ P^{(2)} = \dfrac{3}{2}\left[\left(\bar{v}_H^{(2)} + \bar{v}_L^{(2)}\right) \cdot \bar{i}^{(2)}\right] = \dfrac{3}{2}\bar{v}^{(2)} \cdot \bar{i}^{(2)} \end{cases}, \tag{11}$$

On the basis of (chapter 3, Eqs. 7), the space vectors of the three-phase stator currents and voltages can be calculated as follows:

$$\begin{cases} \bar{i}^{(1)} = \bar{i}_{S1} + \bar{i}^{*}_{S5} \\ \bar{i}^{(2)} = \alpha^{-1}(\bar{i}_{S1} - \bar{i}^{*}_{S5}) \end{cases}. \tag{12}$$

$$\begin{cases} \bar{v}^{(1)} = \bar{v}_{S1} + \bar{v}^{*}_{S5} \\ \bar{v}^{(2)} = \alpha^{-1}(\bar{v}_{S1} - \bar{v}^{*}_{S5}) \end{cases}. \tag{13}$$

Substituting Eqs. 12 and Eqs 13 in Eqs. 11, and taking Eqs. 8 into account yields:

$$\begin{cases} P^{(1)} = 3k_i\,\bar{v}_{S1}\cdot\bar{i}_{S1} + 3k_i\,\bar{v}^{*}_{S5}\cdot\bar{i}_{S1} \\ P^{(2)} = 3(1-k_i)\bar{v}_{S1}\cdot\bar{i}_{S1} - 3(1-k_i)\bar{v}^{*}_{S5}\cdot\bar{i}_{S1} \end{cases}. \tag{14}$$

As can be recognized analyzing the dual three-phase motor model, in particular (Eqs.1, Eqs. 3) the voltage space vector $\bar{v}^{*}_{S5}$ can be considered negligible with respect to $\bar{v}_{S1}$. By comparing Eqs. 10, and Eqs. 14 lead to:

$$\begin{cases} P^{(1)} \cong k_i \cdot P \\ P^{(2)} \cong (1-k_i)\cdot P \end{cases}. \tag{15}$$

Eqs. 15 confirm that the current ratio k_i defined by Eqs. 6 can be practically considered also a power sharing coefficient between the three-phase windings {1} and {2}.

5.5.2 Power sharing between inverter H and L

The reference output voltage $\bar{v}^{(1)}$ supplying the first three-phase stator winding can be determined by the six- to three-phase decomposition Eqs.13, on the basis of multiple space vector references $\bar{v}_{S1,ref}$ and $\bar{v}^{*}_{S5,ref}$. In particular, $\bar{v}^{(1)}$ can be synthesized as the sum of the voltages $\bar{v}_H^{(1)}$ and $\bar{v}_L^{(1)}$ generated by $VSI_H^{(1)}$ and $VSI_L^{(1)}$, respectively, leading to:

$$\bar{v}^{(1)} = \bar{v}_H^{(1)} + \bar{v}_L^{(1)}. \tag{16}$$

Introducing the voltage ratio $k_v^{(1)}$ and imposing the inverter voltage vectors $\bar{v}_H^{(1)}$ and $\bar{v}_L^{(1)}$ to be in phase with the output voltage vector $\bar{v}^{(1)}$, yields:

$$\begin{cases} \bar{v}_H^{(1)} = k_v^{(1)}\,\bar{v}^{(1)} \\ \bar{v}_L^{(1)} = \left(1-k_v^{(1)}\right)\bar{v}^{(1)} \end{cases}. \tag{17}$$

The condition expressed by Eqs. 17 allow maximum dc voltage utilization. Being the output ac current of the two inverters the same, the coefficient $k_v^{(1)}$ also defines the power sharing between the two inverters. In terms of averaged values within the switching period, the power to the first three-phase stator winding can be expressed as:

$$P^{(1)} = \frac{3}{2}\bar{v}^{(1)}\cdot\bar{i}^{(1)} = P_H^{(1)} + P_L^{(1)}. \tag{18}$$

Where $P_H^{(1)}$ and $P_L^{(2)}$ are the individual powers from the two inverters. By combining Eqs 17 with Eqs. 18 lead to:

$$\begin{cases} P_H^{(1)} = \frac{3}{2}\bar{v}_H^{(1)}\cdot\bar{i}^{(1)} = k_v^{(1)}\,P^{(1)} \\ P_L^{(1)} = \frac{3}{2}\bar{v}_L^{(1)}\cdot\bar{i}^{(1)} = \left(1-k_v^{(1)}\right)P^{(1)} \end{cases}. \tag{19}$$

The coefficient $k_v^{(1)}$ has a limited variation range depending on the value of the reference output voltage $\bar{v}^{(1)}$, as already investigated in [42]. Further, it has to be verified that both references are within the range of achievable output voltages of each inverter, which depend on their dc voltages. In the case of a single inverter topology, if the voltage demand exceeds the voltage limit, the output voltage is simply saturated. With the dual-inverter configuration, total voltage reference must be satisfied, so in case of voltage saturation of one inverter, the second has to provide for the missing part. A possible solution to overcome the problems of voltage saturation in the dual-inverter configuration has been proposed in [42].

An identical approach can be applied to synthesize the voltage $\bar{v}^{(2)}$ supplying the second three-phase stator winding by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, leading to:

$$\bar{v}^{(2)} = \bar{v}_H^{(2)} + \bar{v}_L^{(2)} . \tag{20}$$

As in the preceding case, introducing the voltage ratio $k_v^{(2)}$ leads to:

$$\begin{cases} \bar{v}_H^{(2)} = k_v^{(2)} \bar{v}^{(2)} \\ \bar{v}_L^{(2)} = \left(1 - k_v^{(2)}\right) \bar{v}^{(2)} \end{cases} . \tag{21}$$

The powers to the second three-phase stator winding now become:

$$P^{(2)} = \frac{3}{2} \bar{v}^{(2)} \cdot \bar{i}^{(2)} = P_H^{(2)} + P_L^{(2)} . \tag{22}$$

$$\begin{cases} P_H^{(2)} = \frac{3}{2} \bar{v}_H^{(2)} \cdot \bar{i}^{(2)} = k_v^{(2)} P^{(2)} \\ P_L^{(2)} = \frac{3}{2} \bar{v}_L^{(2)} \cdot \bar{i}^{(2)} = \left(1 - k_v^{(2)}\right) P^{(2)} \end{cases} . \tag{23}$$

Same considerations given for $k_v^{(1)}$ now apply to $k_v^{(2)}$.

5.6 Multilevel SVM algorithm

Once the reference voltage vectors $\bar{v}^{(1)}$ and $\bar{v}^{(2)}$ for the two couples of inverters are determined by Eqs. 17, and Eqs. 21, a proper multilevel SVM algorithm must be applied to satisfy the power sharing imposed by $k_v^{(1)}$ and $k_v^{(2)}$, according to the block diagram of Fig. 5.13. In particular, the SVM algorithm considered in this paper is based on the space vector diagram given in Fig. 5.14. Due to the symmetry of the outer hexagon, the analysis can be restricted to one of its six sectors (i.e., OAB in Fig. 5.14), similarly to the case of conventional three-phase SVM algorithm.

Furthermore, the main triangle OAB is divided in four identical equilateral triangles. The reference voltage $\bar{v}^{(1)}$ lays in one of these triangles, leading to four relevant cases. By the basic SVM principle, the components $\bar{v}_H^{(1)}$ and $\bar{v}_L^{(1)}$ can be generated by selecting adjacent vectors. The

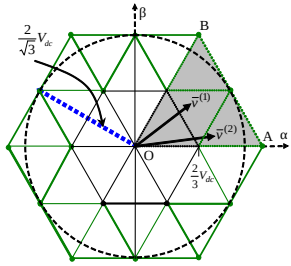


Fig. 5.14: Voltage space vectors generated by inverters H and L for the stator windings {1} and {2}.

switch configurations corresponding to these vectors cannot be applied in an arbitrary sequence if proper multilevel voltage waveforms are desired, i.e., the reference voltage $\bar{v}^{(1)}$ should be generated by using the nearest three vectors approach (NTV) [111]. In order to do this, the method introduced in [42] has been implemented. The same considerations apply to the reference voltage $\bar{v}^{(2)}$.

5.7 Numerical simulation results and discussion

In order to verify the effectiveness of the proposed control strategy, the behavior of the whole system has been numerically tested by means of the PLECS simulation package in the MATLAB environment [121]. For the induction motor, the model presented in section 5.4.2, has been implemented using the parameters given in Table 5.1. The value of the four dc bus voltages (V_{dc}) is set to 155 V and a switching frequency of 5 kHz is selected

Table 5.1: Main parameters of six-phase induction motor

P_{rated}	= 4 kW	R_S	= 0.51Ω
$I_{S,rated}$	= 16 A_{rms}	R_R	= 0.42Ω
$V_{S,rated}$	= 125 V_{rms}	L_{S1}	= 58.2mH
$\omega_{S,rated}$	= 2π50 rad/s	L_{R1}	= 58.2mH
P	= 2 (pairs)	M_1	= 56mH

5.7.1 Investigation test for step variation of torque demand with symmetrical power sharing condition

In the first simulation test (Figs. 5.15-5.19.), the behavior of the system is analyzed in balanced conditions ($k_v^{(1)}$= 0.5: top-purple, $k_v^{(2)}$= 0.5: middle-

turquoise, k_i = 0.5: bottom-blue traces; shown in Fig. 5.15), i.e. the electrical power is equally shared among the four VSIs.

A torque step is demanded to emphasize dynamics, as depicted in Fig. 5.16 (upper trace). The corresponding d_1- q_1 (middle-red, blue traces) and d_5- q_5 stator (bottom-purple, light green traces) current components in the synchronous reference frame are also depicted. Note that i_{5q} and i_{5d} are null being the current ratio k_i set to 0.5 (balanced), according to Eqs. 9, whereas i_{1q} and i_{1d} follow torque and rotor flux commands.

Fig. 5.17 shows the nine-level waveforms of phase voltages $v_1^{(1)}$ (stator voltage of phase 1 of the first three-phase winding {1}: top-purple trace) and $v_1^{(2)}$ (stator voltage of first-phase of the second three-phase winding {2}: bottom-turquoise trace). The time scaled averaged voltage values are also depicted in the same diagram.

The six-phase stator currents are shown in Fig. 5.18, for both the two stator windings (winding {1}: $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; $i_{123}^{(1)}$; top-purple traces and winding {2}: $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; $i_{123}^{(2)}$; bottom-turquoise traces) respectively. It should be noted that the current waveforms are practically sinusoidal, with the same amplitude, and correct phase angle displacements.

Fig. 5.19 shows the low-pass filtered dc currents of the four VSIs, $I_H^{(1)}$, $I_L^{(1)}$, $I_H^{(2)}$, $I_H^{(2)}$ (dual-inverter {1}: top-(H green, L red) traces, dual-inverter {2}: bottom-(H grey, L orange) traces), during the torque step. The instantaneous values have been time scaled averaged by a low-pass filter (τ = 2 ms). The diagrams confirm a balanced dc current sharing among all inverters, i.e., balanced power sharing, as stated by Eqs. 15, Eqs. 19 and Eqs. 23.

5.7.2 Investigation test for asymmetrical power sharing (current) between two three-phase winding {1} and {2}

In the second simulation test (Figs. 5.20-5.24), torque and flux commands are maintained constant. The current ratio k_i has been changed among the values [1/2, 1/3] and [2/3], as shown in Fig. 5.20 (bottom-blue trace), to emphasize the power sharing capability between the two motor windings. The voltage ratio coefficients $k_v^{(1)}$ and $k_v^{(2)}$ are fixed to 0.5 and shown in the same Fig. 5.20 (top-purple, middle-turquoise trace).

Fig. 5.21 shows that torque (upper trace) and d_1- q_1 stator current components in the synchronous reference (i_{1q} and i_{1d}, middle-red, blue traces) are unaffected by this transient, whereas d_5- q_5 stator current components (i_{5q} and i_{5d}, bottom-purple, light green traces) vary according to Eqs. 9.

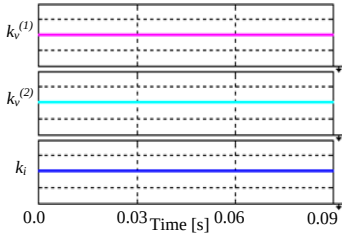


Fig. 5.15: Three degree of freedom. From top-to-bottom: Step variation of voltage and current sharing coefficients. [0.25units/div].

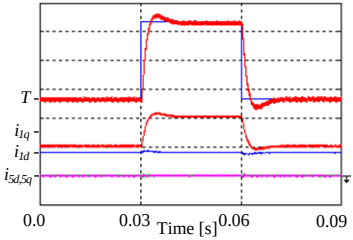


Fig. 5.16: Step change between 50% and 100% of the rated torque, and *d-q* current components. From top-to-bottom: T, i_{1q}, i_{1d}, i_{5q}, i_{5d}. [10Nm/div], [10A/div].

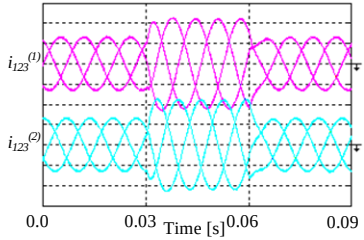


Fig. 5.18: Stator phase currents on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [10A/div].

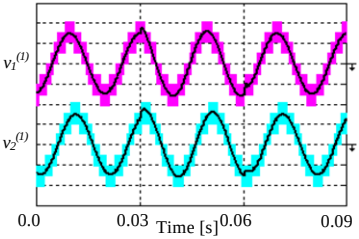


Fig. 5.17: First-phase stator voltage with time scaled average components on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [100v/div].

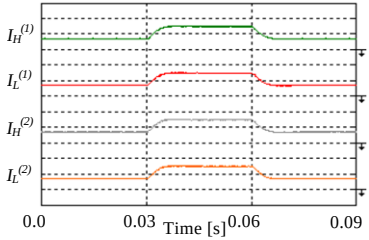


Fig. 5.19: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: Dual-inverter {1}: H (green) and L (red) traces; Dual-inverter {2}: H (gray) and L (orange) traces [10A/div].

The corresponding waveforms of nine-level phase voltages $v_1^{(1)}$(stator voltage of first-phase of the first three-phase winding {1}: top-purple trace) and $v_1^{(2)}$ (stator voltage of first-phase of the second three-phase winding {2} bottom-turquoise trace), are depicted along with time scaled average values in Figs. 5.22 respectively.

Fig. 5.23 shows that the six-phase stator currents amplitudes of windings {1} and {2} change according to Eqs. 7 (winding {1}: $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$, $i_{123}^{(1)}$; top-

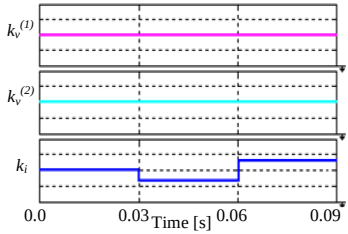


Fig. 5.20: Three degree of freedom. From top-to-bottom: Step variation of voltage and current sharing coefficients. [0.25units/div].

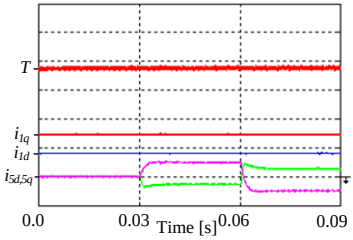


Fig. 5.21: Set point value corresponds to the rated torque, and *d-q* current components. From top-to-bottom: T, i_{1q}, i_{1d}, i_{5q}, i_{5d}. [10Nm/div], [10A/div].

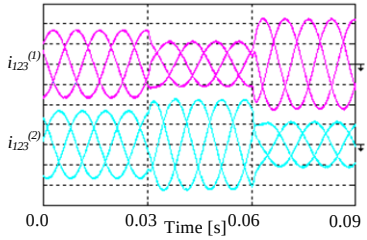


Fig. 5.23: Stator phase currents on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [10A/div].

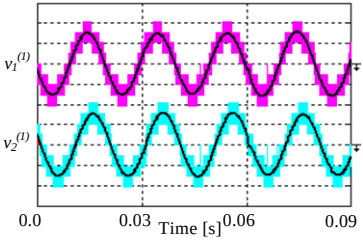


Fig. 5.22: First-phase stator voltage with time scaled average components on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [100v/div].

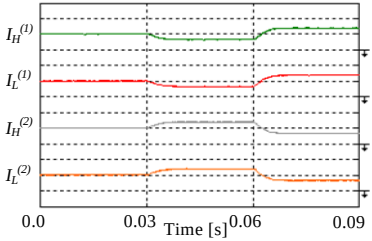


Fig. 5.24: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: Dual-inverter {1}: H (green) and L (red) traces; Dual-inverter {2}: H (gray) and L (orange) traces [10A/div].

purple traces and winding {2}: $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; $i_{123}^{(2)}$; bottom-turquoise traces) respectively.

Fig. 5.24 emphasizes the low-pass filtered value of the four dc currents. Owing to $k_v^{(1)} = k_v^{(2)} = 0.5$, the dc currents of dual-inverter {1} are equal (two upper-(H green, L red) traces) and the same holds for the dc currents of dual-inverter {2} (two lower-(H grey, L orange) traces). On the contrary, the dc currents of dual-inverters {1} and {2} become different as k_i changes

from 0.5, due to the power sharing variation between the two windings {1} and {2}, as stated by Eqs. 15.

5.7.3 Investigation test for asymmetrical power sharing (voltage) between single inverter's (H and L) of two three-phase winding {1} and {2}

In last simulation test (Figs. 5.25-5.29), the power sharing capability between the two inverters H and L of each three-phase stator windings has been emphasized while both torque and flux commands are kept constant. The voltage ratios $k_v^{(1)}$ and $k_v^{(2)}$ have been changed between the values [1/2, 1/3] and [1/2, 2/3] respectively, at different time instants, as shown in Fig. 5.25 (top-purple, middle-turquoise trace). In this case, the current ratio coefficient k_i is fixed to 0.5 and shown in same Fig. 5.25 (bottom-blue trace).

As expected, these changes do not affect the torque and the d_1- q_1 and d_5- q_5 stator current components, as shown in Fig. 5.26. Note that i_{5q} and i_{5d} are null (bottom-purple, light green traces) being the current ratio k_i set to 0.5, whereas the values of i_{1q} and i_{1d} (middle-red, blue traces) are determined by torque and rotor flux references, respectively.

Fig. 5.27 shows the nine-level waveforms of phase voltages $v_1^{(1)}$ (stator voltage of first-phase of the first three-phase winding {1}: top-purple trace) and $v_1^{(2)}$ (stator voltage of first-phase of the second three-phase winding {2}: bottom-turquoise trace) together with their time scaled averaged value. Also the six-phase stator currents are unaffected by this transient, as proved by Fig. 5.28 (winding {1}: $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; $i_{123}^{(1)}$; top-purple traces and winding {2}: $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; $i_{123}^{(2)}$; bottom-turquoise traces).

Fig. 5.29 emphasizes the low-pass filtered values of the four dc currents. Owing to $k_i = 0.5$, the sum of dc currents of dual-inverter {1} (two lower-(H green, L red) traces, proportional to $P^{(1)}$) is constant and equal to the sum of dc currents of dual-inverter {2} (two lower-(H grey, L orange) traces, proportional to $P^{(2)}$), whereas each dc current and its corresponding dc power change according to Eqs. 19 and Eqs. 23.

5.8 Conclusion

Multiphase induction motor drives, control aspects and its applications were discussed elaborately from literatures survey and a novel multiphase multilevel ac motor drive based on a dual three-phase open-end windings induction motor was presented and analyzed in this chapter. The power supply consists of four conventional 2-level three-phase voltage source inverters with insulated dc sources. An appropriate control strategy which

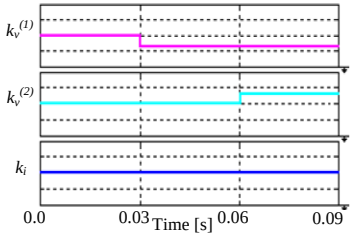


Fig. 5.25: Three degree of freedom. From top-to-bottom: Step variation of voltage and current sharing coefficients [0.25units/div].

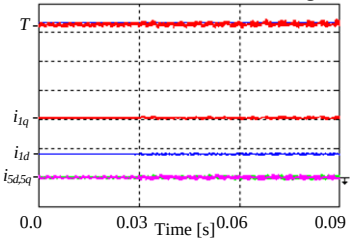


Fig. 5.26: Set point value corresponds to the rated torque, and *d-q* current components. From top-to-bottom: T, i_{1q}, i_{1d}, i_{5q}, i_{5d}. [10Nm/div], [10A/div].

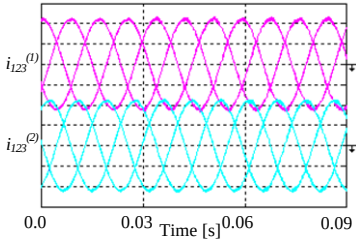


Fig. 5.28: Stator phase currents on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [10A/div].

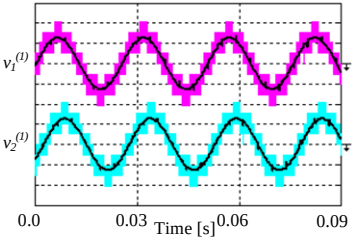


Fig. 5.27: First-phase stator voltage with time scaled average components on windings {1} and {2}. From top-to-bottom: winding-{1} (purple trace); winding-{2} (turquoise trace). [100v/div].

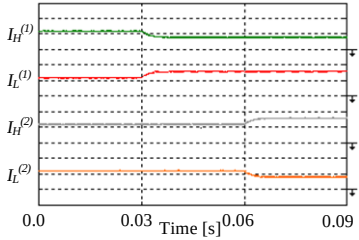


Fig. 5.29: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: Dual-inverter {1}: H (green) and L (red) traces; Dual-inverter {2}: H (gray) and L (orange) traces [10A/div].

allows the total motor power to be shared among the four dc sources with three degrees of freedom has been proposed.

In order to regulate the couple of 2-level VSIs supplying each three-phase winding such as a 3-level inverter, a specific SVM technique has been adopted, allowing the power sharing between the two dc sources. This regulation leads to two degrees of freedom in the total power sharing, one for each three-phase winding. A suitable control technique has been proposed in order to regulate the power sharing between the two three-phase windings, leading to an additional degree of freedom in the total

power sharing. Numerical simulation tests results provided in this chapter prove the most effectiveness of the proposed quad-inverter based ac motor drive with different operating conditions. Power sharing is a useful skill in battery supplied drives where the charge status of batteries should be balanced. Some of the presented results already published in referred conference proceedings [124-125].

6. Post-fault tolerance strategy for multiphase-multilevel AC motor drive

6.1 Introduction

In this chapter, fault occurrence possibilities in ac machine drives either in power conversion section and/or in motor configuration unit discussed based on literatures and some post-fault tolerant control strategies for multiphase-multilevel induction motor drives was investigated and proposed. In healthy conditions, the control algorithm proposed in chapter 5 able to generate multilevel voltage waveforms and to share the total motor power among the four dc sources in each switching period. This sharing capability was investigated under different post-fault operating conditions when one, two, or three VSI must be completely insulated and/or open-circuited due to severe fault on it. In such circumstances, multiphase-multilevel inverter can continue to perform with de-graded power by a proper modulation of the remaining healthy VSIs. The whole ac motor drive has been investigated with theoretical background and numerical simulation results are provided to verify the most effectiveness of the post-fault control strategies under healthy and some developed fault operating conditions.

6.2 Fault tolerant analysis

Fault-tolerability in ac traction systems is a key item with high-voltage/high-current applications, where availability and reliability of performances are mandatory. In specific, for this type of application, induction motors operate continuously in dynamic conditions, requiring frequent start/stop with rapid speed variations. Subsequently, the drives are regularly subjected to abuse of over-current surges and voltage over-swings. Recent research carried out on different failure possibilities in induction motor drives by industrials and experts have revealed that 21% related to the stator windings and its configuration, details report in [111]. Several phenomenon's can affect its reliability, such as mechanical and/or thermal stress, leading to severe failure possibilities such as inter-turn short-circuits, line-to-line, line-to-ground, multiphase line-to-ground and multiphase faults. A detailed analysis on these types of fault occurrences and its propagation, diagnosis can be found in [111-113]. On another hand investigations are performed to increase the power ratings have focused their efforts on passive or/and active semiconductors have been proposed, but its lower reliability still remain their major drawback explained in detail [114-115]. A large reliability investigation of inverter topologies has

Keywords**:** *Multiphase-multilevel ac motor, dual three-phase induction motor, fault-tolerance, and multilevel space vector modulation.*

revealed that its estimated mean time between failures (MTBFs) is of about 2 years investigated in [116]. All inverter configurations still vulnerable to different potential anomalies, leading to an imminent total failure. Recent survey on inverters has revealed that (31-37.9)% of failures are caused by power parts [116] and the main failure mechanisms in modern power modules with IGBT devices for high-power application can be found in [117]. Most potential sources of failures based on power devices, capacitors and gate control are detailed in [118].

In perspective view, in this chapter the proposed contribution devoted towards investigating inherent active redundancy of the used quad-inverter based ac motor drive system, under one, two, or three failed inverters, to ensure system operability in degraded mode [119-120]. During healthy condition quad-inverter system able to generate multilevel output voltages and under faulty condition continue to perform has 2-level inverters with available healthy VSIs in degraded mode. In the next sections, detailed theoretical background was described for the entire ac drive system with faulty VSIs condition, by exploiting the three degree of freedom in different circumstances.

6.3 Proposed post-fault tolerance control strategy

Integrated cooling technologies are widely employed in commercial inverter applications for high power ac traction system. Advantage of such technologies, such as ease-of-use, miniaturization and compactness in traction systems. However, the non-maintainability due to the compact packaging and the reduced thermal dissipation justifies the reduced reliability of the inverters [114-116]. Independently to the technology adopted, the inverters are still mainly subjected to several failures due to:

- Electrolytic capacitor in dc-link, dc bus voltage sensor.
- Power semiconductor (short-circuit or open-circuit).
- Control and driver circuits.

Commonly known by its rapid propagation, leading to severe degrees of damage for the whole system. For these reasons, whenever one among the four inverters is affected by the above failures, most of the times the concerned inverter can be considered as totally damaged and must be removed. The failed inverter should be disconnected from both the motor and the dc source (battery), e.g. using bypass switches. Then, the developed control system is adapted in a manner that the ac motor drive machine still continues to operate in post-fault conditions. In the following section an detailed investigation along with theoretical description for the whole ac

drive system are discussed under some developed post-fault conditions are realized by exploiting the degree of freedom in all cases, without using any additional bypass switches or protective circuitry.

6.3.1 Control strategy when one failed inverter

In this designed post-fault configuration illustrates, the proposed control strategy allows continuity of operation, but with reduced degree of freedom in the power sharing among the dc sources: from three degrees, under healthy conditions, to two. In fact, supposing the fault occurs on inverter $VSI_L^{(1)}$, represented as equivalent circuit in three-phase space vectors shown in Fig. 6.1, the corresponding dc source must be insulated, and three output phases must be short-circuited to allow current circulation on stator winding {1}. The open-end winding configuration of the motor now collapse to traditional three-phase star connection in stator winding {1}, and the entire voltage for stator winding {1}, $\bar{v}^{(1)}$, must be provided by inverter $VSI_H^{(1)}$. Whereas the voltage for stator winding {2}, $\bar{v}^{(2)}$, provided by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$.

Then, according to Eqs. (17, 19, 21, 23) given by chapter 5, the post-fault operating conditions can be summarized as [119-120]:

$$\begin{cases} \bar{v}_L^{(1)} = 0 \\ \bar{v}_H^{(1)} = \bar{v}^{(1)} \end{cases} \Leftrightarrow \quad k_v^{(1)} = 1, \tag{1}$$

Taking into account Eqs. 1, and Eqs. (15, 19, 23) given by chapter 5, the individual inverter powers are now expressed as:

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} \cong k_i \cdot P \end{cases}; \begin{cases} P_L^{(2)} \cong \left(1-k_i\right)\cdot\left(1-k_v^{(2)}\right)\cdot P \\ P_H^{(2)} \cong \left(1-k_i\right)\cdot k_v^{(2)} \cdot P \end{cases}. \tag{2}$$

Being $k_v^{(1)}$ imposed by the fault, the remaining two degree of freedoms are now represented by $k_v^{(2)}$ (i.e. power (voltage) sharing between healthy inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$) and k_i (i.e. power (current) sharing between the two

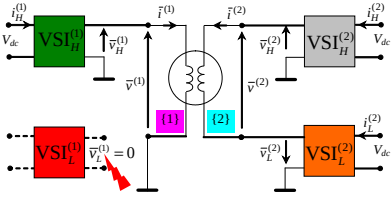


Fig. 6.1: Equivalent circuit of the post-fault configuration, in terms of three-phase space vectors, with one failed inverter $VSH_L^{(1)} = 0$.

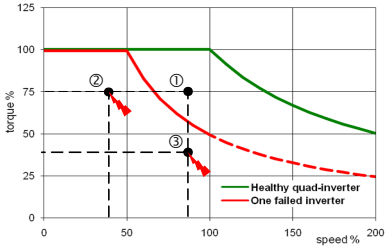


Fig. 6.2: Considered operating points in torque-speed diagram for healthy (4 VSIs) and one failed inverter (3 VSIs) conditions.

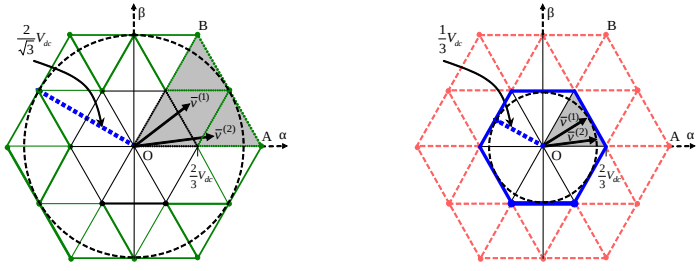


Fig. 6.3: Voltage space vectors generated by inverters H and L for the stator windings {1} and {2}. (a) Healthy conditions. (b) One failed inverter conditions.

three-phase winding {1} and {2}). In this investigation, condition Eqs. 1 will be used in numerical simulations to represent the post-fault conditions instead of using additional bypass switches for creating star connection on the faulty inverter and complete insulation and for current circulation. The first relevant consequence of the fault in one inverter is that the maximum output voltage for one of the two three-phase stator windings is halved. As a consequence, since the two stator windings share the same magnetic circuit and have the same induced e.m.f., the maximum voltage of the other stator winding halved as well, leading to a 50% reduction of the whole maximum motor power, from $2/\sqrt{3}V_{dc}$ to $1/\sqrt{3}V_{dc}$, as emphasized in Fig. 6.3b. This condition is summarized in Fig. 6.2, with reference to the torque versus speed characteristics in healthy (green line) and faulty (red line) operating conditions.

As an example, the operating point ① can be implemented only in healthy conditions, whereas the operating points ② and ③ can be implemented also in post-fault conditions (the last one with a flux weakening to reduce the required stator winding voltage). Different strategies can be introduced to realize the post-fault operating conditions, with three healthy VSIs. In this investigation two cases relating one to the minimization of power losses and another one for symmetrical power sharing among the three healthy VSIs (i.e., among the corresponding three dc sources).

6.3.1A Balanced power sharing between the two three-phase stator motor windings and minimization of power losses

As known, a balanced current sharing between the two three-phase windings leads to minimum stator copper losses. This can be simply implemented in post-fault conditions by setting k_i=1/2, with arbitrary voltage sharing coefficient $k_v^{(2)}$ to synthesize $\bar{v}^{(2)}$. Although the usage of both $VSI_H^{(2)}$ and $VSI_L^{(2)}$ allows an active redundancy, it is not optimal from the point of view of the inverter losses, involving two inverters when the desired output voltage could be synthesized with just one of them.

For this reason, the provision of a passive redundancy with one inverter for the winding {2} still considerably improve the reliability of the post-fault configuration but it reduces the whole converter losses. In this case, inverter $VSI_H^{(1)}$ can operate just with inverter $VSI_H^{(2)}$, whereas the output voltage of inverter $VSI_L^{(2)}$ is set to zero, or vice versa, leading to exactly the same operating performances of the motor. The open-end windings configuration of the motor now collapse to traditional three-phase star connections in both stator winding sets {1}, {2} and represented as equivalent circuit in three-phase space vectors shown in Fig. 6.4. Voltage and power Eqs. (17, 21, 19, 23) given by chapter 5, in addition to the fault condition Eqs. 1 can now be summarized as:

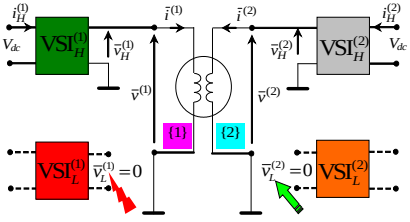


Fig. 6.4: Equivalent circuit of the post-fault configuration, in terms of three-phase space vectors, with one failed inverter $VSH_L^{(1)}=0$, and passive redundancy $VSH_L^{(2)}=0$.

$$\begin{cases} \bar{v}_L^{(2)} = 0 \\ \bar{v}_H^{(2)} = \bar{v}^{(2)} \end{cases} \Leftrightarrow \quad k_v^{(2)} = 1, \tag{3}$$

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} = \frac{1}{2} \cdot P \end{cases}; \begin{cases} P_L^{(2)} = 0 \\ P_H^{(2)} = \frac{1}{2} \cdot P \end{cases} \Leftrightarrow \quad k_v^{(2)} = 1, \tag{4}$$

6.3.1B Balanced power sharing among the three healthy VSIs

Further step in this post-fault investigation when one VSI severer failure on it, point of interest is to share the total motor power symmetrically among the three healthy inverters, i.e., among the three remaining dc sources. This behavior is recommended for battery supplied traction systems, in which the balanced charge status of batteries can be considered as a crucial issue. In order to implement a balanced power sharing among the three dc power supplies, an unbalanced power sharing between the two three-phase windings {1} and {2} must be introduced. In particular, one third of the total motor power must be supplied by each VSI, leading to the

following voltage and power equations, according to Eqs. 1, Eqs. 2, and Eqs. (15, 17, 19, 21, 23) given by chapter 5, leads to summarized as:

$$\begin{cases} \bar{v}_L^{(2)} = \frac{1}{2}\cdot\bar{v}^{(2)} \\ \bar{v}_H^{(2)} = \frac{1}{2}\cdot\bar{v}^{(2)} \end{cases} \Leftrightarrow \quad k_v^{(2)} = \frac{1}{2}, \tag{5}$$

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} \cong \frac{1}{3}\cdot P \end{cases}; \begin{cases} P_L^{(2)} \cong \frac{1}{3}\cdot P \\ P_H^{(2)} \cong \frac{1}{3}\cdot P \end{cases} \Leftrightarrow \quad k_i = \frac{1}{3}. \tag{6}$$

6.3.2 Control strategy when two failed inverter

In this designed post-fault configuration illustrates, the proposed control strategy allows continuity of operable state, but with reduced degree of freedom in the power sharing among the dc sources: from three degrees, under healthy conditions, to one. Presumed the fault occurs on inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, represented as equivalent circuit in three-phase space vectors shown in Fig. 6.5, the corresponding three output phases on either sides of the winding {2} must open-circuited by disconnecting the faulty inverters. The multiphase configuration of the motor now collapse to three-phase open-end winding machine. The entire voltage for stator winding {1}, $\bar{v}^{(1)}$, must be provided by inverters $VSI_H^{(1)}$ and $VSI_L^{(1)}$.

Then, according to Eqs. 7 given by chapter 5, the post-fault operating conditions can be summarized as:

$$\begin{cases} \bar{i}^{(2)} = 0 \\ \bar{i}^{(1)} = 2\bar{i}_{S1} \end{cases} \Leftrightarrow \quad k_i = 1, \tag{7}$$

Taking into account Eqs. 7, and Eqs. (15, 19, 23) given by chapter 5, the individual inverter powers are now expressed as:

$$\begin{cases} P_H^{(1)} = \frac{1}{2}.P \\ P_L^{(1)} = \frac{1}{2}.P \end{cases} \leftrightarrow k_v^{(1)} = \frac{1}{2}; \begin{cases} P_L^{(2)} = 0 \\ P_H^{(2)} = 0 \end{cases} \leftrightarrow k_i = 1. \tag{8}$$

Being k_i imposed by the fault, obviously $k_v^{(2)}$ vanishes and the remaining one degree of freedoms are now represented by $k_v^{(1)}$, i.e. voltage sharing between healthy inverters $VSI_H^{(1)}$ and $VSI_L^{(1)}$. In this investigation, condition Eqs. 7 will be used in numerical simulations to represent the post-fault conditions instead of using additional bypass switches for creating open-circuit connection on the faulty inverters. As a consequences of this post-fault condition, stator windings {1} as the magnetic circuit and produce induced e.m.f., the maximization of phase voltage from $1/\sqrt{3}V_{dc}$ to $2/\sqrt{3}V_{dc}$, as emphasized in Fig. 6.3b, leading to a 50% reduction of the

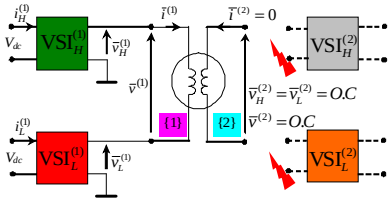


Fig. 6.5: Equivalent circuit of the post-fault configuration, in terms of three-phase space vectors, with two failed inverter $i_L^{(1)} = 0$.

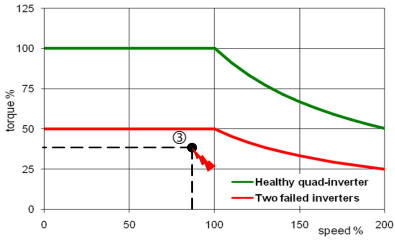


Fig. 6.6: Considered operating points in torque-speed diagram for healthy (4 VSIs) and two failed inverter (2 VSIs) conditions.

whole maximum motor power halved by the open-circuit of stator winding {2}. This condition is summarized in Fig. 6.6, with reference to the torque versus speed characteristics in healthy (green line) and faulty (red line) operating conditions.

For illustrate this post-fault condition an example, the operating point ③ was used for numerical simulation implementation with keeping rated flux value to maximizes the required stator winding {1} voltages. Apparently this condition causes the voltage sharing coefficient $k_v^{(1)}$ always fixed to 1/2, for balanced power sharing between $VSI_H^{(1)}$ and $VSI_L^{(1)}$, leads to maximum output phase voltages with nine-stepped multilevel waveform (Fig. 6.3a). Post-fault condition are realized with out disconnecting the faulty inverters from the circuit, hence the voltage across stator winding {2}, $\bar{v}^{(2)}$, provided by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, are practically an open-circuited voltage.

6.3.3 Control strategy when three failed inverter

In this designed post-fault configuration illustrates, the maximum redundancy operation of the entire ac drive system, the proposed control strategy allows continuity of operation, but with three degree of freedom in the power sharing among the dc sources, under healthy state, to null in faulty condition. Presumed the fault occurs on inverters $VSI_L^{(1)}$, $VSI_H^{(2)}$ and $VSI_L^{(2)}$ represented as equivalent circuit in three-phase space vectors shown in Fig. 6.7. The corresponding dc source of $VSI_L^{(1)}$ must be

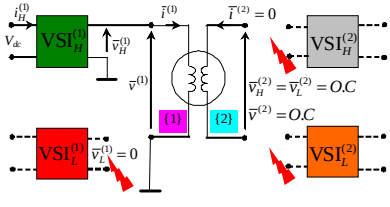


Fig. 6.7: Equivalent circuit of the post-fault configuration, in terms of three-phase space vectors, with three failed inverter $VSH_L^{(1)} = i_L^{(1)} = 0$.

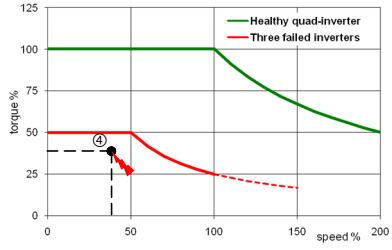


Fig. 6.8: Considered operating points in torque-speed diagram for healthy (4 VSIs) and three failed inverter (1 VSIs) conditions.

insulated, and three output phases must be short-circuited to allow current circulation on stator winding {1}. The open-end winding configuration of the motor now collapse to traditional three-phase star connection in stator winding {1}.

Further, the corresponding three output phases on either sides of the winding {2} must be open-circuited. Now, multiphase configuration of the entire ac motor collapse to three-phase star connected machine. The entire voltage for stator winding {1}, $\bar{v}^{(1)}$, must be provided by inverter $VSI_H^{(1)}$ (given by section 6.3.1). Whereas for the stator winding {2}, $\bar{v}^{(2)}$, provided by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, are practically an open-circuit voltage (given by section 6.3.2). Then, according to Eqs. (7, 17, 19, 23) given by chapter 5, the post-fault operating conditions can be summarized as:

$$\begin{cases} \bar{v}_L^{(1)} = 0 \\ \bar{v}_H^{(1)} = \bar{v}^{(1)} \\ \bar{i}^{(2)} = 0 \\ \bar{i}^{(2)} = 2\bar{i}_{S1} \end{cases} \Leftrightarrow \begin{matrix} k_v^{(1)} = 1 \\ k_i = 1 \end{matrix}, \tag{9}$$

Taking into account Eqs. 9 and Eqs. (15, 19, 23) given by chapter 5, the individual inverter powers are now expressed as:

$$\begin{cases} P_L^{(1)} = 0 \\ P_H^{(1)} = P \end{cases} \leftrightarrow k_v^{(1)} = 1; \begin{cases} P_L^{(2)} = 0 \\ P_H^{(2)} = 0 \end{cases} \leftrightarrow k_i = 1 \cdot \tag{10}$$

Being $k_v^{(1)}$, k_i imposed by the fault, obviously $k_v^{(2)}$ vanishes and degree of freedom reduced to null in total power sharing of the proposed ac drive system. In this investigation, condition Eqs. 9 will be used in numerical simulations to represent the post-fault conditions instead of using additional bypass switches for creating star connection and/or open-circuited on the faulty inverters and complete insulation for current circulation.

Consequence of this fault in three inverters is that the maximum output voltage for three-phase stator windings {1} is halved by fault on $VSI_L^{(1)}$. Since the stator winding {1} has the magnetic circuit and produce induced e.m.f., the maximization of phase voltage from $2/\sqrt{3}V_{dc}$ to $1/\sqrt{3}V_{dc}$, as emphasized in Fig. 6.3b, leading to a 75% reduction of the whole maximum motor power halved by the open-circuit of winding {2}. This condition is summarized in Fig. 6.8, with reference to the torque versus speed characteristics in healthy (green line) and faulty (red line) operating conditions. For illustrate this post-fault condition an example, the operating point ④ was used for numerical simulation implementation with keeping rated flux to maximizes the required stator winding {1} voltage.

6.4 Numerical simulation results and discussion

For the purposes of investigation studies and to verify the most effectiveness of the proposed post-fault control strategies, the entire ac drive system has been designed, implemented and numerically tested by means of

the PLECS simulation software package in the MATLAB environment under healthy and one, two, and three failed VSI conditions [119-121]. For the induction motor and its drive model, parameters are taken from Table 5.1 (chapter 5).

6.4.1 Investigation performances during healthy condition (operating point ①)

In this simulation test, the system is analyzed in healthy state conditions in the whole interval (90 ms) considering the operating point ① in Fig. 6.2 (speed 1200 rpm, torque 38 Nm). Balanced behavior is introduced by setting the all the sharing coefficients to 1/2 ($k_v^{(1)}$: purple, $k_v^{(2)}$: turquoise, k_i: blue; traces) as shown in Fig. 6.9, i.e., the electrical power is equally shared among the four healthy VSIs. The electromagnetic torque T is depicted in the same Fig. 6.9 (bottom-red; trace).

Fig. 6.10 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. It can be clearly noticed that the time scaled averaged voltages are almost sinusoidal (fundamental components) with the same amplitude and with a proper phase shift (i.e., 180° between the two voltages on the same winding, and 30° between the voltages on different windings).

The stator windings voltages of the first-phase along with their time averaged values are depicted in Fig. 6.11, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. As expected, proper multilevel stepped waveforms appear with 9 levels, being the modulation index greater than 50% (outer hexagon shown in Fig. 6.3a), and a phase shift of 30° is noticed.

The six stator winding currents are shown in the same Fig. 6.11, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. Currents are almost sinusoidal, with the same amplitude, and correct 30° phase displacements.

Fig. 6.12 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. Values are low-pass filtered (τ = 20 ms) to emphasize the dc current components and have the same value, proving the effectiveness of the modulation strategy in balanced operating conditions.

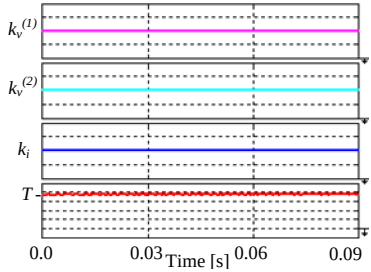


Fig. 6.9: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in steady-state and healthy condition [10Nm/div].

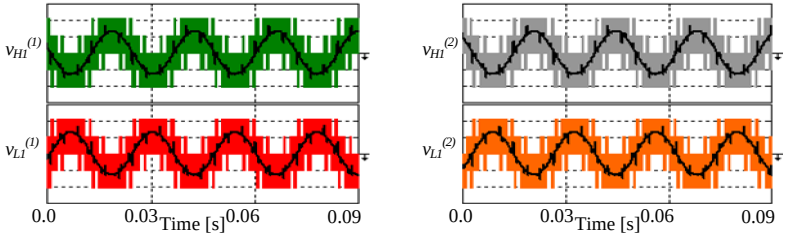


Fig. 6.10: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

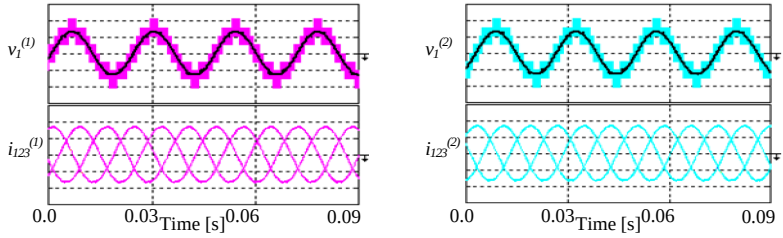


Fig. 6.11: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

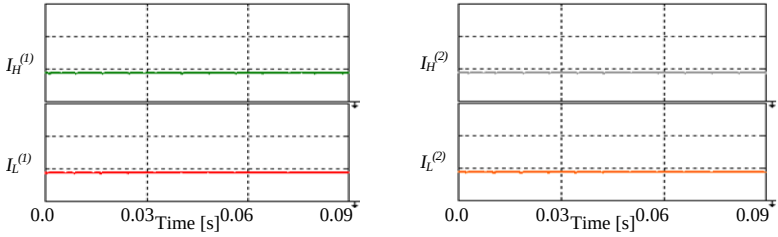


Fig. 6.12: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [10A/div].

6.4.2 Investigation performances during post-fault conditions with one failed inverter

In the following two simulation tests, depicted in Figs. 6.13-6.20, the system is analyzed with healthy state in the first time interval [0-30ms] considering the operating point ② in Fig. 6.2 (halved speed, 600 rpm, same torque, 38 Nm). At the time instant t = 30 ms the fault on inverter $VSI_L^{(1)}$ occurs, and it is completely disabled by setting to 1 corresponding voltage sharing coefficient $k_v^{(1)}$, as expressed by Eqs. 1. No further actions are taken in the second time interval [30-60 ms]. At the time instant t = 60 ms the two proposed post-fault strategies are applied, according to the description given in sub-sections 6.3.1A and 6.3.1B. No further actions are taken in this third time interval [60-90 ms].

For the sake of readability of figures, the fault instant is emphasized by a red-shock arrow, whereas the starting instant of the proposed control strategy is represented by a green-straight arrow and will be depicted for all the proceeding post-fault investigation conditions.

6.4.2A Balanced power sharing between the two three-phase stator motor windings (operating point ②)

This first test during post-fault conditions was conducted to prove the effectiveness of the proposed control strategy when a balanced power sharing between the two winding {1} and {2} is required, and minimization of inverter losses is realized by switching off one of the remaining three healthy VSIs.

Fig. 6.13 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, $k_v^{(1)}$ turns to 1) and when the first post-fault strategy is applied (t = 60 ms, $k_v^{(2)}$ turns to 1), according to conditions Eqs. 3 and Eqs. 4 introduced in sub-section 6.3.1.A. The current sharing coefficient k_i remains unchanged.

Fig. 6.13 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as it should be.

Fig. 6.14 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. When the fault occurs on inverter $VSI_L^{(1)}$, the corresponding voltage $v_{L1}^{(1)}$ goes to zero, whereas the voltage on the other side of winding {1}, $v_{H1}^{(1)}$, doubles its value to provide for the missing winding voltage.

Voltages $v_{H1}^{(2)}$ and $v_{L1}^{(2)}$ are unaffected by the fault, being applied to the other winding. As the first post-fault control strategy is applied, $VSI_L^{(2)}$ is turned off by setting $v_{L1}^{(2)}$ to zero, and the voltage $v_{H1}^{(2)}$ doubles its value to provide for the missing voltage on winding {2}. Remaining active inverters $VSI_H^{(1)}$ and $VSI_H^{(2)}$ provide now the voltages $v_{H1}^{(1)}$ and $v_{H1}^{(2)}$ with same amplitudes and the proper 30° phase shift.

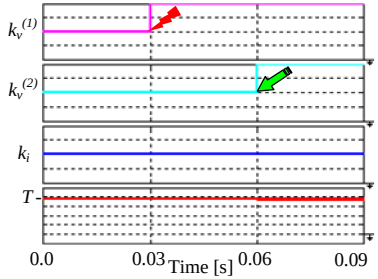


Fig. 6.13: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

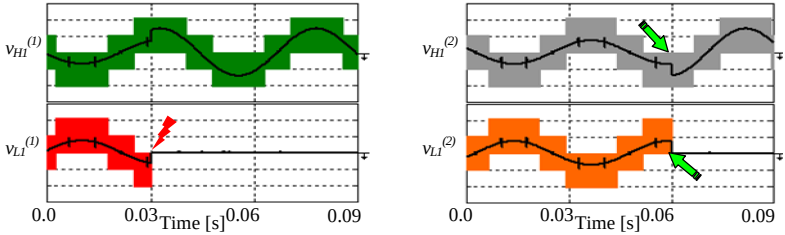


Fig. 6.14: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

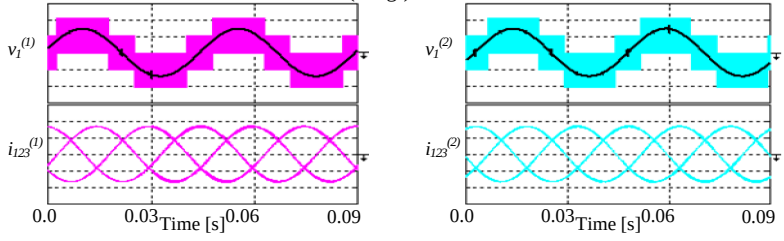


Fig. 6.15: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

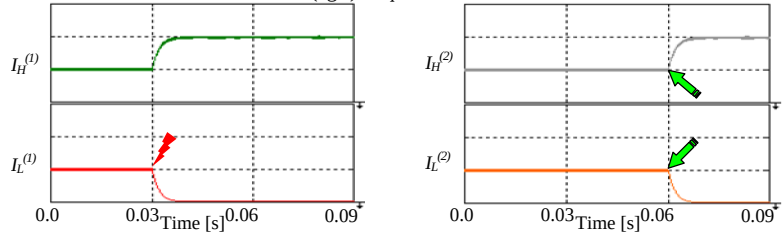


Fig. 6.16: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

Fig. 6.15 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. As expected, multilevel stepped waveforms appear now with 5 levels, as for traditional 2-level inverters, being the modulation index lower than 50% (inner hexagon shown in Fig. 6.3b).

The six stator winding currents are shown in the same Fig. 6.15, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. Note that both voltages and currents are practically unaffected by the fault and by the power sharing transients, as expected.

Fig. 6.16 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. Values are low-pass filtered (τ = 20 ms) to emphasize the dc current components. Being the dc supply voltage V_{dc} constant during all transients, the dc currents well represent the individual powers supplied by the four VSIs. Then, it can be clearly seen as the total motor power is equally shared between inverters $VSI_H^{(1)}$ and $VSI_H^{(2)}$ in this first post-fault control strategy, according to Eqs. 4.

6.4.2B Balanced power sharing between the three healthy VSIs (operating point ②)

This second test during post-fault conditions was conducted to prove the effectiveness of the proposed control strategy when a balanced power sharing among the remaining three healthy VSIs is required (i.e., balanced power sharing among the corresponding three dc sources).

Fig. 6.17 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, $k_v^{(1)}$ turns to 1) and when the second post-fault strategy is applied (t = 60 ms, k_i turns to 1/3), according to conditions Eqs. 5 and Eqs. 6 introduced in sub-section 6.3.1B. The voltage sharing coefficient $k_v^{(2)}$ remains unchanged. Fig. 6.17 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as it should be.

Fig. 6.18 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. When the fault occurs on inverter $VSI_L^{(1)}$, the corresponding voltage $v_{L1}^{(1)}$ goes to zero, whereas the voltage on the other side of winding {1}, $v_{H1}^{(1)}$, doubles its value to provide for the missing winding voltage.

Voltages $v_{H1}^{(2)}$ and $v_{L1}^{(2)}$ are unaffected by the fault, being applied to the other winding, as in the previous test. As the second post-fault strategy is applied, voltages $v_{H1}^{(1)}$, $v_{H1}^{(2)}$, and $v_{L1}^{(2)}$ just slightly change as a consequences of the change of the current sharing

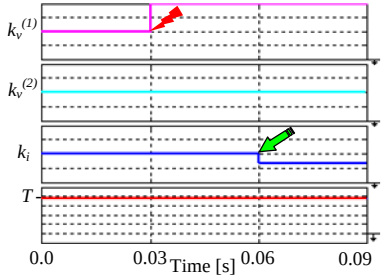


Fig. 6.17: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

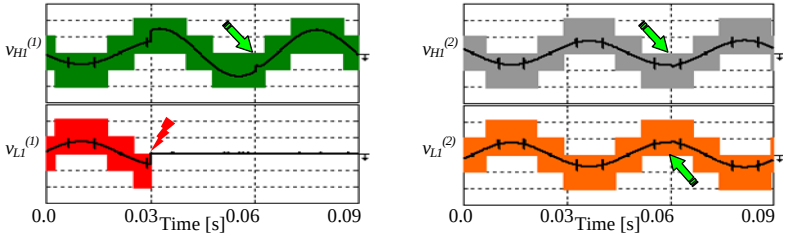


Fig. 6.18: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

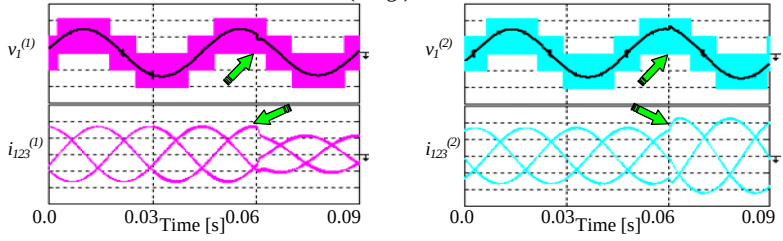


Fig. 6.19: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

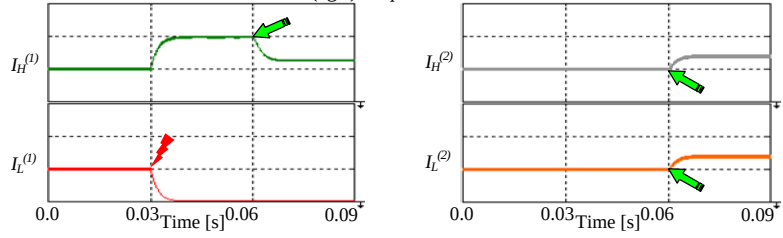


Fig. 6.20: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

coefficient. In fact, just a small variation of stator winding voltages can be responsible of considerable currents changes.

Fig. 6.19 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. Also in this case, multilevel stepped waveforms appear with 5 levels, as for traditional 2-level inverters, being the modulation index lower than 50% (inner hexagon shown in Fig. 6.3b). The slight voltage variation introduced by the current sharing coefficient change can now be better observed.

The six stator winding currents are shown in the same Fig. 6.19, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. The current sharing coefficient change from 1/2 to 1/3 leads to an increase of currents on winding {2}, and to an decrease of currents on winding {1}, becoming ones the double of the others, and according to Eqs. 7 given by chapter 5.

Fig. 6.20 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. It can be clearly seen from low-pass filtered dc currents, the total motor power is equally shared among inverters $VSI_H^{(1)}$, $VSI_H^{(2)}$, and $VSI_L^{(2)}$ in this second post-fault control strategy, according to Eqs. 6.

6.4.3 Investigation performances during post-fault conditions with one failed inverter in field-weakening region

In the following two simulation tests, depicted in Figs. 6.21-6.28, the system is analyzed with considering the operating point ③ in Fig. 6.2 (speed, 1200 rpm, halved torque, 19 Nm). Noted that in the following simulation tests, operating point ③ was chosen in the flux-weakening region, hence the reference flux command value reduced to half for lowering stator windings voltages, in comparison to the operating point②. Further action and investigation with healthy as well as post-fault conditions are employed in similar with respect to, operating point②.

6.4.3A Balanced power sharing between the two three-phase stator motor windings (field-weakening region operating point ③)

In this post-fault conditions, first test was conducted to prove the effectiveness of the proposed control strategy when a balanced power sharing between the two windings {1} and {2} is required, and minimization of inverter losses is realized by switching off one of the remaining three healthy VSIs.

Fig. 6.21 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, $k_v^{(1)}$ turns to 1) and when the first post-fault strategy is applied (t = 60 ms, $k_v^{(2)}$ turns to 1), according to conditions Eqs. 3 and Eqs. 4 introduced in sub-section 6.3.1.A. The current sharing coefficient k_i remains unchanged.

Fig. 6.21 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as it should be.

Fig. 6.22 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. When the fault occurs on inverter $VSI_L^{(1)}$, the corresponding voltage $v_{L1}^{(1)}$ goes to zero, whereas the voltage on the other side of winding {1}, $v_{H1}^{(1)}$, doubles its value to provide for the missing winding voltage.

Voltages $v_{H1}^{(2)}$ and $v_{L1}^{(2)}$ are unaffected by the fault, being applied to the other winding. As the first post-fault strategy is applied, $VSI_L^{(2)}$ is turned off by setting $v_{L1}^{(2)}$ to zero, and the voltage $v_{H1}^{(2)}$ doubles its value to provide for the missing voltage on winding {2}. The remaining active inverters $VSI_H^{(1)}$ and $VSI_H^{(2)}$ provide now the voltages $v_{H1}^{(1)}$ and $v_{H1}^{(2)}$ with same amplitudes and the proper 30° phase shift.

Fig. 6.23 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. As expected, multilevel stepped waveforms appear now with 5 levels, as for traditional 2-level inverters, being the modulation index lower than 50% (inner hexagon shown in Fig. 6.3b).

The six stator winding currents are shown in the same Fig. 6.23, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. Note that both voltages and currents are practically unaffected by the fault and by the power sharing transients, as expected.

Fig. 6.24 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. It can be clearly seen from low-pass filtered dc currents, the total motor power is equally shared between inverters $VSI_H^{(1)}$ and $VSI_H^{(2)}$ in this first post-fault control strategy, according to Eqs. 4.

It can be notified from the time scaled average values of artificial line-to-neutral, stator winding phase voltages and/or six-phase currents, the frequency of operational cycles are doubled in respect to the operating test point ② (shown in Fig. 6.14-6.15), which illustrates the confirmation of operation in flux-weakening region and holds the same power (shown in Fig. 6.16).

6.4.3B Balanced power sharing between the three healthy VSIs (field-weakening region operating point ③)

In this post-fault conditions, second test was conducted to prove the effectiveness of the proposed control strategy when a balanced power sharing among the remaining three healthy VSIs is required (i.e., balanced power sharing among the corresponding three dc sources).

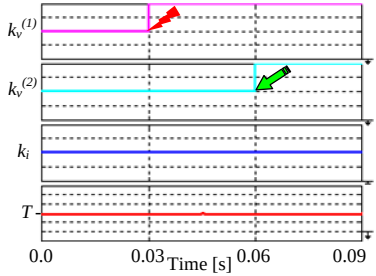


Fig. 6.21: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

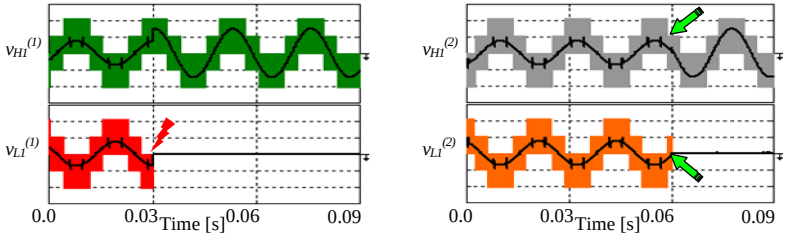


Fig. 6.22: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

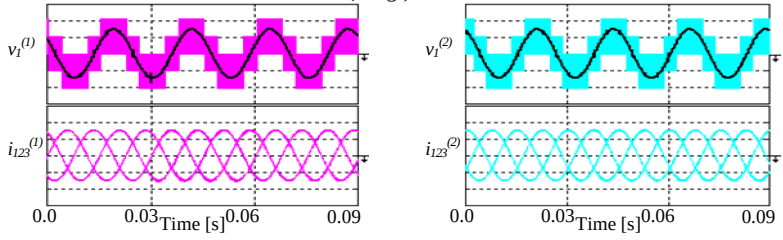


Fig. 6.23: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

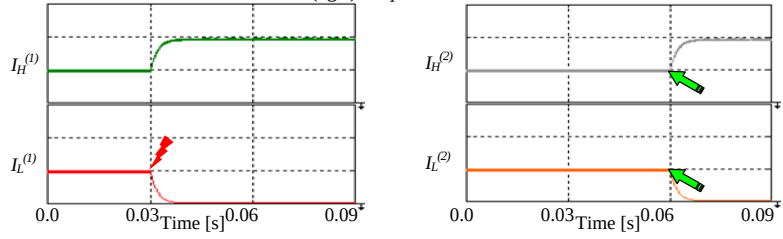


Fig. 6.24: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

Fig. 6.25 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, $k_v^{(1)}$ turns to 1) and when the second post-fault strategy is applied (t = 60 ms, k_i turns to 1/3), according to conditions Eqs. 3 and Eqs. 4 introduced in sub-section 6.3.1.A. The current sharing coefficient k_i remains unchanged.

Fig. 6.25 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as it should be.

Fig. 6.26 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. When the fault occurs on inverter $VSI_L^{(1)}$, the corresponding voltage $v_{L1}^{(1)}$ goes to zero, whereas the voltage on the other side of winding {1}, $v_{H1}^{(1)}$, doubles its value to provide for the missing winding voltage.

Voltages $v_{H1}^{(2)}$ and $v_{L1}^{(2)}$ are unaffected by the fault, being applied to the other winding, as in the previous test. As the second post-fault strategy is applied, voltages $v_{H1}^{(1)}$, $v_{H1}^{(2)}$, and $v_{L1}^{(2)}$ just slightly change as a consequences of the change of the current sharing coefficient. In fact, just a small variation of stator winding voltages can be responsible of considerable currents changes.

Fig. 6.27 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. Also in this case, multilevel stepped waveforms appear with 5 levels, as for traditional 2-level inverters, being the modulation index lower than 50% (inner hexagon shown in Fig. 6.3b). The slight voltage variation introduced by the current sharing coefficient change can now be better observed.

The six stator winding currents are shown in the same Fig. 6.27, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. The current sharing coefficient change from 1/2 to 1/3 leads to an increase of currents on winding {2} and to a decrease of currents on winding {1}, becoming ones the double of the others, and according to Eqs. 7 given by chapter 5.

Fig. 6.28 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. It can be clearly seen from low-pass filtered dc currents, the total motor power is equally shared among inverters $VSI_H^{(1)}$, $VSI_H^{(2)}$, and $VSI_L^{(2)}$ in this second post-fault control strategy, according to Eqs. 6.

In similar to the first test in this investigation, the time scaled average values of artificial line-to-neutral, stator winding phase voltages and/or six-phase currents, the frequency of operational cycle are doubled in respect to the operating test point ②

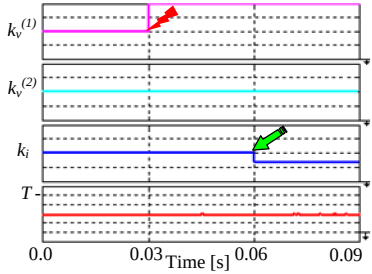


Fig. 6.25: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

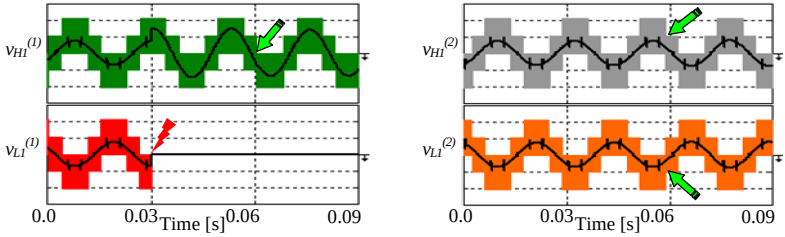


Fig. 6.26: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

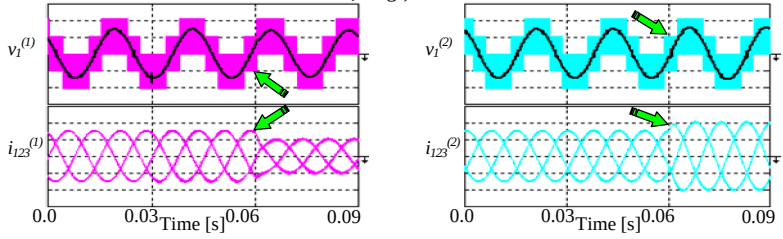


Fig. 6.27: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

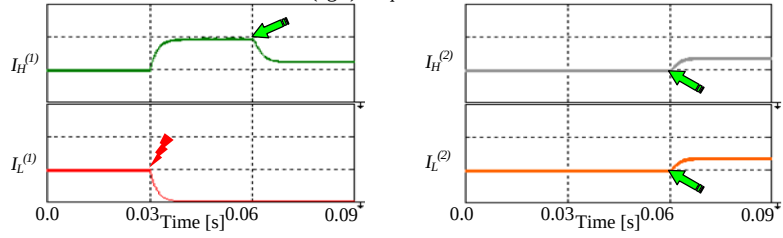


Fig. 6.28: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

(shown in Fig. 6.18-6.19), which illustrates the confirmation of operation in flux-weakening region and holds the same power (shown in Fig. 6.20).

6.4.4 Investigation performances during post-fault conditions with two failed inverter (operating point ③)

In this simulation tests, depicted in Figs. 6.29-6.32, the system is analyzed with healthy state in the first time interval [0-30 ms] considering the operating point ③ in Fig. 6.2 (speed, 1200 rpm, halved torque, 19 Nm) and the flux reference was kept at the rated value for maximizing the output phase voltage. At the time instant t = 30 ms the fault on inverters $VSI_H^{(2)}$, $VSI_L^{(2)}$ occurs, and it is completely disabled by setting to 1 current sharing coefficient k_i, as expressed by Eqs. 7. No further actions are taken in the time interval [30-90] ms, according to the description given in sub-Sections 6.3.2 and investigated the proposed control strategy performances. Fig. 6.29 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, k_i turns to 1) and according to conditions Eqs. 7 introduced in sub-Sections 6.3.2. The voltage sharing coefficients $k_v^{(1)} = k_v^{(2)} = 0.5$, remains unchanged, showing the balanced power sharing between inverters $VSI_H^{(1)}$ and $VSI_L^{(1)}$

Fig. 6.29 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as expected and it should be.

Fig. 6.30 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams.

Fig. 6.31 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. As expected, proper multilevel stepped waveforms appear with 9 levels, being the modulation index greater than 50% (outer hexagon shown in Fig. 6.3a).

The six stator winding currents are shown in the same Fig. 6.31, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. When the fault occurs on inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, the corresponding currents $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$ in winding {2} goes to zero, whereas the current $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$ in winding {1}, doubles its value to provide for the missing winding currents to maintain the required torque constant, according to Eqs. 7 given by chapter 5.

Voltages $v_{H1}^{(1)}$, $v_{L1}^{(1)}$ and its corresponding currents $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$ in winding {1} are unaffected by the fault, being applied to the other winding {2}. Fig. 6.16 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. It can be clearly seen from low-pass filtered dc currents, the total motor power is provided by and equally shared between inverters

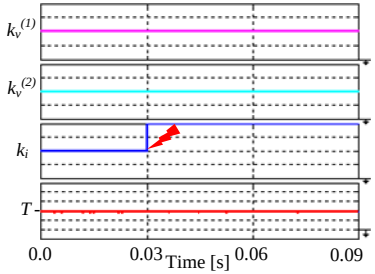


Fig. 6.29: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

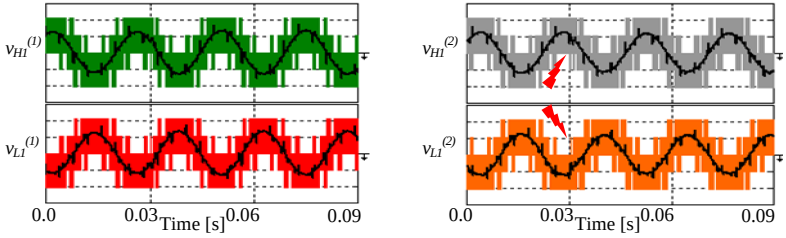


Fig. 6.30: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

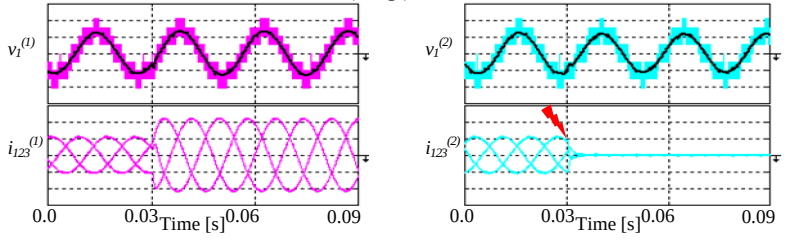


Fig. 6.31: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

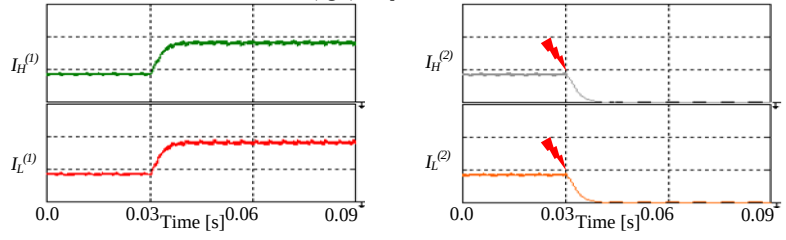


Fig. 6.32: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

$VSI_H^{(1)}$ and $VSI_L^{(1)}$, whereas inverters $VSI_H^{(2)}$, $VSI_L^{(2)}$ provides null in this post-fault control strategy, according to Eqs. 8.

Hence, the stator winding {2} voltage: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$, $v_1^{(2)}$ provided by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, are practically an open-circuit voltages.

6.4.5 Investigation performances during post-fault conditions with three failed inverter (operating point ④)

In this simulation tests, depicted in Figs. 6.33-6.36, the system is analyzed with healthy state in the first time interval [0-30 ms] considering the operating point ④ in Fig. 6.2 (halved speed, 600 rpm, halved torque, 19 Nm) and the flux reference was kept at the rated value for maximizing the output phase voltage. At the time instant t = 30 ms the fault on inverters $VSI_L^{(1)}$, $VSI_H^{(2)}$, $VSI_L^{(2)}$ occurs, and it is completely disabled by setting to 1, sharing coefficient $k_v^{(1)}$, k_i, as expressed by Eqs. 9. No further actions are taken in the time interval [30-90] ms, according to the description given in sub-Sections 6.3.3 and investigated the proposed control strategy performances.

Fig. 6.33 shows the variation of voltage and current sharing coefficients when the fault occurs (t = 30 ms, $k_v^{(1)}$, k_i turns to 1) and according to conditions Eqs. 10 introduced in sub-Section 6.3.3. The voltage sharing coefficient $k_v^{(2)}$ = 0.5, remains unchanged, showing the fault on inverters $VSI_L^{(1)}$, $VSI_H^{(2)}$, $VSI_L^{(2)}$.

Fig. 6.33 (bottom-red trace), shows that the electromagnetic torque T is practically unaffected by transients in sharing coefficients, as expected and it should be.

Fig. 6.34 shows the waveforms of artificial line-to-neutral voltages of the first-phase, dual-inverter {1}: $v_{H1}^{(1)}$, $v_{L1}^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$; (right: top-grey, bottom-orange; traces) respectively. The time scaled averaged voltage values are also depicted on the corresponding diagrams. When the fault occurs on inverter $VSI_L^{(1)}$, the corresponding voltage $v_{L1}^{(1)}$ goes to zero, whereas the voltage on the other side of winding {1}, $v_{H1}^{(1)}$, four times it value to provide for the missing winding voltage of $v_{L1}^{(1)}$ in {1} and $v_{H1}^{(2)}$, $v_{L1}^{(2)}$ in winding {2}.

Fig. 6.35 shows the stator windings voltages of the first-phase, along with their time scaled averaged values in the same diagram, $v_1^{(1)}$; (left: top-purple; trace) and $v_1^{(2)}$; (right: top-turquoise; trace) respectively. As expected, multilevel stepped waveforms appear with 5 levels, being the modulation index less than 50% (inner hexagon shown in Fig. 6.3b).

The six stator winding currents are shown in the same Fig. 6.35, $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$; ($i_{123}^{(1)}$ {1}; left: bottom-purple; traces) and $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$; ($i_{123}^{(2)}$ {2}; right: bottom-turquoise; traces), respectively. When the fault occurs $VSI_H^{(2)}$, $VSI_L^{(2)}$, the corresponding currents $i_1^{(2)}$, $i_2^{(2)}$, $i_3^{(2)}$ winding {2} goes to zero, whereas the current $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$ winding {1}, doubles its value to provide for the missing winding currents for maintains the required torque constant, according to Eqs. 7 given by chapter 5.

Voltage $v_{H1}^{(1)}$ and its corresponding currents $i_1^{(1)}$, $i_2^{(1)}$, $i_3^{(1)}$ winding {1} are unaffected by the fault, being applied to the both winding {1} and {2}.

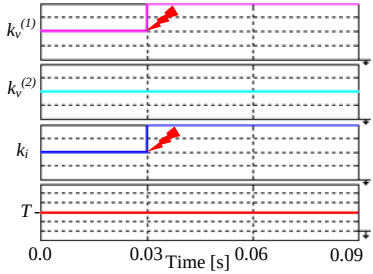


Fig. 6.33: Three degree of freedom, torque waveforms. From top-to-bottom: voltage and current sharing coefficients [0.25units/div]; Torque behavior in healthy-state to post-fault conditions [10Nm/div].

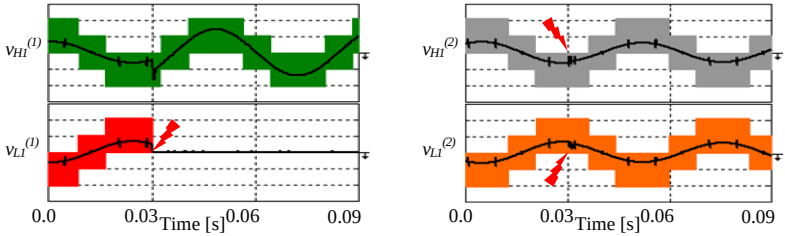


Fig. 6.34: Artificial line-to-neutral voltages (first-phase) with their time scaled average components [100V/div]. From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces.

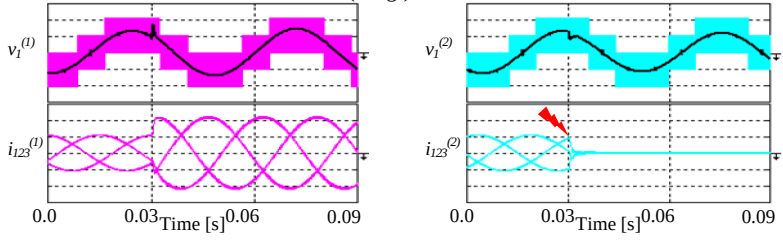


Fig. 6.35: Stator variables on windings {1} and {2}. From top-to-bottom: First-phase voltage with time scaled average components [100V/div], currents [10A/div]: dual-inverter {1} (left): purple traces; dual-inverter {2} (right): turquoise traces.

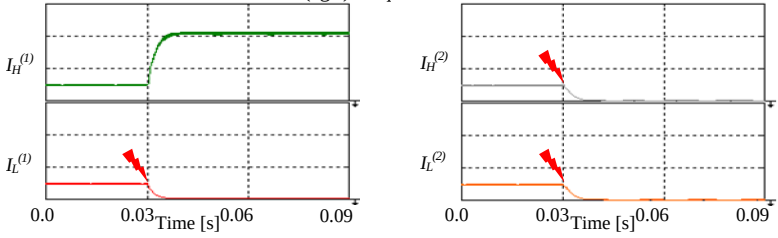


Fig. 6.36: DC currents (low-pass filtered, τ=20 ms). From top-to-bottom: dual-inverter {1} (left): H (green) and L (red) traces; dual-inverter {2} (right): H (gray) and L (orange) traces [5A/div].

Fig. 6.36 shows the dc currents of the four VSIs (currents from the dc supplies), dual-inverter {1}: $I_H^{(1)}$, $I_L^{(1)}$; (left: top-green, bottom-red; traces) and dual-inverter {2}: $I_H^{(2)}$, $I_L^{(2)}$; (right: top-grey, bottom-orange; traces), respectively. It can be clearly seen from low-pass filtered dc currents, the total motor power is provided by inverter $VSI_H^{(1)}$ whereas inverters $VSI_L^{(1)}$, $VSI_H^{(2)}$, $VSI_L^{(2)}$ provides null in this post-fault control strategy, according to Eqs. 10.

Hence, the stator winding {2} voltage: $v_{H1}^{(2)}$, $v_{L1}^{(2)}$, $v_1^{(2)}$ provided by inverters $VSI_H^{(2)}$ and $VSI_L^{(2)}$, are practically an open-circuit voltages.

6.5 Conclusion

Fault tolerance capabilities of proposed multiphase-multilevel ac motor were investigated in this chapter and developed some post-fault control strategies after detailed theoretical studies. The quad-inverter system capable to generate multilevel voltage waveforms, which equivalent to the ones of a 3-level inverter during healthy state. Also it has been shown that during proposed post-fault operating conditions, in particular with one, two, or three VSI failed, the total power rating is reduced to the half and consecutively one-by-one degree of freedom in total power sharing is lost. More specifically, the control strategy can be exploited for maximum redundancy for continue the operable condition of the motor even with three VSI failed.

Complete theoretical background characteristics of the entire ac motor drive are provided for each post-fault conditions and set of numerical simulation results are presented to show the most effectiveness of the proposed post-fault control strategies, and some of the results presented in this chapter are accepted for publication in conference proceeding [120].

7. Hardware implementation and experimental results

7.1 Introduction

In this chapter, presents the comprehensive hardware prototype model implementation of multiphase-multilevel inverter (quad-inverter configuration) for two three-phase open-winding loads. The control aspect in open-loop scheme based on inverse three-phase space vector approach was developed using two TMS320F2812 DSP controllers working with McBSP protocol for PWM communication and synchronization, for modulating quad-inverter system and controlled output waveforms. A simplified PWM technique (independent and level-shifted multilevel modulation) was adopted, allowing the total power sharing with three degree of freedom. Complete set of experimental results are given with reference to both balanced and unbalanced operating conditions.

7.2 Full-scale low-voltage high-current hardware prototype implementation

Multiphase-multilevel inverter (six-phase quad-inverter) for open-end winding loads, as a full-scale low-voltage high-current prototype model was implemented. A picture of the working area is given in Fig. 7.1. The system consists in two processor boards, including a TMS320F2812 DSP each, as depicted in Fig. 7.2. The DSP-{1} board acts a master unit, performing all the calculations required by the control scheme given by chapter 4 (shown in Fig. 4.5), and providing for the firing signals of inverters $H^{(1)}$ and $L^{(1)}$ by its own internal PWM unit. The DSP-{2} board acts a slave unit, receiving the modulating signals from the DSP-{1} by the multi-channel buffered serial port (McBSP data cable connection shown in Fig. 7.3). DSP-{2} provides for the firing signals of inverters $H^{(2)}$ and $L^{(2)}$ by its own internal PWM unit [122].

7.3 McBSP serial communication protocol implementation

The McBSP (Multi-channel buffered serial port) communication protocols of DSP TMS320F2812 provides the peripheral interface between DSPs devices and transmit/receive synchronous compatibility with 8/12/16/20/24 or 32 bits-serial datas and schematic shown in Fig. 7.3. The main advantage of McBSP communication protocol utilized for this experimental activity for the implementation of quad-inverter PWM

Keywords**:** *Multiphase-multilevel ac motor, dual three-phase induction motor, fault-tolerance, and multilevel space vector modulation.*

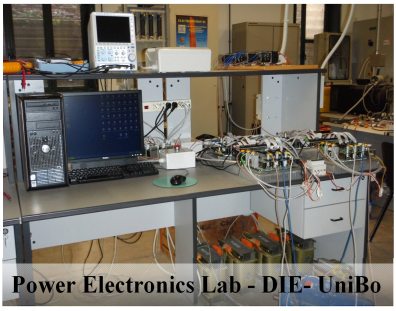


Fig. 7.1: Overall view of the working area in the Lab.

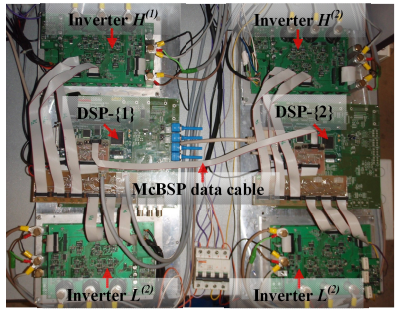


Fig. 7.2: Top view of the main system boards.

communication and interface between two DSPs with synchronization are [123]:

- Full-duplex communication.
- Double-buffered transmission and triple-buffered reception, which allow a continuous data stream.
- Independent clocking and framing for reception and for transmission.
- Time division multiplexer (TDM) 128 channels for transmission and6 for reception.
- Multi-channel selection modes that enable you to allow or block transfers in each of the channels.
- DMA replaced with two 16-level, 32-bit first-input first-out (FIFOs).
- Direct interface to industry-standard codec, analog interface chips (AICs), and other serially connected A/D and D/A devices.
- Support for external generation of clock signals and frame-synchronization (frame-sync) signals.
- A programmable sample rate generator for internal generation

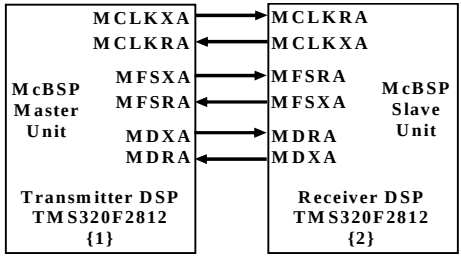


Fig. 7.3: Schematic diagram of McBSP data cable communication protocol channel between two DSP TMS320F2812 controllers {1} and {2}.

and control of frame-sync signals.
- Programmable internal clock and frame generation.
- Programmable polarity for frame-synchronization and data clocks and support for SPI devices.
- Maximum I/O pin buffer speed is limited to 20MHz.

Two DSP controllers are synchronized with proper communication for transmitting/receiving the signals by setting proper frame period, frame pulse-width of frame synchronization generator, sample rate clock division and transmitter/receiver interrupts of the McBSP protocol unit [124]. In detail, transmitter/receiver is configured in reset at the beginning of initialization, and then the McBSP is programmed for desired transmitter/receiver operation. Finally the McBSP transmitter/receiver is taken out of reset after two clock cycle of the sample rate generator clock cycle. In DSP-{1} McBSP transmitter frame is configured with single-phase, 2 words per frame of two 16-bit data for transmitting (modulating signal in stationary reference frame) to DSP-{2} and receiver frame is configured with single-phase, 1 words per frame of one 16-bit data for receiving enable reception from DSP-{2} slave unit. In DSP-{2} McBSP receiver frame is configured with single-phase, 2 words per frame of two 16-bit data for receiving (modulating signal in stationary reference frame) from DSP-{1} and transmitter frame is configured with single-phase, 1 words per frame of one 16-bit data for transmitting enable reception to DSP-{1} master unit.

Rising edge of the transmitter clock pin generates the transmission of the data and falling edge of the receiver clock pin generates the reception of the data in the both master/slave DSP McBSP configuration with transmitting/receiving the data in 2-bit data delay. The McBSP sends a receiver interrupt request to the CPU when each receive frame-synchronization pulse is detected and in reset state as well. Transmitter generates an interrupt request to the CPU when new frame synchronization occurs. In this way both master DSP-{1} and slave DSP-{2} transmit/receive the data with proper synchronization and hand-shake [122-123].

7.4 Experimental results and discussion

A complete set of open-loop (shown in Fig. 4.5) experimental results is presented in this section using independent and level-shifted modulation techniques, on the basis of the numerical simulations results given in chapter 4 and 5, with reference to balanced and unbalanced operating conditions. The main parameters of the four 2-level VSIs together with load parameters are given in Table 7.1. For the sake of simplicity,

Table 7.1: Main parameters of four inverters and six-phase load.

MOSFETs (6 in parallel per switch)	Vishay SiliconixSUM85N15-19
MOSFET ratings	V_{DSS}=150 [V]; R_{DS}=19[mΩ]@V_{GS}=10[V]; I_D=85[A]
switching frequency	2 [kHz]
dc-bus capacitance (4 banks)	12 [mF]
dc-bus voltage (4 in all)	52 [V]
load impedance (open ends, 6 in all)	6 [Ω]
load power factor (angle)	0.67 (48°)
load rated current	10 [A]

experimental tests are carried out by using a system of six balanced impedances (passive load) as open-winding loads. Inverters are modulated here without multilevel output voltage optimization and a phase angle of 30° is set as the displacement between the output voltages of the two dual three-phase inverters. In the next section, experimental results relating the balanced and unbalanced operating conditions are discussed in detail.

7.4.1 Independent modulation scheme

In the first experimental test (Figs. 7.4-7.6), conducted to illustrate the behavior of the system in balanced conditions with modulation indexes $m^{(1)} = m^{(2)} = 0.75$, corresponding to a current ratio $k_i = 1/2$ (balanced currents), and voltage ratios $k_v^{(1)} = k_v^{(2)} = 1/2$ (balanced voltages).

In this operating condition the total power is equally shared among the four VSIs, and individual modulation indexes from chapter 4 (Eqs. 3 and 4) are $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = m_L^{(2)} = 0.75$.

Fig. 7.4 depicts line-to-line voltages (H and L), artificial line-to-neutral voltages (H and L), and load phase voltage (calculated) for the two dual-inverters {1} and {2}. Fig. 7.5 shows artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual-inverters {1} and {2}.

All the six-phase output currents are shown in Fig. 7.6. It should be noted that the currents are almost sinusoidal; practically with same amplitude and correct phase angle displacement (load impedances are not perfectly balanced).

In the second experimental test (Fig. 7.7), conducted to illustrate the behavior of the system in unbalanced conditions to verify the power sharing capability between the two inverters H and L of the two dual-inverter {1} and {2}. In particular, modulation indexes $m^{(1)} = m^{(2)} = 0.75$ are set as in the previous case, corresponding to a current ratio $k_i = 1/2$(balanced currents),

whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 0.6$ (unbalanced voltages), leading to individual modulation indexes $m_H^{(1)} = m_H^{(2)} = 0.9$, $m_L^{(1)} = m_L^{(2)} = 0.6$, given by chapter 4 (Eqs. 3 and 4). In this operating condition inverters H supply 50% more power that inverters L.

Fig. 7.7 shows artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual-inverters {1} and {2}. As expected, fundamental voltage components of individual inverters H and L are one 50% more than the other. However, being load phase voltages the same as in previous case, load currents are the same as well.

In the third and last experimental test (Figs. 7.8-7.9), conducted to illustrate the behavior of the system in unbalanced conditions to verify the power sharing capability between the two inverters {1} and {2}.

In particular, modulation indexes $m^{(1)}$ and $m^{(2)}$ are set one the double of the other, $m^{(1)}= 0.75$, $m^{(2)}= 0.375$, corresponding to a current ratio $k_i = 2/3$ (unbalanced currents), whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 1/2$ (balanced voltages), leading to individual modulation indexes $m_H^{(1)}= m_L^{(1)}= 0.75$, $m_H^{(2)}= m_L^{(2)}= 0.375$, given by chapter 4 (Eqs. 3 and 4). In this operating condition inverter {1} supplies 50% more power that inverter {2}.

Fig. 7.8 shows artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual three-phase inverters {1} and {2}. As expected, fundamental voltage components of inverters {1} and {2} are one the double of the other, providing load currents with the same ratio, corresponding to $k_i = 2/3$.

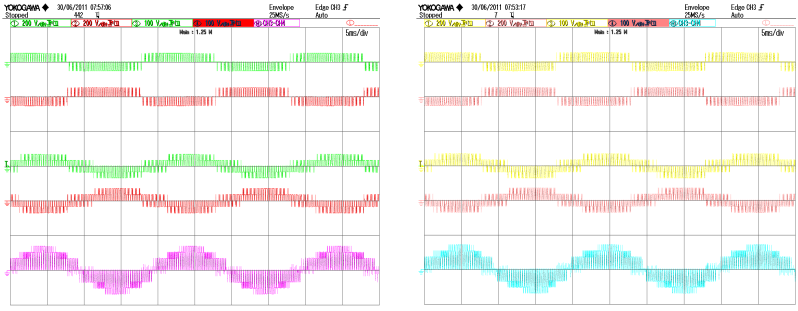
All the six-phase output currents are shown in Fig. 7.9. Also in this case, currents are practically sinusoidal, with an almost correct phase angle displacement (even if load impedances are not perfectly balanced). As expected, the currents supplied by inverter {1} have an amplitude double of the currents supplied by inverter {2}.

7.4.2 Level-shifted multilevel modulation (third harmonic injection scheme)

In the first experimental test (Figs. 7.10-7.12), conducted to illustrate the behavior of the system in balanced conditions with modulation indexes $m^{(1)} = m^{(2)} =0.75$, corresponding to a current ratio $k_i=1/2$ (balanced currents), and voltage ratios $k_v^{(1)} = k_v^{(2)} =1/2$ (balanced voltages).

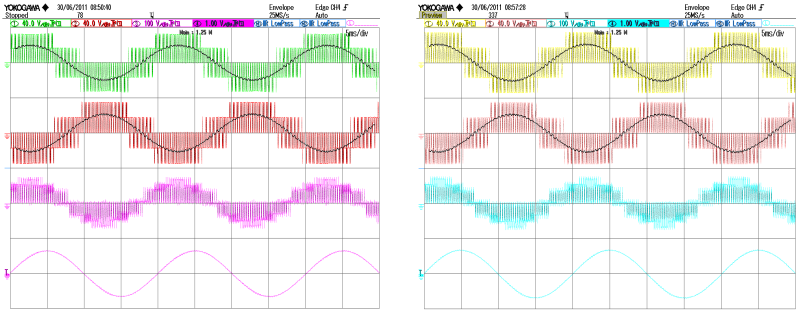
In this operating condition the total power is equally shared among the four VSIs, and individual modulation indexes from chapter 4 (Eqs. 3 and 4) are $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = m_L^{(2)} = 0.75$.

Fig. 7.10 depicts line-to-line voltages (H and L), artificial line-to-neutral voltages (H and L), and multi-stepped load phase voltage (calculated) for



{1} {2}

Fig. 7.4: Voltage waveforms of the two dual three-phase inverters {1} and {2} in balanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: line-to-line voltages (H and L), artificial line-to-neutral voltages (H and L), and load phase voltage (calculated).



{1} {2}

Fig. 7.5: Voltage, current, and filtered waveforms of inverters {1} and {2} in balanced conditions. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

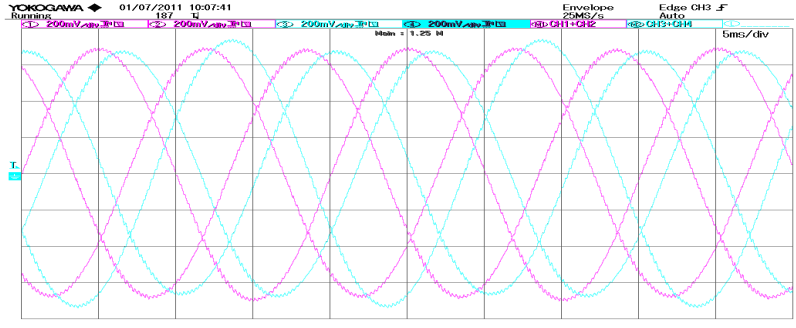
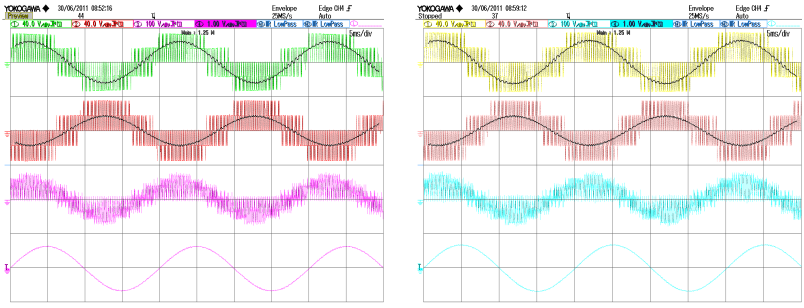
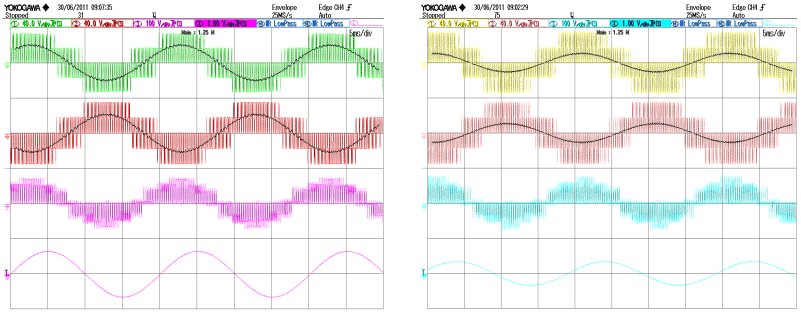


Fig. 7.6: Six-phase load currents waveform in balanced condition: dual-inverter {1}: purple traces (2 measured, 1 calculated); dual-inverter {2}: turquoise traces (2 measured, 1 calculated).



{1} {2}

Fig. 7.7: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.60$. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.



{1} {2}

Fig. 7.8: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = 0.75$, $m^{(2)} = 0.375$ ($k_i = 2/3$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

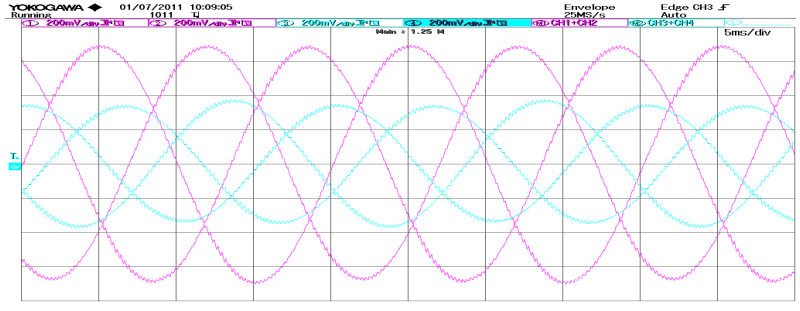


Fig. 7.9: Six-phase load currents waveform in unbalanced condition: dual-inverter {1}: purple traces (2 measured, 1 calculated); dual-inverter {2}: turquoise traces (2 measured, 1 calculated).

the two dual-inverters {1} and {2}. Fig. 7.11 shows artificial line-to-neutral voltages (H and L), multi-stepped load phase voltage (measured) and current for the two dual three-phase inverters {1} and {2}. To be noticed, artificial line-to-neutral voltages are not symmetrical in a cycle has the voltage is shared between inverters (H and L) in a half cycle of the fundamental period, but difference in voltages lead to the multi- stepped waveform in the output load phase voltages.

All the six-phase output currents are shown in Fig. 7.12. It should be noted that the currents are almost sinusoidal; practically with same amplitude and correct phase angle displacement (load impedances are not perfectly balanced).

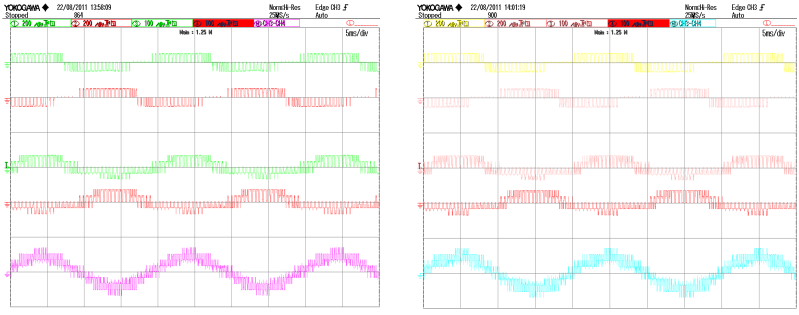
In the second experimental test (Fig. 7.13), conducted to illustrate the behavior of the system in unbalanced conditions to verify the power sharing capability between the two inverters H and L of the two dual-inverter {1} and {2}. In particular, modulation indexes $m^{(1)} = m^{(2)} = 0.75$ are set as in the previous case, corresponding to a current ratio $k_i = 1/2$ (balanced currents), whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 0.6$ (unbalanced voltages), leading to individual modulation indexes $m_H^{(1)} = m_H^{(2)} = 0.9$, $m_L^{(1)} = m_L^{(2)} = 0.6$, given by chapter 4 (Eqs. 3 and 4). In this operating condition inverters H supply 50% more power that inverters L.

Fig. 7.13 shows artificial line-to-neutral voltages (H and L) and their fundamental components, multi-stepped load phase voltage (measured) and current for the two dual-inverters {1} and {2}. As expected, fundamental voltage components of individual inverters H and L are one 50% more than the other. However, being load phase voltages the same as in previous case, load currents are the same as well.

In the third and last experimental test (Figs. 7.14-7.15), conducted to illustrate the behavior of the system in unbalanced conditions to verify the power sharing capability between the two inverters {1} and {2}.

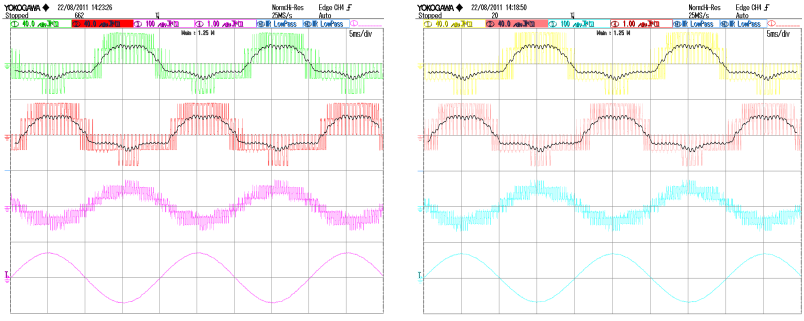
In particular, modulation indexes $m^{(1)}$ and $m^{(2)}$ are set one the double of the other, $m^{(1)}=0.75$, $m^{(2)}=0.375$, corresponding to a current ratio $k_i=2/3$ (unbalanced currents), whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 1/2$ (balanced voltages), leading to individual modulation indexes $m_H^{(1)} = m_L^{(1)} = 0.75$, $m_H^{(2)} = m_L^{(2)} = 0.375$, given by chapter 4 (Eqs. 3 and 4). In this operating condition dual-inverters {1} supplies 50% more power that dual-inverter {2}.

Fig. 7.14 shows artificial line-to-neutral voltages (H and L), multi-stepped load phase voltage (measured) and current for the two dual-inverters {1} and {2}. As expected, fundamental voltage components of dual-inverters {1} and {2} are one the double of the other, providing load currents with the same ratio, corresponding to $k_i=2/3$.



{1} {2}

Fig. 7.10: Voltage waveforms of the two dual three-phase inverters {1} and {2} in balanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: line-to-line voltages (H and L), artificial line-to-neutral voltages (H and L), and load phase voltage (calculated).



{1} {2}

Fig. 7.11: Voltage, current, and filtered waveforms of inverters {1} and {2} in balanced conditions. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

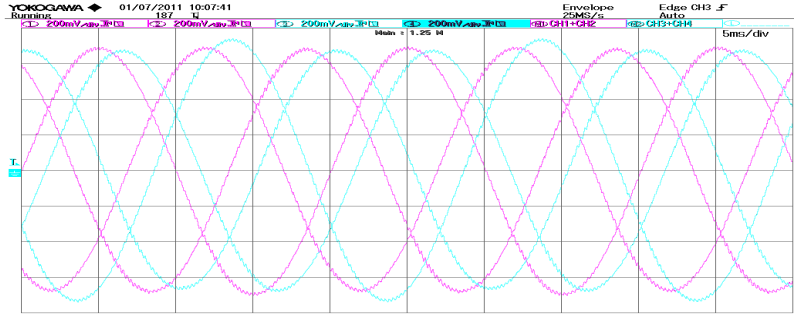
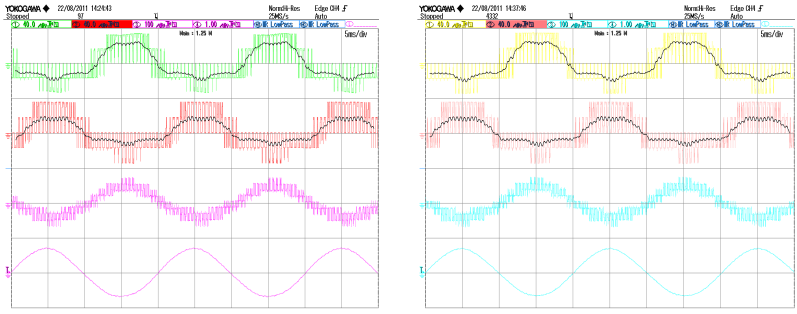
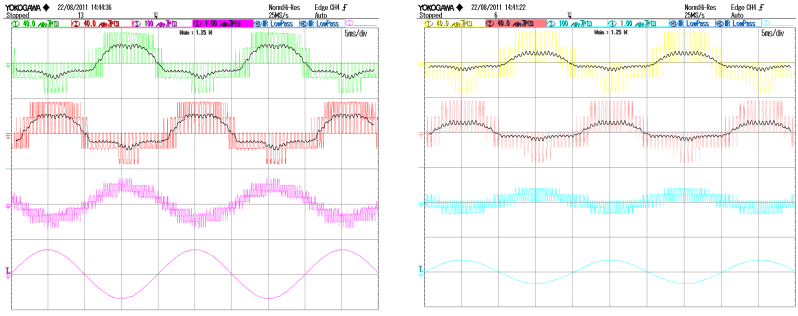


Fig. 7.12: Six-phase load currents waveform in balanced condition: dual-inverter {1}: purple traces (2 measured, 1 calculated); dual-inverter {2}: turquoise traces (2 measured, 1 calculated).



{1} {2}

Fig. 7.13: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.60$. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.



{1} {2}

Fig. 7.14: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = 0.75$, $m^{(2)} = 0.375$ ($k_i = 2/3$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: artificial line-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

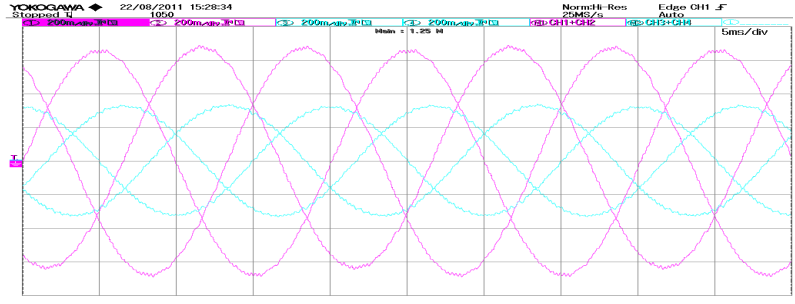


Fig. 7.15: Six-phase load currents waveform in unbalanced condition: dual-inverter {1}: purple traces (2 measured, 1 calculated); dual-inverter {2}: turquoise traces (2 measured, 1 calculated).

All the six-phase output currents are shown in Fig. 7.15. Also in this case, currents are practically sinusoidal, with an almost correct phase angle displacement (even if load impedances are not perfectly balanced). As expected, the currents supplied by inverter {1} have an amplitude double of the currents supplied by inverter {2}.

The main drawback of this level-shifted modulation scheme, power is shared in half cycle of the fundamental period and this asymmetric leads (Fig. 7.11, Fig. 7.14 artificial phase voltage) to have more harmonics content in output and it can be clearly notified from rising peak in Fig. 7.12 and Fig. 7.15.

7.5 Conclusion

Hardware prototype model of multiphase-multilevel inverters for open-winding loads was implemented in this chapter. Open-loop control scheme based on inverse three-phase space vector approach was developed using two TMS320F2812 DSP controllers. A communication algorithm based on McBSP protocol for PWM communication and synchronization was framed between two DSPs, controlling quad-inverter system for its modulation and controlled output waveforms. It has been shown that, developed control scheme shares the total power among the four dc sources with three degrees of freedom. In order to regulate the couple of 2-level VSIs supplying each three-phase winding, a simplified PWM technique (independent and level-shifted multilevel modulation) was adopted for testing under balanced and unbalanced power (voltage/current) sharing conditions.

Real time test results provided in this chapter prove the effectiveness of the proposed six-phase quad-inverter system in balanced/unbalanced operating conditions using two DSP-based TMS320F2812 controllers. Experimental results show good agreement with numerical simulation and in accordance to the theoretical developments. Some of the presented experimental results already published in referred conference proceedings [126].

Conclusions and future works

In this thesis work a new version of multiphase-multilevel ac motor drive system is proposed. It is much suitable for low-voltage high-current power applications. In detail, power section consists of four standard two-level voltage source inverters (VSIs) and asymmetrical six-phase induction motor (dual three-phase), with open-end stator windings. A dedicated control aspect based on synchronous reference frame was developed, which provides the sharing capabilities of the total motor power among the four VSIs in each switching cycle with three degree of freedom. Precisely, first degree of freedom concerns with the current sharing between two three-phase stator windings. Based on modified multilevel space vector pulse width modulation, the voltage is shared between the two VSIs feeding the same three-phase stator motor winding, leading to the second and the third degree of freedom.

The proposed multiphase-multilevel inverter was implemented in numerical simulation by PLECS software with some carrier-based pulse width modulation for showing its output multilevel waveforms. Control algorithm based on inverse three-phase space vector decomposition approach in open-loop scheme, has been provided with set of results in respect to theoretical aspect for showing its benefits and drawback of each PWM techniques.

Comprehensive model of ac motor drive system based on three-phase space vector decomposition approach was developed in PLECS - numerical simulation software working in MATLAB environment. Proposed synchronous reference control algorithm was framed in MATLAB with modified multilevel space vector pulse width modulator. The effectiveness of the entire ac motor drives system was tested. Simulation results are given in detail to show symmetrical and asymmetrical, power sharing conditions. Furthermore, fault-tolerant capabilities of the entire ac drive system was tested based on developed post-fault operating condition by exploiting three degree of freedom. Complete set of simulation results are provided when one, two and three VSIs are faulty.

Hardware prototype model of the quad-inverter conversion system was implemented with two three-phase passive loads in open-end configuration using two TMS320F2812 DSP controllers. The developed McBSP (multi-channel buffered serial port) communication algorithm was able to control the four VSIs for PWM communication and synchronization. Open-loop control scheme based on inverse three-phase decomposition approach was proposed to control entire quad-inverter configuration and tested in both balanced and unbalanced operating conditions with simplified PWM techniques.

Both simulation and experimental results were in good agreement with theoretical developments, in all considered cases.

A prototype of the multiphase-multilevel inverter with two three-phase passive loads in open-end configuration was implemented and analyzed using two DSP TMS320F2812 controllers. Furthermore, for future research work keeps open with many interesting tasks such as:

- Complete realization of proposed closed-loop control system for whole ac motor drive system based on synchronous reference frame, using two DSP TMS320F2812 process controllers.

- Developments of switching PWM techniques for optimized multi-level output waveforms using different and improved multilevel space vector modulation schemes.

- Extending the sharing capabilities of quad-inverter in one switching cycle, i.e., all the four VSIs with operating single multilevel space vector modulator.

- Investigation for control dynamics of the proposed ac drive system based on different control techniques, in particular to stationary reference frame orientations and direct torque control etc.

- Investigation of multiphase-multilevel inverter as active filter, for grid-connected applications, such as renewable power generation.

- Possibility to increase the number of phases and to investigate the redundancy operation when n = 9, 12,… for the proposed multiphase-multilevel inverter.

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Appendix

Facilities for conducted prototype model experimental test setup and expandable for future applications. Module fully developed with Power Electronics Laboratory,
Department of Electrical Engineering, University of Bologna, (IT).

Low-voltage high-current prototype model of Quad-Inverter configuration unit with two three-phase open-winding loads
Specifications:
DC-link capacitor of each two-level three-phase voltage source inverter: 12mH/100v.
DC bus voltage of each two-level three-phase voltage source inverter: 100v (maximum).
Current rating: 25x6=150A (6 MOSFETs in parallel combination to form each switch configuration).

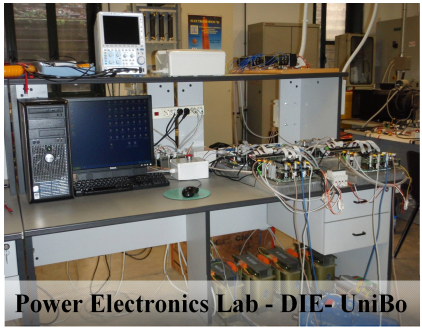

Fig. A.1: Overall view of the working area in the Lab.

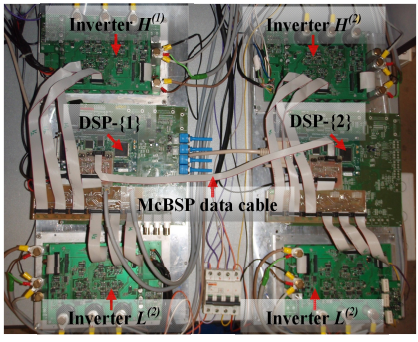

Fig. A.2: Top view of the main system boards.

Power section unit
Specifications:
Step-down transformers: Three-phase, 440v/75v (rms), 50/60Hz, 5000vA. Four units. [Type: Star connection].
Bridge diode rectifiers: Three-phase, 1200v (rms), 63A (rms). Four units. [Module: IXYS VU062-12N07].

Fig. A.3: Three-phase transformers. (Four in number).

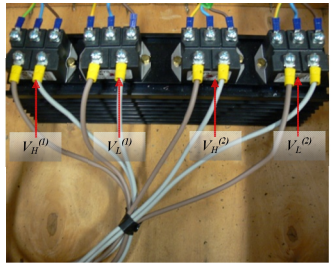

Fig. A.4: DC power sources. (Four in number).

Protection circuitry section unit
Specifications:
Contactor protection for four dc bus links for inverters: Module - SW200-460. [Type: Normally open].
Fuse: 300v/16A (rms).
Power supply for the driver unit consists of four three-phase transformers with four three-phase diode bridge rectifier units.
Step-down transformers: Single-phase, 400v/55v-0v-55v (rms), 50Hz. [Module ST 53363].
Diode bridge rectifier: 560v (rms), 25A (rms). [Module DB 25-08].

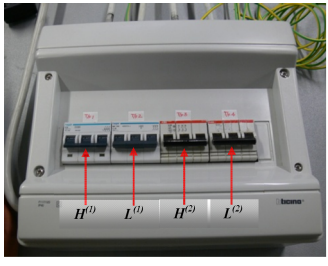

Fig. A.5: Main power circuit breakers. (Four in number).

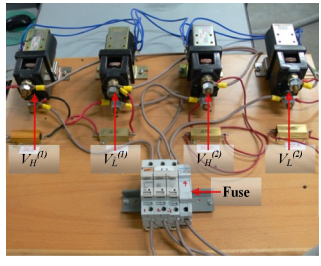

Fig. A.6: Contactor protection for dc bus links. (Four in number).

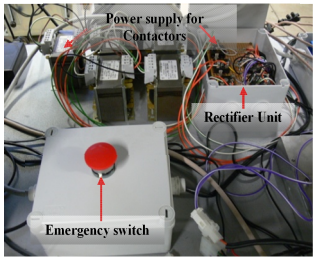

Fig. A.7: Protection unit with emergency switch control.

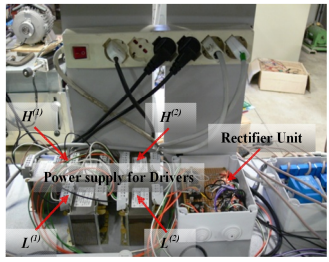

Fig. A.8: Power supply unit for drivers and contactors.

Voltage and current sensing section unit
Specifications:
Voltage sensor: Sensing maximum 135v dc. Each unit has two dc sensors. [Module LV25-P].
Current sensor: Sensing maximum 70A peak ac current. Each unit has three ac current sensors. [Module LA55-P].

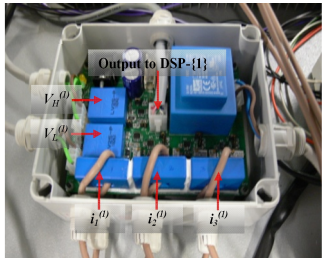

Fig. A.9: Voltage and current sensing unit {1}.

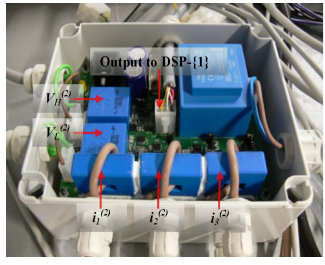

Fig. A.10: Voltage and current sensing unit {2}.

Controller section unit (Master/Slave DSP TMS320F2812)

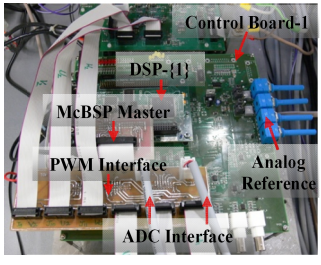

Fig. A.11: TMS320F2812 master DSP-{1} control unit.

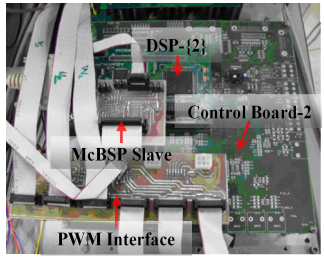

Fig. A.12: TMS320F2812 slave DSP-{2} control unit.

Experimental test specifications:

Table A.1: Experimental parameters of four inverters and six-phase load.

MOSFETs (6 in parallel per switch)	Vishay SiliconixSUM85N15-19
MOSFET ratings	V_{DSS}=150 [V]; R_{DS}=19[mΩ]@V_{GS}=10[V]; I_D=85[A]
switching frequency	2 [kHz]
dc-bus capacitance (4 banks)	12 [mF]
dc-bus voltage (4 in all)	52 [V]
load impedance (open ends, 6 in all)	6 [Ω]
load power factor (angle)	0.67 (48°)
load rated current	10 [A]

Complete setup of Quad-Inverter hardware prototype Model

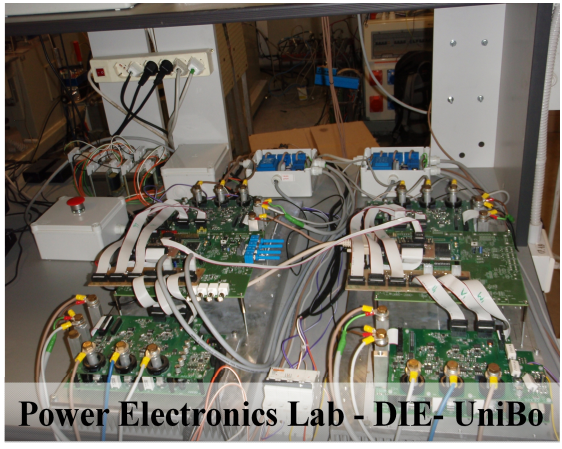

Fig. A.13: Complete setup view and facilities for quad-inverter configuration as multiphase-multilevel inverter.