Preliminary hardware implementation of a six-phase quad-inverter induction motor drive

Gabriele Grandi, Padmanaban Sanjeevikumar, Domenico Casadei DEPT. OF ELECTRICAL ENGINEERING – UNIVERSITY OF BOLOGNA viale Risorgimento 2, 40136 Bologna, Italy Ph./Fax: +39 05120935 61/88 E-Mail: <*name.surname*>@unibo.it URL: <u>http://www.die.unibo.it</u>

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Multilevel converters, Multiphase drive, Power conditioning, Converter control, Voltage Source Inverters (VSI).

Abstract

A hardware implementation of a quad-inverter configuration for multi-phase multi-level induction motor drives is presented in this paper. The scheme is based on four conventional 2-level three-phase voltage source inverters, able to supply the open-end windings of a dual three-phase motor (asymmetric six-phase machine), quadrupling the power capability of a single VSI with given voltage and current ratings. By a proper control algorithm the proposed converter is able to generate multi-level voltage waveforms, equivalent to the ones of a 3-level inverter, and to share the total motor power among the four dc sources within each switching period. A full-scale prototype of the whole power system has been realized utilizing six balanced impedances as six-phase load. A complete set of experimental results is given with reference to both balanced and unbalanced operating conditions.

Introduction

Both multi-phase and multi-level inverter technologies have been widely recognized as a viable solution to overcome current and voltage limits of power switching converters for high-power mediumvoltage ac drives.

In more details, multi-phase motor drives have many advantages over the traditional three-phase motor drives, such as reducing the amplitude and increasing the frequency of torque pulsations, reducing the rotor harmonic current losses and lowering the dc link current harmonics. In addition, owing to their redundant structure, multi-phase motor drives improve the system reliability. As a consequence, the use of multi-phase inverters together with multi-phase ac machines has been recognized as a viable approach to obtain high power ratings with current limited devices [1]-[3].

On the other side, multi-level converters are able to generate output voltage waveforms consisting in a large number of steps. In this way, high voltages can be synthesized using sources and switching devices with lower voltage values, with the additional benefit of a reduced harmonic distortion and lower dv/dt in the output voltages. For these reasons, the use of multi-level inverters has been recognized as a viable approach to obtain high power ratings with voltage-limited devices [4]-[6].

It becomes evident that the combination of multi-phase and multi-level inverter technologies [7] could be an effective method to group the benefits of such technologies and to obtain high power ratings with both voltage- and current-limited devices.

Several conversion structures have been introduced in last decades for multi-phase and multi-level inverters. Among these structures, there are topologies based on a proper arrangement of conventional 2level three-phase voltage source inverters (VSIs) to realize both multi-phase [8]-[12] and multi-level [13]-[17] inverters, or dual-source fed multiphase induction motor drives [18]. The great advantages of such topologies are reliable power layout and effective protecting circuitry, reduced cost of both con-



Fig. 1: Schematic diagram of the proposed multi-phase multi-level induction motor drive consisting in four voltage source inverters supplying a dual three-phase machine with open-end windings.

verter and motor due to conventional slot/winding configurations, and modularity of the whole conversion structure.

In order to exploit all these advantages, a novel structure based on a dual three-phase open-ends winding motor (asymmetric six-phase induction machine) has been proposed in [19]. In this paper, the hardware implementation of this multi-phase multi-level structure is described. The power supply consists of four standard 2-level three-phase VSIs having insulated dc sources to prevent circulation of zero-sequence current components. A schematic diagram of the whole system is given in Fig. 1. Note that the structure is easy scalable to nine, twelve, or higher triplen phase numbers.

Each couple of 2-level VSIs is modulated to obtain output voltage waveforms such as a 3-level inverter, providing proper multi-level voltage waveforms for each three-phase stator winding. The control algorithm allows total motor power to be shared among the four dc sources with three degrees of freedom. Power sharing is a useful skill in battery supplied drives where the charge status of batteries should be balanced.

Dual three-phase induction motor drive

Multiple Space Vector Representation

Multiple space vectors are considered to represent the variables of the whole six-phase system consisting of the dual three-phase machine supplied by four insulated three-phase VSIs. In particular, the asymmetric six-phase space vector transformations introduced in [8], [12] are considered. The relationships between multiple space vector variables (\bar{x}_1 , \bar{x}_3 , \bar{x}_5) and the three-phase space vector variables ($\bar{x}^{(1)}$, $\bar{x}^{(2)}$) of each three-phase sub-system {1}, {2} are

$$\begin{cases} \overline{x}_{1} = \frac{1}{2} \left[\overline{x}^{(1)} + \alpha \ \overline{x}^{(2)} \right] , \quad \overline{x}_{3} = x_{0}^{(1)} + j x_{0}^{(2)} \\ \overline{x}_{5}^{*} = \frac{1}{2} \left[\overline{x}^{(1)} - \alpha \ \overline{x}^{(2)} \right] , \qquad (1) \end{cases}$$

$$\begin{cases} \overline{x}^{(1)} = \overline{x}_1 + \overline{x}_5^* \\ x_0^{(1)} = \overline{x}_3 \cdot 1 \end{cases}, \begin{cases} \overline{x}^{(2)} = \alpha^{-1} \left(\overline{x}_1 - \overline{x}_5^* \right) \\ x_0^{(2)} = \overline{x}_3 \cdot j \end{cases},$$
(2)

where the symbols "*" and " \cdot " denote complex conjugate and scalar (dot) product, respectively. The representation of the proposed multi-phase multi-level induction motor drive shown in Fig. 1 in terms of three-phase space vectors leads to the schematic equivalent circuit of Fig. 2.

Machine Model by Multiple Space Vectors

The behavior of the dual three-phase induction machine having sinusoidal distributed stator windings can be described in terms of multiple space vectors by the following equations, written in a stationary reference frame:



Fig. 2: Equivalent circuit of the whole induction motor drive in terms of three-phase space vectors.

$$\overline{v}_{S1} = R_S \,\overline{i}_{S1} + \frac{d\overline{\varphi}_{S1}}{dt} \,, \, \overline{\varphi}_{S1} = L_{S1} \,\overline{i}_{S1} + M_1 \,\overline{i}_{R1} \,, \tag{3}$$

$$0 = R_R \,\bar{i}_{R1} - j \, p \, \omega_m \,\overline{\varphi}_{R1} + \frac{d \,\overline{\varphi}_{R1}}{dt} \,, \, \overline{\varphi}_{R1} = M_1 \,\bar{i}_{S1} + L_{R1} \,\bar{i}_{R1} \,, \tag{4}$$

$$\overline{v}_{S5} = R_S \,\overline{i}_{S5} + \frac{d\Phi_{S5}}{dt} , \ \overline{\phi}_{S5} = L_{S\ell} \,\overline{i}_{S5} , \qquad (5)$$

$$T = 3p M_1 \overline{i}_{S1} \cdot j \overline{i}_{R1} \quad , \tag{6}$$

where *p* is the pole pairs number, ω_m is the rotor angular speed, and the subscripts *S* and *R* denote stator and rotor quantities, respectively. It should be noted that \bar{i}_{S1} and \bar{i}_{R1} are responsible for the sinusoidal spatial distribution of the magnetic field in the air gap, whereas \bar{i}_{S5} does not contribute to the air gap field.

Field Oriented Control

In dual three-phase induction motor drives, the reference values of the d_1 - q_1 components of the stator currents in a synchronous reference frame, $i_{1d,ref}$ and $i_{1q,ref}$, are determined on the basis of flux and torque commands, respectively [11]. The *d*-axis of synchronous reference frame is aligned with the rotor flux, displaced by angle ϑ with respect to the *d*-axis stationary reference frame. The reference voltages of the two dual three-phase inverters are determined according to the block diagram shown in Fig. 3 [19].



Fig. 3: Block diagram of the regulation scheme with power sharing capabilities for dual three-phase induction motor drives [19].

In the considered system, the power sharing among the four dc sources shows three degrees of freedom. The first one, k_i , concerns the power sharing between the two three-phase windings {1} and {2}. The second and third ones, $k_v^{(1)}$ and $k_v^{(2)}$, are related to the power sharing between the two inverters H and L which supply each three-phase winding. With reference to the block diagram of Fig. 3, individual modulation indexes are defined as

$$m^{(1)} = \frac{\sqrt{3}}{2} \frac{v_{ref}^{(1)}}{V_{dc}} , \qquad m_{H}^{(1)} = \sqrt{3} \frac{v_{H,ref}^{(1)}}{V_{dc}} , \quad m_{L}^{(1)} = \sqrt{3} \frac{v_{L,ref}^{(1)}}{V_{dc}}$$
(7)

$$m^{(2)} = \frac{\sqrt{3}}{2} \frac{v_{ref}^{(2)}}{V_{dc}} , \qquad m_H^{(2)} = \sqrt{3} \frac{v_{H,ref}^{(2)}}{V_{dc}} , \ m_L^{(2)} = \sqrt{3} \frac{v_{L,ref}^{(2)}}{V_{dc}}$$
(8)

being $2/\sqrt{3} V_{dc}$ and $1/\sqrt{3} V_{dc}$ the maximum amplitude of sinusoidal balanced output voltages for dual three-phase inverters and single three-phase inverters, respectively [17]. Introducing in (7) and (8) the definition of voltage ratios $k_v^{(1)}$ and $k_v^{(2)}$, the relationships among

individual modulation indexes can be determined as follows

$$v_{H,ref}^{(1)} = k_v^{(1)} v_{ref}^{(1)} , \quad v_{L,ref}^{(1)} = (1 - k_v^{(1)}) v_{ref}^{(1)} \quad \Rightarrow \quad m_H^{(1)} = 2 m^{(1)} k_v^{(1)} , \quad m_L^{(1)} = 2 m^{(1)} (1 - k_v^{(1)})$$
(9)

$$v_{H,ref}^{(2)} = k_v^{(2)} v_{ref}^{(2)} , \quad v_{L,ref}^{(2)} = (1 - k_v^{(2)}) v_{ref}^{(2)} \rightarrow m_H^{(2)} = 2m^{(2)} k_v^{(2)} , \quad m_L^{(2)} = 2m^{(2)} (1 - k_v^{(2)})$$
(10)

Hardware implementation

The six-phase quad-inverter induction motor drive has been implemented in the Power Electronics Lab of the Dept. of Electrical Engineering, University of Bologna (IT). A picture of the working area is given in Fig. 4. The system consists in two processor boards, including a TMS320F2812 DSP each, as depicted in Fig. 5. The DSP-1 board acts a master unit, performing all the calculations required by the control scheme of Fig. 3, and providing for the firing signals of inverters H1 and L1 by its own internal PWM unit. The DSP-2 board acts a slave unit, receiving the modulating signals from the DSP-1 by the multichannel buffered serial port (McBSP data cable connection). DSP-2 provides for the firing signals of inverters H2 and L2 by its own internal PWM unit.

Two DSP controllers are synchronized with proper communication for transmitting/receiving the signals by setting proper frame period, frame pulse-width of frame synchronization generator, sample rate clock division and transmitter/receiver interrupts of the McBSP protocol unit. In detail, transmitter/receiver is configured in reset at the beginning of initialization, then the McBSP is programmed for desired transmitter/receiver operation. Finally the McBSP transmitter/receiver is taken out of reset after two clock cycle of the sample rate generator clock cycle.



Fig. 4: Overall view of the working area in the Lab. Fig. 5: Top view of the main system boards.

MOSFETs (6 in parallel per switch)	Vishay Siliconix SUM85N15-19
MOSFET ratings	$ \begin{array}{c} V_{DSS} = 150 \ [V]; \ R_{DS} = 19 [m\Omega] \\ \hline @ \ V_{GS} = 10 [V]; \ I_D = 85 [A] \end{array} $
switching frequency	2 [kHz]
dc-bus capacitance (4 banks)	12 [mF]
dc-bus voltage (4 in all)	52 [V]
load impedance (open ends, 6 in all)	6 [Ω]
load power factor (angle)	0.67 (48°)
load rated current	10 [A]

Table I: Main parameters of four inverters and six-phase load

In DSP-1 McBSP transmitter frame is configured with single-phase, 2 words per frame of two 16-bit data for transmitting (modulating signal in stationary reference frame) to DSP-2 and receiver frame is configured with single-phase, 1 words per frame of one 16-bit data for receiving enable reception from DSP-2 slave unit. In DSP-2 McBSP receiver frame is configured with single-phase, 2 words per frame of two 16-bit data for receiving (modulating signal in stationary reference frame) from DSP-1 and transmitter frame is configured with single-phase, 1 words per frame of one 16-bit data for transmitter frame is configured with single-phase, 1 words per frame of one 16-bit data for transmitter frame is configured with single-phase, 1 words per frame of one 16-bit data for transmitting enable reception to DSP-1 master unit.

Rising edge of the transmitter clock pin generates the transmission of the data and falling edge of the receiver clock pin generates the reception of the data in the both master/slave DSP McBSP configuration with transmitting/receiving the data in 2-bit data delay. The McBSP sends a receiver interrupt request to the CPU when each receive frame-synchronization pulse is detected and in reset state as well. Transmitter generates an interrupt request to the CPU when new frame synchronization occurs. In this way both master DSP-1 and slave DSP-2 transmit/receive the data with proper synchronization and hand-shake.

The main parameters of the four 2-level VSIs are given in Table I, together with load parameters. For the sake of simplicity, these first experimental tests are carried out by using a system of six balanced impedances (passive load) instead of the dual three-phase induction motor load. The six-phase motor will be derived from a conventional three-phase induction motor by rearranging the winding connections. Inverters are modulated here without multilevel output voltage optimization, and a phase angle of 30° is set as the displacement between the output voltages of the two dual three-phase inverters.

Experimental Results

A complete set of open-loop experimental results is presented in this section, on the basis of the simulations given in [19], with reference to balanced and unbalanced operating conditions.

In the first experimental test (Figs. 6-8), the behavior of the system is analyzed in balanced conditions with modulation indexes $m^{(1)} = m^{(2)} = 0.75$, corresponding to a current ratio $k_i = 1/2$ (balanced currents), and voltage ratios $k_v^{(1)} = k_v^{(2)} = 0.50$ (balanced voltages). In this operating condition the total power is equally shared among the four VSIs, and individual modulation indexes from (9) and (10) are $m_H^{(1)} = m_L^{(1)} = m_H^{(2)} = 0.75$.

Fig. 6 depicts line-to-line voltages (H and L), artificial phase-to-neutral voltages (H and L), and load phase voltage (calculated) for the two dual three-phase inverters $\{1\}$ and $\{2\}$.

Fig. 7 shows artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual three-phase inverters {1} and {2}.

All the six-phase output currents are shown in Fig. 8. It should be noted that the currents are almost sinusoidal, practically with same amplitude and correct phase angle displacement (load impedances are not perfectly balanced).



Fig. 6: Voltage waveforms of the two dual three-phase inverters {1} and {2} in balanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: line-to-line voltages (H and L), artificial phase-to-neutral voltages (H and L), and load phase voltage (calculated).



Fig. 7: Voltage, current, and filtered waveforms of inverters {1} and {2} in balanced conditions. From top to bottom: artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.



Fig. 8: Six-phase load currents in balanced conditions. Inverter {1}: purple traces (2 measured, 1 calculated). Inverter {2}: turquoise traces (2 measured, 1 calculated).

In the second experimental test (Fig. 9) the behavior of the system is analyzed in unbalanced conditions to verify the power sharing capability between the two inverters H and L of the two dual threephase inverter {1} and {2}. In particular, modulation indexes $m^{(1)} = m^{(2)}$ are set as in the previous case, $m^{(1)} = m^{(2)} = 0.75$, corresponding to a current ratio $k_i = 1/2$ (balanced currents), whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 0.60$ (unbalanced voltages), leading to individual modulation indexes $m_H^{(1)} = m_H^{(2)} =$ 0.90, $m_L^{(1)} = m_L^{(2)} = 0.60$, given by (9) and (10). In this operating condition inverters H supply 50% more power that inverters L.

Fig. 9 shows artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual three-phase inverters $\{1\}$ and $\{2\}$. As expected, fundamental voltage components of individual inverters H and L are one 50% more than the other. However, being load phase voltages the same as in previous case, load currents are the same as well.



Fig. 9: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = m^{(2)} = 0.75$ ($k_i = 1/2$), $k_v^{(1)} = k_v^{(2)} = 0.60$. From top to bottom: artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

In the third and last experimental test (Figs. 10-11) the behavior of the system is analyzed in unbalanced conditions to verify the power sharing capability between the two inverters {1} and {2}. In particular, modulation indexes $m^{(1)}$ and $m^{(2)}$ are set one the double of the other, $m^{(1)} = 0.75$, $m^{(2)} = 0.375$, corresponding to a current ratio $k_i = 2/3$ (unbalanced currents), whereas voltage ratios are $k_v^{(1)} = k_v^{(2)} = 0.50$ (balanced voltages), leading to individual modulation indexes $m_H^{(1)} = m_L^{(1)} = 0.75$, $m_H^{(2)} = m_L^{(2)} = 0.375$, given by (9) and (10). In this operating condition inverter {1} supplies 50% more power that inverter {2}.



Fig. 10: Voltage, current, and filtered waveforms of inverters {1} and {2} in unbalanced conditions, $m^{(1)} = 0.75$, $m^{(2)} = 0.375$ ($k_i = 2/3$), $k_v^{(1)} = k_v^{(2)} = 0.50$. From top to bottom: artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current.

Fig. 10 shows artificial phase-to-neutral voltages (H and L) and their fundamental components, load phase voltage (measured) and current for the two dual three-phase inverters {1} and {2}.

As expected, fundamental voltage components of inverters $\{1\}$ and $\{2\}$ are one the double of the other, providing load currents with the same ratio, corresponding to $k_i = 2/3$.

All the six-phase output currents are shown in Fig. 11. Also in this case, currents are practically sinusoidal, with an almost correct phase angle displacement (even if load impedances are not perfectly balanced). As expected, the currents supplied by inverter {1} have an amplitude double of the currents supplied by inverter {2}.



Fig. 11: Six-phase load currents in unbalanced conditions. Inverter {1}: purple traces (2 measured, 1 calculated). Inverter {2}: turquoise traces (2 measured, 1 calculated).

Conclusion

A preliminary version of a multi-phase multi-level ac motor drive based on a dual three-phase openend windings induction machine has been implemented and analyzed in this paper. The power supply consists of four conventional 2-level three-phase voltage source inverters with insulated dc sources. The whole control scheme was developed using two TMS320F2812 DSP controllers working under McBSP protocol for PWM communication in open-loop analysis, controlling a six-phase load with open-end configuration.

It has been shown that, by an appropriate control strategy, the total motor power can be shared among the four dc sources with three degrees of freedom. In order to regulate the couple of 2-level VSIs supplying each three-phase winding such as a 3-level inverter, a simplified PWM technique has been adopted, allowing the power sharing between the two dc sources. This regulation leads to two degrees of freedom in the total power sharing, one for each dual three-phase inverter. A suitable technique has been adopted in order to regulate the power sharing between the two dual three-phase inverters, leading to an additional degree of freedom in the total power sharing.

Real time test results provided in this paper prove the effectiveness of the proposed six-phase quadinverter system in different operating conditions using two DSP-based controllers. However, these experimental results should be considered only as the preliminary tests in order to prove the effectiveness of the hardware implementation of the multi-phase multi-level induction motor drive. Next step is to introduce the six-phase induction motor instead of the passive load, according to the control scheme presented in [19], and to optimize the output voltage waveforms according to the multilevel control strategy proposed in [17].

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