

# DUAL INVERTER SPACE VECTOR MODULATION WITH POWER BALANCING CAPABILITY

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**Abstract:** Dual two-level inverter topology is a simple structure capable to produce a multilevel voltage output equivalent to a 3-level inverter. Its modular structure consists of two standard two-level three-phase voltage source inverter (VSI) supplied by one or two dc sources. Known modulations cannot provide arbitrary power sharing between inverters in order to balance their dc voltages in case of two separate dc supplies. This paper proposes a new space vector modulation (SVM) technique for a dual two-level inverter which can provide load control of the two dc sources as well as multilevel voltage output. An original modulation algorithm has been introduced to regulate the dc-link voltages of each VSI according with the requirement of a control system, by means of a specialized space vector modulation. The proposed algorithm has been verified by experimental tests.

**Index Terms:** Dual two-level inverter, space vector modulation, power sharing, three-level inverter.

## I. INTRODUCTION

Multilevel inverters are being increasingly used in high-power medium voltage applications due to their advantages compared to two-level inverters, such as lower common-mode voltage, lower  $dv/dt$ , lower harmonics in output voltage and current and reduced voltage on the power switches. Having  $n$ -level leg (e.g. for the multi point clamped inverter) a three-phase multilevel inverter provides

$$p = 2(2n - 1) - 1 = 4n - 3 \quad (1)$$

different phase voltage levels for a star-connected load. Although the principle is very simple, the complexity of both the leg hardware and modulation/control algorithms sharply increases with the number of levels. This drawback lead to application of the dual topology, providing the same number of output voltage levels as  $n$ -level inverter by using two simpler multilevel inverters (with less levels) [1], [2].

The two inverters are connected "in opposition" at two ends of the load in order to obtain output voltage as a difference of inverter's leg potentials as shown in Fig. 1 for two identical two-level three-phase inverters ( $m = 2$ ). They will produce:

$$p = 2(4n - 3) - 1 = 8n - 7 \quad (2)$$

different phase voltage levels of output voltage. Comparing (2) with (1) gives  $m = (n+1)/2$ , which is significant reduction compared to  $n$ . Even for dual two-level inverter (Fig. 1) the saving is significant compared to 3-level, since it means the use of readily available standard two-level inverters. It should be noted that in

general two inverters do not have to be necessary equal [3].

The combination of the eight switching configuration for each three-phase inverter yields total 64 switching states. In the case of  $V_H = V_L = V_{dc}$  these switching states correspond to 19 different output voltage vectors, including zero vector, as represented in Fig. 2. The redundancy of switching states corresponds to a degree of freedom which is useful to develop different modulation strategies, as discussed in Section III. In particular, the output voltage waveform of the converter has up to nine output levels of phase voltage. It represents a viable solution when the three-phase output can be connected in the open-winding configuration, as for transformers and ac motors, and especially when the dc source can be easily split in two insulated supplies, as for batteries and PV panels. Note that the presence of two insulated dc sources prevents the circulation of zero-sequence currents, avoiding the use of an additional homopolar reactor or the application of a modified voltage modulation algorithm which doesn't produce zero-sequence voltage but leads to lower dc bus voltage utilization [4].

Being the converter supplied by two distinct sources, in several applications it is necessary to regulate the power flow from the two sources. This requirement can be demanded in order to equalize the state of charge of two banks of batteries, or to exploit the different characteristic of two sources, e.g., generators and batteries. A possible approach to achieve the power sharing control is to define the decomposition of the total reference into two collinear vectors [5]:

$$\begin{cases} \vec{v}_H^* = k \vec{v}^* \\ \vec{v}_L^* = (1 - k) \vec{v}^* \end{cases} \quad (3)$$

as shown in Fig. 3(a). It also provides optimum inverter utilization since the output voltage is maximal [6]. In general, unequal treatment of the two inverters is often useful approach, e.g. in case of completely different sources [7], or in case of a failure [8], making system more fault-tolerant.

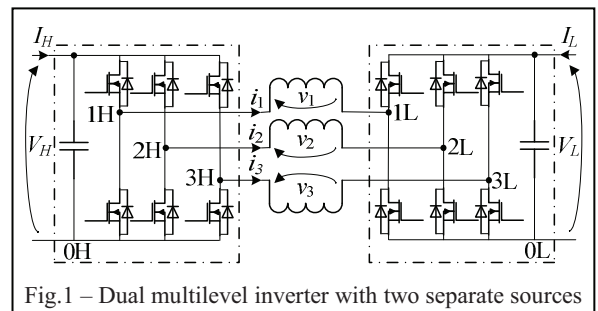


Fig.1 – Dual multilevel inverter with two separate sources

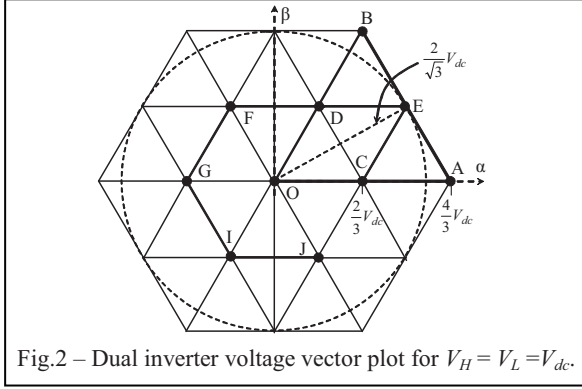


Fig.2 – Dual inverter voltage vector plot for  $V_H = V_L = V_{dc}$ .

Known modulations for dual inverter presume ideally symmetrical sources and consequently provide a symmetrical power sharing between them. A SVM method to overcome these problems has been presented in [9]. However, it leads to switching sequences difficult to implement on the PWM generation unit of a standard (digital signal processor) DSP. In this paper a new modulation technique is presented, which is able both to perform multilevel operation and to regulate the load power sharing between the two dc sources within each switching period. The proposed modulation provides a simple implementation on a standard PWM generation unit of a DSP.

## II. DUAL THREE-PHASE INVERTER MODULATION

With reference to the scheme of Fig.1, using space vector representation, the output voltage vector  $\bar{v}$  of the multilevel converter is given by the contribution of the voltage vectors  $\bar{v}_H$  and  $\bar{v}_L$ , generated by inverter H and L respectively,

$$\bar{v} = \bar{v}_H + \bar{v}_L, \quad (4)$$

$$\bar{v}_H = \frac{2}{3} V_H (S_{1H} + S_{2H} e^{j2\pi/3} + S_{3H} e^{j4\pi/3}),$$

$$\bar{v}_L = -\frac{2}{3} V_L (S_{1L} + S_{2L} e^{j2\pi/3} + S_{3L} e^{j4\pi/3}), \quad (5)$$

where  $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$  are the switch states of the inverter legs.

Load voltages can be expressed analogously as for single three-phase inverter [10]:

$$v_1 = \frac{2(S_{1H} - S_{1L}) - (S_{2H} - S_{2L}) - (S_{3H} - S_{3L})}{3},$$

$$v_2 = \frac{-(S_{1H} - S_{1L}) + 2(S_{2H} - S_{2L}) - (S_{3H} - S_{3L})}{3}, \quad (6)$$

$$v_3 = \frac{-(S_{1H} - S_{1L}) - (S_{2H} - S_{2L}) + 2(S_{3H} - S_{3L})}{3}$$

In what follows SVM approach will be used as a insightful method for the analysis. Due to the hexagon symmetry (Fig.2), the analysis can be restricted to the one of the six big sectors (i.e., OAB in Fig. 2), similarly to the case of standard three-phase SVM algo-

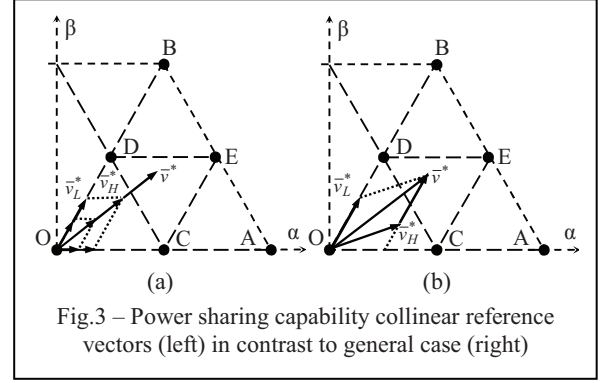


Fig.3 – Power sharing capability collinear reference vectors (left) in contrast to general case (right)

rithm. Furthermore, the big triangle OAB is divided in four identical equilateral triangles denoted OCD (inner), CDE (intermediate), ACE and BDE (outers), as shown in Fig. 3. The voltage reference vector  $\bar{v}^*$  lays in one of these triangles, leading to the four homonymous cases. Using space vector modulation principle (Fig. 4), references  $\bar{v}_H^*$  and  $\bar{v}_L^*$  can be generated by selecting adjacent vectors  $\bar{v}_{aH}$ ,  $\bar{v}_{bH}$ ,  $\bar{v}_{oH}$  and  $\bar{v}_{aL}$ ,  $\bar{v}_{bL}$ ,  $\bar{v}_{oL}$ , respectively.

The switch configurations corresponding to selected vectors cannot be applied in an arbitrary sequence if proper multilevel voltage waveform is desired, i.e., the reference voltage  $\bar{v}^*$  should be generated by using the nearest three vectors approach (NTV) [11]. Furthermore, the PWM generation unit of the DSP allows up to two commutations for each inverters leg.

### A. Independent modulation

Rewriting (6) as:

$$v_1 = \frac{2v_{AN} - v_{BN} - v_{CN}}{3} - \frac{2v_{DM} - v_{EM} - v_{FM}}{3}$$

$$v_2 = \frac{-v_{AN} + 2v_{BN} - v_{CN}}{3} - \frac{-v_{DM} + 2v_{EM} - v_{FM}}{3} \quad (7)$$

$$v_3 = \frac{-v_{AN} - v_{BN} + 2v_{CN}}{3} - \frac{-v_{DM} - v_{EM} + 2v_{FM}}{3}$$

yields that output voltage of a dual inverter can be obtained as difference of phase-to-neutral voltages produced by two three-phase inverters separately. Here the two inverters can be modulated by any of

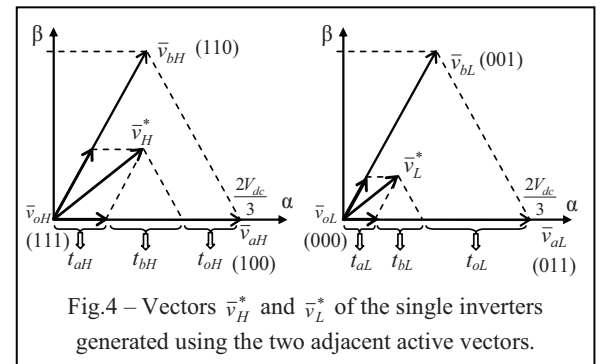


Fig.4 – Vectors  $\bar{v}_H^*$  and  $\bar{v}_L^*$  of the single inverters generated using the two adjacent active vectors.

known modulation techniques, e.g. popular SVM with equal zero vector placement or a carrier-based (CB) equivalent. The voltage references can be given independently regarding both amplitude and phase (within available dc voltage limits). This approach has been proposed for automotive applications [6], [7]. Benefits of the method are simple modulation and direct power sharing capability. The disadvantage is improper multilevel waveform depicted in Fig. 5, showing large voltage excursion from maximal to minimal voltage levels.

### B. Sine-Sawtooth modulation

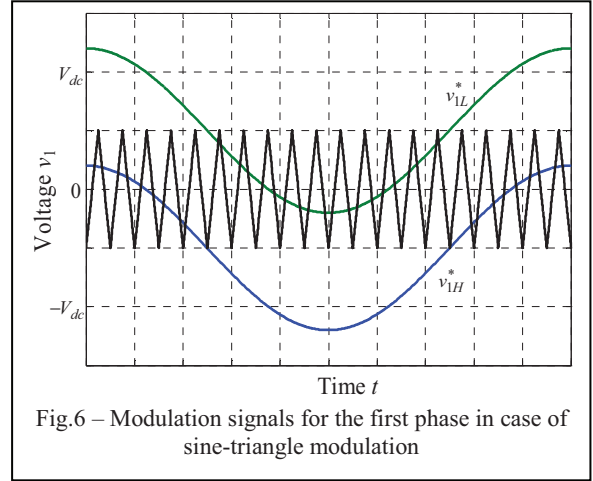
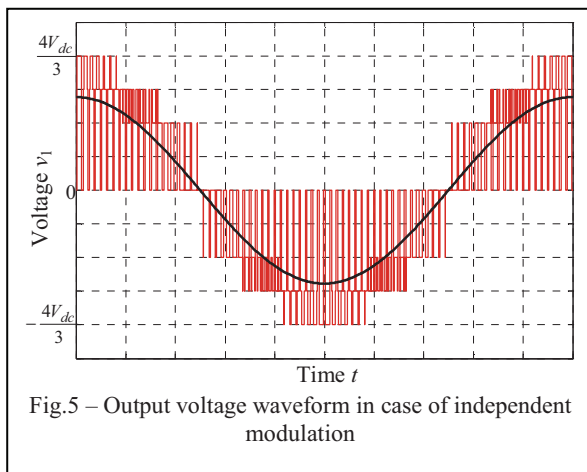
Historically, this was the first proposed CB modulation [2]. Based on (6), it uses the same reference for the inverter L but applying opposite modulation logic. Due to the sawtooth carrier all three legs of each inverter commute simultaneously at the end of the switching period, which is unacceptable and therefore will not be considered further.

### C. Sine-Triangle modulation

Another CB algorithm is a sine-triangle modulation adopted from the “phase opposition disposition” approach used for traditional 3-level inverters [11], which can be easily extended to dual inverter configuration. Using (6), the simplest multilevel modulation would be discontinuous modulation treating separately three pairs of legs. For positive values of  $v_1^*$  the reference for the single inverters H and L are  $v_{1H}^* = v_1^*$  and  $v_{1L}^* = 0$ , respectively, whereas for negative values it will be the opposite:  $v_{1H}^* = 0$  and  $v_{1L}^* = -v_1^*$ . The modulation can be achieved by using common triangular carrier and references

$$\begin{aligned} v_{1H}^* &= mV_{dc} \cos \theta^f - V_{dc} / 2 \\ v_{1L}^* &= mV_{dc} \cos(\theta^f - \pi) - V_{dc} / 2 \end{aligned} \quad (8)$$

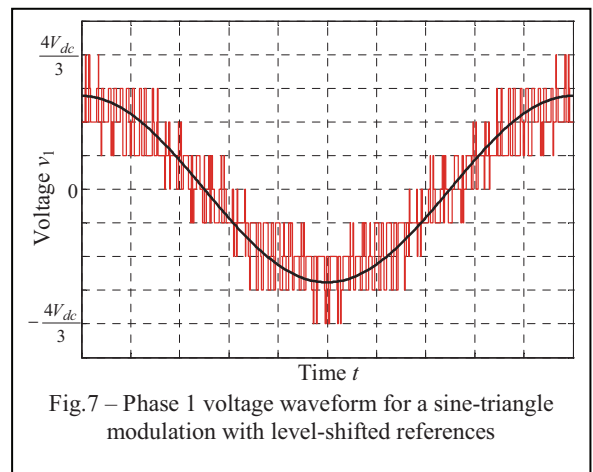
as illustrated in Fig.6, taking in account that for the in-



verter L modulation logic has to be opposite to provide corresponding negative values. The resulting proper multilevel output voltage is depicted in Fig. 7. The switching pattern during one switching period for  $\bar{v}^*$  inside OCD triangle has been illustrated in Fig. 8. Note that one of the inverter H applies all three NTVs ( $\bar{v}_{aH}$ ,  $\bar{v}_{bH}$ ,  $\bar{v}_{oH}$ ), while the other uses just two of them ( $\bar{v}_{bL}$ ,  $\bar{v}_{oL}$ ). Yields that period-averaged vectors  $\bar{v}_H$  and  $\bar{v}_L$  cannot be collinear, a case illustrated in Fig. 3(b). In Sect. III will be shown that the omission of the one of the active vector is actually stipulated by the demand of proper multilevel waveform.

### D. Discrete SVM

In order to treat dual inverter with well-known single inverter modulation the application of only one vector for one of the inverters during the switching period have been proposed in [12]. The remaining part of the total reference is provided by the other inverter using standard SVM. Then in the following switching period the roles of the inverters are interchanged to achieve symmetrical loading. The period-averaged vectors  $\bar{v}_H^*$  and  $\bar{v}_L^*$  produced by inverters H and L are not collinear, which makes the modulation inapplicable for applications demanding power sharing control.



### E. SVM with power sharing capability

A SVM method providing power sharing has been presented in [5], [9]. However, it leads to switching sequences difficult to implement on the standard PWM generation unit of a DSP, possessing a unique carrier for all three phases. For this reason, a modified SVM algorithm, more suitable to be implemented on standard DSP is presented in the following section.

### III. PROPOSED MODULATION

Having the inverter reference voltages  $\bar{v}_H^*$  and  $\bar{v}_L^*$  determined by the control system, the modulation algorithm must ensure their application to the load.

#### A. Calculation of the vector application times

Referred to Figs. 3 and 4, the application times of active vectors can be calculated as:

$$\begin{cases} t_{aH} = \frac{3v_{\alpha H} - \sqrt{3}v_{\beta H}}{2V_{dc}} T_S, t_{aL} = \frac{3v_{\alpha L} - \sqrt{3}v_{\beta L}}{2V_{dc}} T_S \\ t_{bH} = \frac{\sqrt{3}v_{\beta H}}{V_{dc}} T_S, t_{bL} = \frac{\sqrt{3}v_{\beta L}}{V_{dc}} T_S \end{cases} \quad (9)$$

being  $\bar{v}_H^* = v_{\alpha H}^* + jv_{\beta H}^*$ ,  $\bar{v}_L^* = v_{\alpha L}^* + jv_{\beta L}^*$ , and  $T_S$  the switching period. The remaining application times of null vectors are:

$$\begin{aligned} t_{oH} &= T_S - t_{aH} - t_{bH}, \\ t_{oL} &= T_S - t_{aL} - t_{bL}. \end{aligned} \quad (10)$$

#### B. Determination of the switching sequence

As stated before, in order to determine the switching sequence, the four relevant cases will be examined.

*Triangle OCD:* For the inner triangle the NTV are  $\bar{v}_O$ ,  $\bar{v}_C$ , and  $\bar{v}_D$  which can be obtained by the following combinations of voltage vectors selected for the two inverters:  $(\bar{v}_{oH}, \bar{v}_{oL})$ ,  $(\bar{v}_{aH}, \bar{v}_{oL})$  and  $(\bar{v}_{oH}, \bar{v}_{aL})$ ,  $(\bar{v}_{bH}, \bar{v}_{oL})$  and  $(\bar{v}_{oH}, \bar{v}_{bL})$ , respectively. By using these combinations, since  $\bar{v}^* = \bar{v}_H^* + \bar{v}_L^*$  is inside the inner triangle, for any value of  $\bar{v}_H^*$  and  $\bar{v}_L^*$  the total application time of active vectors is (Fig. 3)

$$t_{aH} + t_{bH} + t_{aL} + t_{bL} \leq T_S. \quad (11)$$

By combining (11) with (10) yields

$$t_{oH} + t_{oL} \geq T_S. \quad (12)$$

Note that (12) provides a criterion for the identification of the inner triangle OCD. The voltage vector combinations can be arranged within the switching

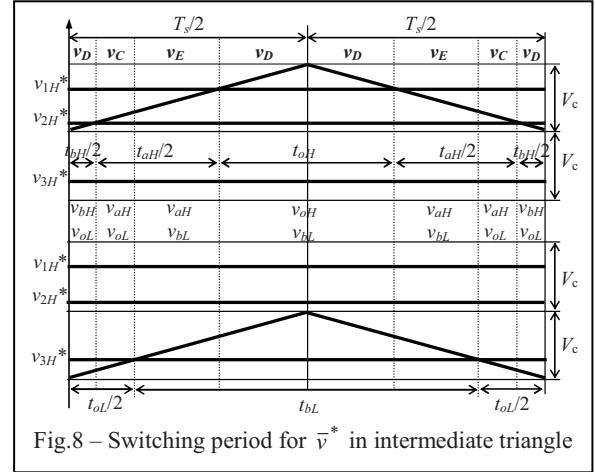


Fig.8 – Switching period for  $\bar{v}^*$  in intermediate triangle

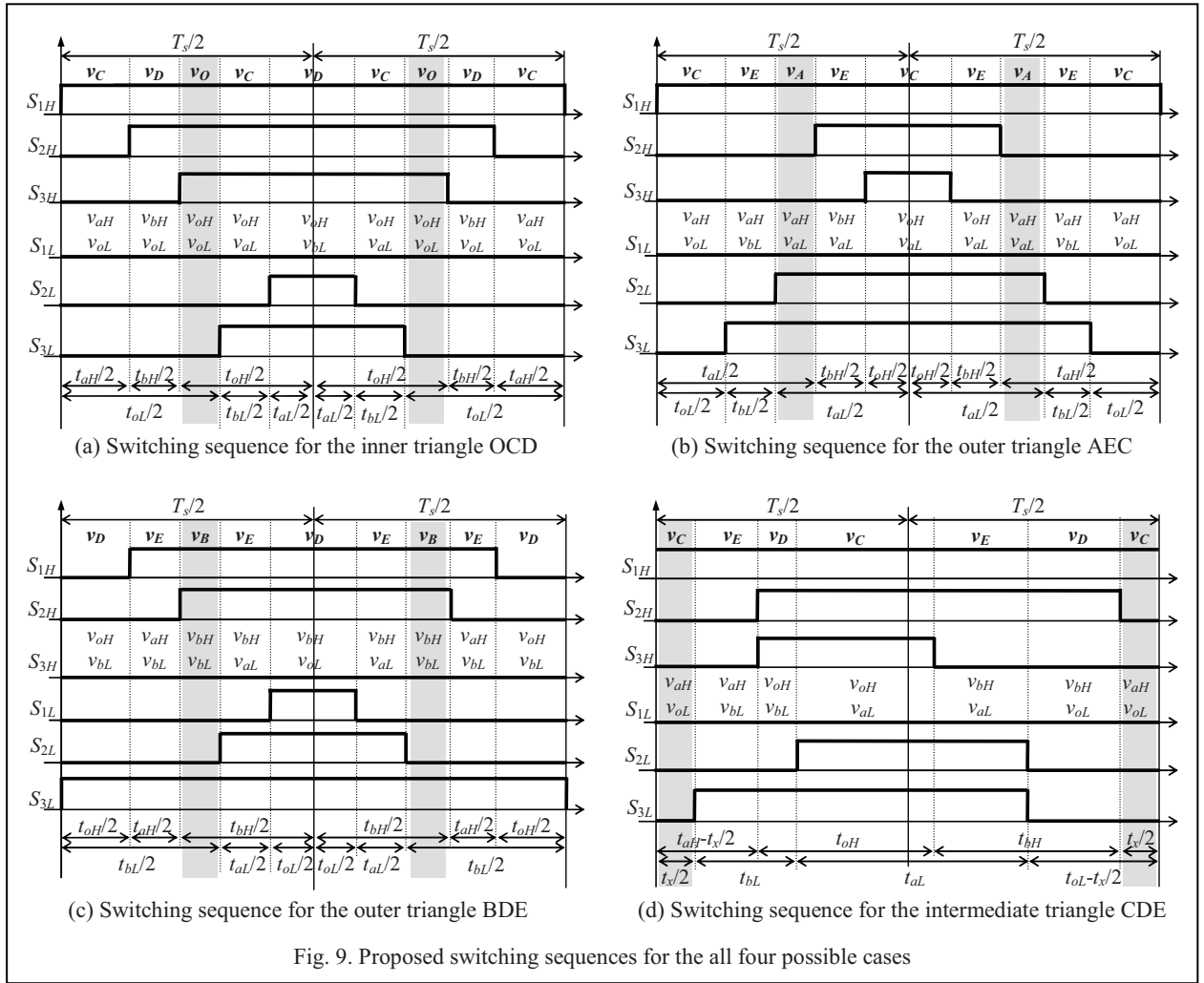
period to obtain a switching sequence suitable for the implementation in PWM generation unit of a standard DSP, as represented in Fig. 9(a). In the diagram is emphasized the overlap between the two null vectors ( $\bar{v}_{oH}$  and  $\bar{v}_{oL}$ ), provided by (12), which allows the generation of  $\bar{v}^*$  only by vectors  $\bar{v}_O$ ,  $\bar{v}_C$ , and  $\bar{v}_D$ . The proposed switching sequence belongs to symmetrical and discontinuous modulation, minimizing the number of commutations. A continuous modulation can be easily obtained by introducing the null vector  $\bar{v}_O$  in the middle and at the ends of the switching period.

*Triangle AEC:* For the first outer triangle the NTV are  $\bar{v}_A$ ,  $\bar{v}_C$ , and  $\bar{v}_E$ , which can be composed by the combinations:  $(\bar{v}_{aH}, \bar{v}_{oL})$  and  $(\bar{v}_{oH}, \bar{v}_{aL})$ ,  $(\bar{v}_{aH}, \bar{v}_{aL})$  and  $(\bar{v}_{aH}, \bar{v}_{bL})$ ,  $(\bar{v}_{bH}, \bar{v}_{aL})$ , respectively. Since  $\bar{v}^*$  lies inside the triangle ACE its component along  $\bar{v}_{aH}$  is bigger than  $|\bar{v}_{aH}|$  (Fig. 3). Similarly to the previous case, this consideration leads to

$$t_{aH} + t_{aL} \geq T_S \quad (13)$$

Equation (13) provides a criterion for the identification of the outer triangle ACE. Also in this case, the voltage vector combinations can be arranged within the switching period to obtain a switching sequence suitable for the implementation in PWM generation unit of a standard DSP, as represented in Fig. 9(b). In the figure is emphasized the overlap between the two active vectors ( $\bar{v}_{aH}$  and  $\bar{v}_{aL}$ ), provided by (14), which allows the generation of  $\bar{v}^*$  only by vectors  $\bar{v}_A$ ,  $\bar{v}_C$  and  $\bar{v}_E$ . Note that, as in the previous case of the inner triangle, the proposed sequence leads to symmetrical and discontinuous modulation.

*Triangle BDE:* For the second outer triangle the NTV are  $\bar{v}_B$ ,  $\bar{v}_D$ , and  $\bar{v}_E$ . Due to the symmetry of outer triangles ACE and BDE, this case can be treated as the previous one, involving vectors  $\bar{v}_{bH}$  and  $\bar{v}_{bL}$  in-



stead of  $\bar{v}_{aH}$  and  $\bar{v}_{aL}$ , respectively, leading to

$$t_{bH} + t_{bL} \geq T_S. \quad (14)$$

Similarly, (14) provides a criterion for the identification. The proposed switching sequence is shown in Fig. 9(c).

*Triangle CDE:* For the intermediate triangle the NTV are  $\bar{v}_C$ ,  $\bar{v}_D$ , and  $\bar{v}_E$ , which can be generated by the combinations:  $(\bar{v}_{aH}, \bar{v}_{oL})$  and  $(\bar{v}_{oH}, \bar{v}_{aL})$ ,  $(\bar{v}_{bH}, \bar{v}_{oL})$  and  $(\bar{v}_{oH}, \bar{v}_{bL})$ , and  $(\bar{v}_{aH}, \bar{v}_{bL})$  and  $(\bar{v}_{bH}, \bar{v}_{aL})$ , respectively. The following three conditions define the triangle CDE:

$$t_{oH} + t_{oL} \leq T_S \quad (\text{outside OCD}), \quad (15)$$

$$t_{aH} + t_{aL} \leq T_S \quad (\text{outside ACE}), \quad (16)$$

$$t_{bH} + t_{bL} \leq T_S \quad (\text{outside BDE}). \quad (17)$$

The presence of three simultaneous conditions (15)-(17) makes this case the most complex among the four considered cases.

The proposed switching sequence, suitable for the implementation on a standard DSP is shown in Fig. 9(d). The parameter  $t_x$  (denoted with grey) stands for a

degree of freedom which determines the relative position of the switching sequence of the one inverter with respect to the other. I.e., one of the sequences can be translated by the time interval  $t_x$ . A similar degree of freedom is present also in the previous three cases (grey intervals in Fig. 9(a)-9(c)). Since application times are given by (9)-(10), the remaining step is to choose the value for interval  $t_x$ , which completely determines the requirements for the DSP implementation. In particular, for the existence of all the vector combinations shown in Fig. 9(d),  $t_x$  has to satisfy the following constraints:

$$\begin{cases} t_x \geq 0 & (18) \end{cases}$$

$$\begin{cases} t_x \geq t_{aH} - t_{bL} & (19) \end{cases}$$

$$\begin{cases} t_x \geq t_{oL} - t_{bH} & (20) \end{cases}$$

$$\begin{cases} t_x \leq t_{aH} & (21) \end{cases}$$

$$\begin{cases} t_x \leq T_S - t_{bH} - t_{bL} & (22) \end{cases}$$

$$\begin{cases} t_x \leq t_{oL} & (23) \end{cases}$$

A detailed derivation of inequalities (18)-(23) is presented in the Appendix, together with the proof that a solution always exists.

The drawback of the proposed sequence is a si-

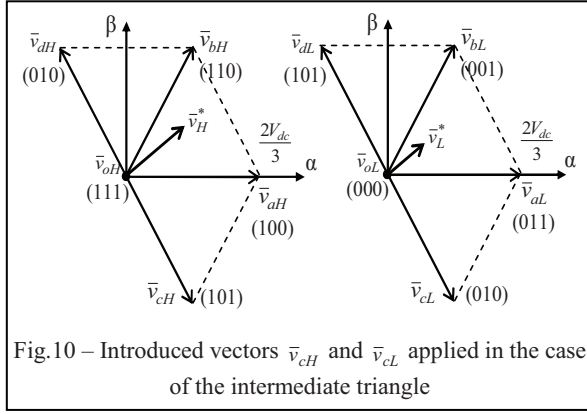


Fig. 10 – Introduced vectors  $\bar{v}_{cH}$  and  $\bar{v}_{cL}$  applied in the case of the intermediate triangle

multaneous commutation of two legs for both inverters H and L. It is possible to overcome this disadvantage by introducing the additional vectors  $\bar{v}_{cH}, \bar{v}_{cL} / \bar{v}_{dH}, \bar{v}_{dL}$  (depicted in Fig. 10) in the space vector decomposition (Fig. 4). Which of the two pairs will be included in switching sequence depends on the position of  $\bar{v}^*$  in respect to OE (Fig. 2). If the reference is in the "lower" subtriangle (closer to A)  $\bar{v}_{cH}$  and  $\bar{v}_{cL}$  are applied, otherwise  $\bar{v}_{dH}$  and  $\bar{v}_{dL}$ . In following the first pair will be examined in details, and the analysis can be repeated in a similar manner for the second.

The application time  $t_c$  of the new vector is introduced at the expense of  $t_{oH}$  and  $t_{oL}$ , and it present a degree of freedom. It adds two new vector combinations ( $\bar{v}_{cH}, \bar{v}_{bL}$ ) and ( $\bar{v}_{bH}, \bar{v}_{cL}$ ) equivalent to already present ( $\bar{v}_{aH}, \bar{v}_{oL}$ ) and ( $\bar{v}_{oH}, \bar{v}_{aL}$ ), as can be seen in Fig. 10. From equation

$$\begin{aligned}\bar{v}_{cH} &= \bar{v}_{aH} - \bar{v}_{bH}, \\ \bar{v}_{cL} &= \bar{v}_{aL} - \bar{v}_{bL}.\end{aligned}\quad (24)$$

yields that  $t_{bH}$  and  $t_{bL}$  should be increased for an amount of  $t_c$ , whereas  $t_{aH}$  and  $t_{aL}$ , should be decreased:

$$\begin{cases} t'_{bH} = t_{bH} + t_c, t'_{bL} = t_{bL} + t_c \\ t'_{aH} = t_{aH} - t_c, t'_{aL} = t_{aL} - t_c \\ t'_{oH} = t_{oH} - t, t'_{oL} = t_{oL} - t_c \end{cases}\quad (25)$$

where the corresponding application times of the vectors  $\bar{v}_{aH}, \bar{v}_{bH}, \bar{v}_{oH}$  and  $\bar{v}_{aL}, \bar{v}_{bL}, \bar{v}_{oL}$  are now denoted as  $t'_{aH}, t'_{bH}, t'_{oH}$ , and  $t'_{aL}, t'_{bL}, t'_{oL}$ , respectively. From (25) arises:

$$t_c \leq \min\{t_{aH}, t_{aL}, t_{oH}, t_{oL}\}\quad (26)$$

The proposed asymmetrical switching sequence is shown in Fig. 11, with all time intervals calculated in Appendix. Similarly as for the previously proposed switching sequence the parameter  $k_{oH}$  stands for a degree of freedom which determines the relative position of the one inverter switching sequence to the other, i.e., one of the sequences can be translated

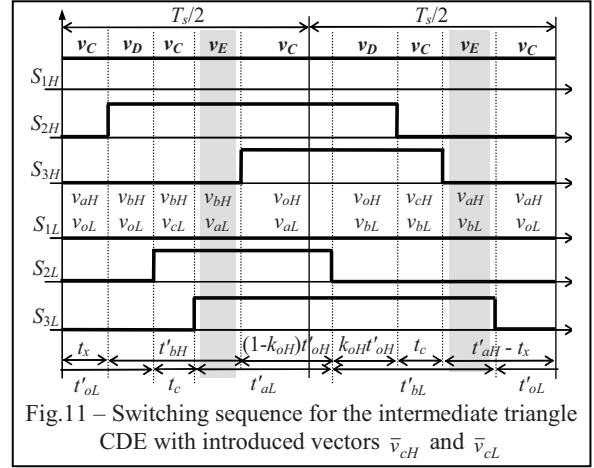


Fig. 11 – Switching sequence for the intermediate triangle CDE with introduced vectors  $\bar{v}_{cH}$  and  $\bar{v}_{cL}$

regarding the other for the time interval  $k_{oH}t_{oH}$ . Applying similar analysis as in previous case yields condition:

$$t_{bL} \leq k_{oH}t'_{oH} \leq t_{oH} - t_{aL}\quad (27)$$

A detailed derivation of (27) is presented in the Appendix, together with the proof that a solution exists.

The proposed switching sequence is discontinuous, as in previous cases, but it does not contain a simultaneous commutation of two legs as in previous case. Despite of the asymmetric distribution of pulses within the switching period, the proposed modulation can be implemented on the PWM generation unit of a standard DSP, as proved by the experimental tests.

#### IV. EXPERIMENTAL RESULTS

The proposed modulation is implemented in TMS320F2812 DSP, equipped with two separate three-phase PWM units and a 150 MHz timer. Then, the DSP is capable to modulate two inverters. The experimental setup is shown in Fig. 12.

The experiment has been done for modulation index  $m = 0.75$  and for both symmetrical ( $k = 0.5$ ) and asymmetrical ( $k = 0.65$ ) inverter's power sharing, with results presented in Fig. 13. Each PWM waveform is shown together with its fundamental component obtained by the low-pass filter. Figures 13(a) and 13(c) show individual phase voltages for each in-

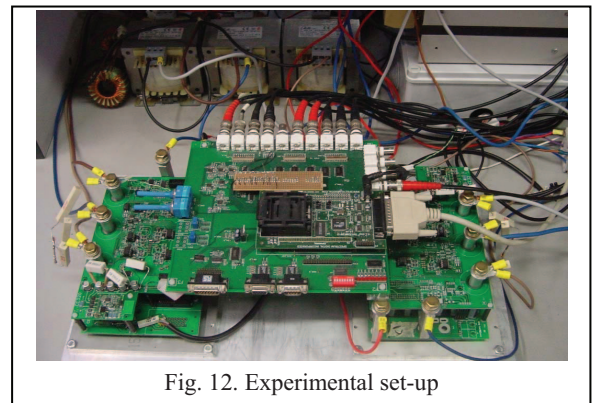


Fig. 12. Experimental set-up

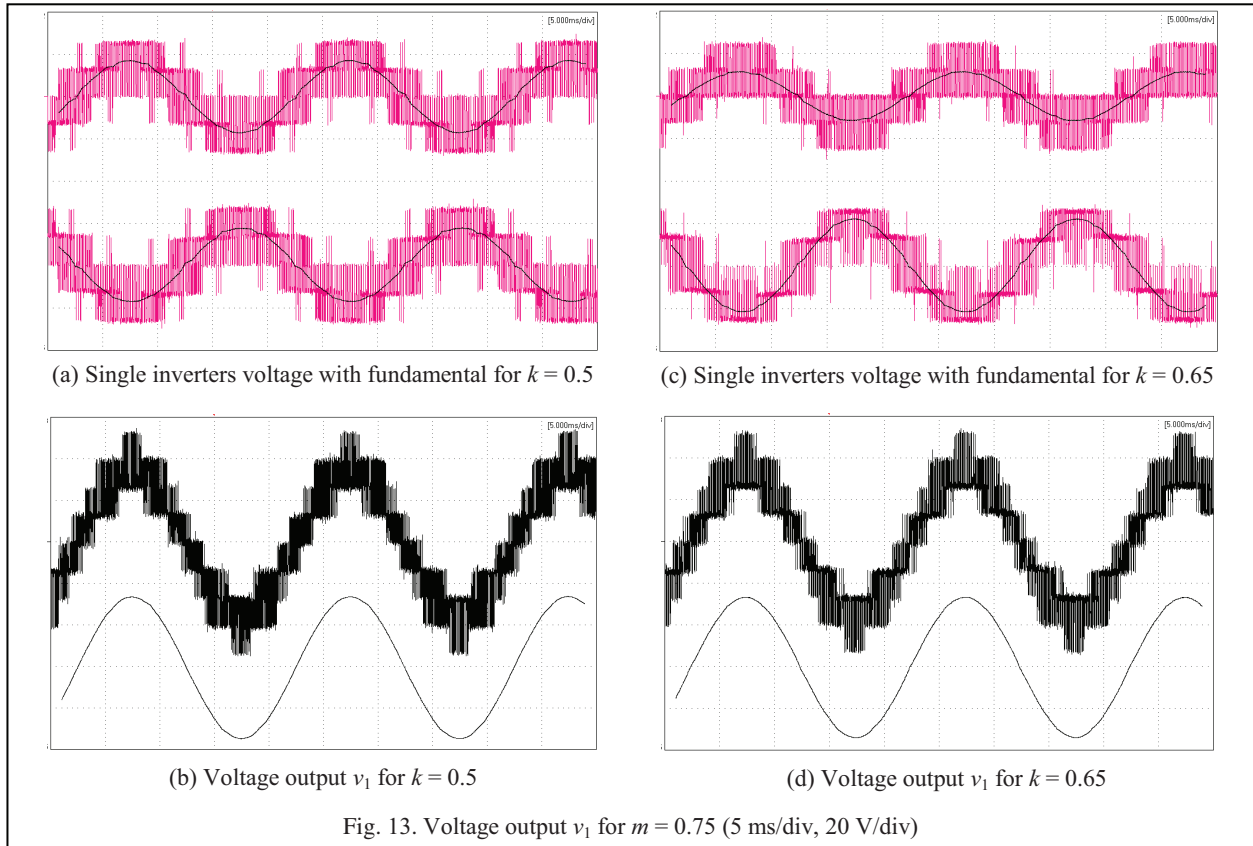


Fig. 13. Voltage output  $v_1$  for  $m = 0.75$  (5 ms/div, 20 V/div)

verter. It can be noticed that voltages are in phase opposition in order to achieve maximum voltage utilization, as specified by (3) and (4). Figures 13(b) and 13(d) show corresponding total output voltages containing maximum nine output voltage levels, followed by its fundamental component. Note that in two cases both output voltages provide equal fundamental component, only individual inverters provide different voltage share.

## V. CONCLUSION

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding a three-phase load with open-end windings has been analyzed in this paper. The dc supplies insulation allows full dc bus utilization and avoids common mode currents without the need of a common mode reactor. The paper has been focused on the development of a modulation strategy able to regulate the power sharing between the dc sources and on the determination of a correct switching sequence for the two inverters. It has been shown that an unbalanced power sharing between the two inverters is possible.

A switching sequence has been proposed which ensures the correct multilevel operation and the possibility to limit the number of simultaneous commutations to one. The experimental tests confirm the effectiveness of the proposed modulation strategy.

## APPENDIX

### INEQUALITIES FOR INTERMEDIATE TRIANGLE

The following inequalities need to be satisfied in order to prove the existence of time intervals for all vector combinations shown in Fig. 9(d). Starting from left-side of switching period inequalities are:

- $(\bar{v}_{aH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_C$  :

$$t_x / 2 \geq 0, \quad (A1)$$

leading to (18);

- $(\bar{v}_{aH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_E$  :

$$(t_{aH} - t_x / 2) - t_x / 2 \geq 0 \quad (A2)$$

leading to (21);

- $(\bar{v}_{oH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_D$  :

$$(t_x / 2 + t_{bL}) - (t_{aH} - t_x / 2) \geq 0 \quad (A3)$$

leading to (19);

- $(\bar{v}_{oH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_C$  :

$$(t_{aH} - t_x / 2 + t_{oH}) - (t_{bL} + t_x / 2) \geq 0 \quad (A4)$$

leading to (22) by introducing (13);

- $(\bar{v}_{bH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_E$  :

$$(t_{bH} + t_x / 2) - (t_{oL} - t_x / 2) \geq 0 \quad (A5)$$

leading to (20);

- $(\bar{v}_{bH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_E$ :

$$(t_{oL} - t_x / 2) - t_x / 2 \geq 0 \quad (A6)$$

leading to (23).

On the basis of (18)-(23), the solution for  $t_x$  exists if the following condition is satisfied

$$\max\{0, t_{aH} - t_{bL}, t_{oL} - t_{bH}\} \leq \min\{t_{aH}, T_s - t_{bH} - t_{bL}, t_{oL}\} \quad (A7)$$

Inequality (A7) can be proved by verifying, one by one, the nine possible combinations of (18)-(20) and (21)-(23). For this purpose, (11) and (16)-(18) must be applied. As an example, for pair (20) and (21) is

$$t_{oL} - t_{bH} \leq t_{aH} \quad (A8)$$

By introducing (11) in (A8) yields

$$t_{oL} \leq T_s - t_{oH} \quad (A9)$$

which is proved by (165). A similar procedure can be used for the remaining combinations.

The following inequalities need to be satisfied in order to prove the existence of time intervals for two "critical" vector combinations shown in Fig. 11. (denoted with grey)

- $(\bar{v}_{bH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_E$ :

$$t'_{aL} - ((1 - k_{oH})t_{oH} + t_c) \geq 0, \quad (A10)$$

- $(\bar{v}_{aH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_E$ :

$$t'_{bL} - (k_{oH}t_{oH} + t_c) \geq 0, \quad (A11)$$

together leading to (27);

The solution for  $k_{oH}$  exists if the condition from (27) is satisfied

$$t_{oH} - t_{aL} \leq t_{bL} \quad (A12)$$

By introducing (12) in (A8) yields

$$t_{oL} \leq T_s - t_{oH} \quad (A13)$$

which is proved by (15).

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