# Multilevel Operation of a Dual Two-Level Inverter with Power Balancing Capability

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***Abstract*—A multilevel converter topology feeding three-phase open-end winding loads is considered in this paper. The scheme is based on two insulated dc supplies, each one feeding a standard two-level, three-phase inverter. A three-phase six-wire load is connected across the output terminals. A new modulation technique able to regulate the sharing of the output power between the two dc sources within each switching cycle is presented. The performance of the whole system has been verified by numerical simulations and experimental tests.**

*Index Terms*—Multilevel converter, dual two-level inverter, space vector modulation strategy, power sharing, voltage source inverter.

## I. Introduction

There are at least two applications in transport where the capability to supplying an electric motor by using two separate sources could be of a great interest in a near future. The first one concerns battery powered electric vehicles. The second one is related to hybrid thermal-electric powertrains which are under development for both vehicle traction and ship propulsion.

The battery powered electric vehicles such as electric fork lift trucks and industrial trucks in the power rating lower than 20kW represents more than 50% of the market and are frequently preferred to thermal engine vehicles for the undeniable economical and environmental advantages inherent in the electric traction.

In modern battery powered industrial electric vehicles the standard solution for the traction system is given by a two-level inverter feeding a three phase induction motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V) for safety reason. With this solution, it is quite difficult to realize an ac drive for a power rating higher than 20 kW, due to the high cost of the resulting high-current semiconductor power switches of the inverter. This problem limits the expansion of ac/drive and consequently the penetration of electric vehicles on this market.

Several solutions have been proposed in order to reduce the current rating of the power switches. The six-phase machine supplied by a six-phase inverter [1]-[4] allows to size the power switches at half the rated current of an equivalent three-phase scheme, but requires the realization of a six-phase machine. The multi-phase drive solution with 7 or more phases further reduces the power sizing of the converter legs, increase the reliability of the drive, but requires special machine design and complex control hardware [5].

An interesting solution is given by the use of a multilevel inverter, which can be realized with semiconductor devices having a voltage rating that is lower than the voltage applied to the motor. Several topologies of multilevel converters have been presented for low voltage applications [6]-[8]. Among these, the cascaded converter configuration called 'dual two-level inverter' can be conveniently used with a battery supply, due to the simplicity to obtain two electrically separated dc sources [9],[10]. The scheme of this multilevel converter applied to a battery supply system is given in Fig. 1. An important feature of the dual two-level inverter that will be presented

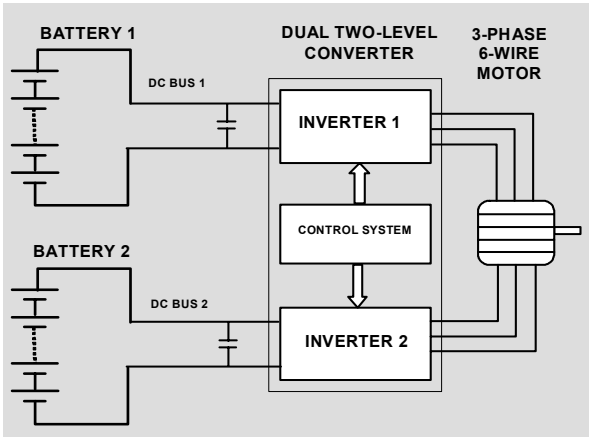



Fig. 1. Basic scheme of the battery powered electric system.

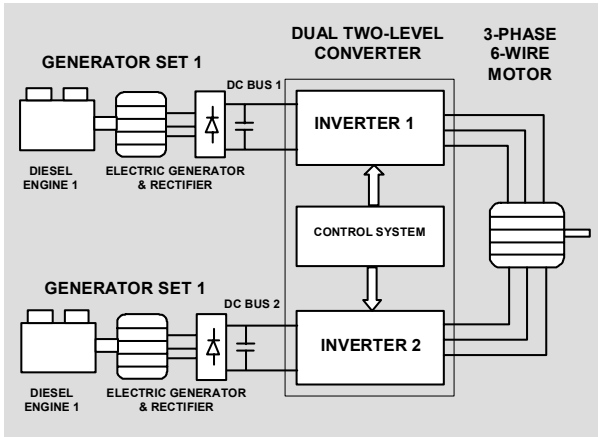



Fig. 2. Basic scheme of the diesel-electric propulsion system.

in this paper is the capability to regulate the power sharing between the two sources yielding to an optimal control of the charge level of the two battery packs.

The second application regards hybrid powertrains. Nowadays, hybrid power trains in series configuration are developed for the thermal-electric traction system of heavy vehicles (industrial vehicles, trains, buses, etc..) and for the thermal - electric propulsion system of ships.

An attractive solution for hybrid powertrains could be realized by using the dual two-level inverter as it is represented in Fig. 2. This scheme is based on the use of two diesel-generator units supplying the two inputs of the dual two-level inverter connected to the motor. In this system, the two generating units are controlled in order to operate always with the best efficiency with respect to the power demanded by the electric motor connected to the vehicle wheels or to the ship screw. This is made possible by using the dual two-level inverter controlled with the proposed modulating strategy, because it allows to regulate the power sharing between the two sources. A very interesting characteristic of this system is the capability to operate at high efficiency in the low power range (less than 50%). In fact, the multilevel converter can be supplied from only one side, keeping off one diesel engine. This working condition yields to a reduced fuel consumption.

## II. MULTILEVEL MODULATION STRATEGY

With reference to the scheme of Fig. 3, using space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter *H* and inverter *L*, respectively:

$$\bar{v} = \bar{v}_H + \bar{v}_L \ . \tag{1}$$

The voltages $\bar{v}_H$ and $\bar{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to:

$$\bar{v}_H = \frac{2}{3} E \left( S_{1H} + S_{2H}\, e^{j\frac{2}{3}\pi} + S_{3H}\, e^{j\frac{4}{3}\pi} \right), \text{ and}$$

$$\bar{v}_L = -\frac{2}{3} E \left( S_{1L} + S_{2L}\, e^{j\frac{2}{3}\pi} + S_{3L}\, e^{j\frac{4}{3}\pi} \right), \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs.

The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 4. By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 *E*. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2/\sqrt{3}\ E$ (i.e., the radius of the inscribed circle).

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 5 (a), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted).

In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\bar{v}$ is synthesized by using the vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, as represented in Fig. 5 (b) for the three types of triangles.

Considering the standard SVM technique, $\bar{v}$ is obtained on the basis of the duty cycles $\mu, \lambda, \gamma$ :

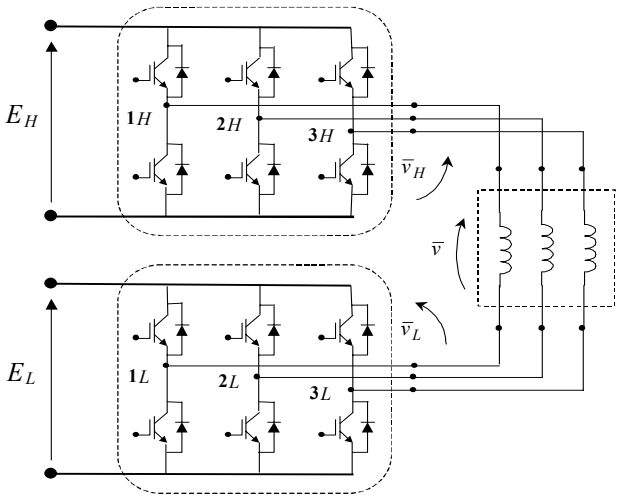



Fig. 3. Electric scheme of the multilevel converter.

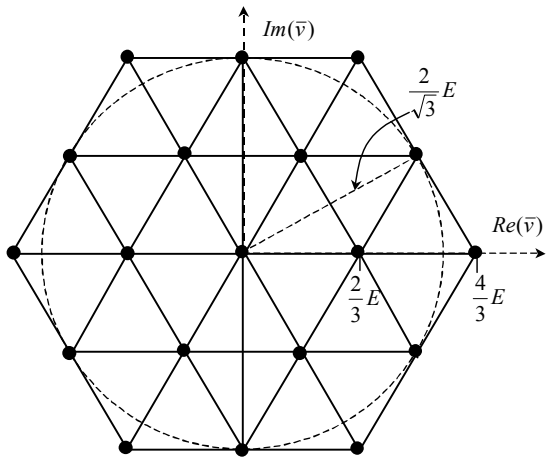



Fig. 4. Output voltage vectors of the multilevel converter.

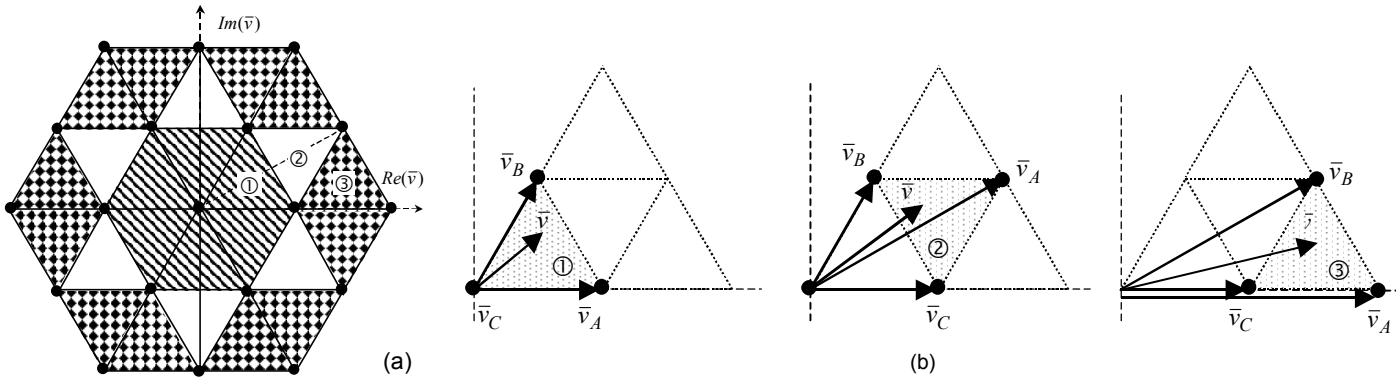



Fig. 5. (a) Highlight of the triangles in the three different regions ①, ②, and ③;
(b) Vector composition to obtain the output voltage in the three different regions.

$$\bar{v} = \mu \bar{v}_A + \lambda \bar{v}_B + \gamma \bar{v}_C . \tag{3}$$

where the duty cycle $\mu, \lambda, \gamma$ can be determined as

$$\begin{cases} \mu = \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \lambda = -\dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_A - \bar{v}_C)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \\ \gamma = 1 - (\mu + \lambda) = 1 - \dfrac{(\bar{v} - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_A)}{(\bar{v}_A - \bar{v}_C) \cdot j(\bar{v}_B - \bar{v}_C)} \end{cases} . \tag{4}$$

## III. Regulation of the Power Sharing

A novel modulation technique, able to share the output power $p$ between the two dc sources, is considered in this section. Introducing the power ratio $k$ and imposing the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ to be in phase with the output voltage vector $\bar{v}$, leads to the following equations (average values over a switching period):

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \\ p = \dfrac{3}{2}\bar{v} \cdot \bar{i} = p_H + p_L \end{cases} \quad \begin{cases} p_H = \dfrac{3}{2}\bar{v}_H \cdot \bar{i} = k \cdot p \\ p_L = \dfrac{3}{2}\bar{v}_L \cdot \bar{i} = (1-k) \cdot p \end{cases} \tag{5}$$

In order to synthesize an output vector $\bar{v}$, the two inverters must generate the corresponding fraction of $\bar{v}$ by applying only their active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector. Being $\bar{v}_H$ and $\bar{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$, as shown in Fig. 6. Then, the voltage generated by the two inverters are:

$$\begin{cases} \bar{v}_H = \mu_H \bar{v}_\alpha + \lambda_H \bar{v}_\beta \\ \bar{v}_L = \mu_L \bar{v}_\alpha + \lambda_L \bar{v}_\beta \end{cases} . \tag{6}$$

In (6) the duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *H*, whereas the duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *L*.

By using standard SVM equations, the duty-cycles of inverters *H* and *L* can be calculated as:

$$\begin{cases} \mu_H = \dfrac{\bar{v}_H \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} , \quad \gamma_H = 1 - (\mu_H + \lambda_H) \end{cases} , \tag{7}$$

$$\begin{cases} \mu_L = \dfrac{\bar{v}_L \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_L = -\dfrac{\bar{v}_L \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} , \quad \gamma_L = 1 - (\mu_L + \lambda_L) \end{cases} . \tag{8}$$

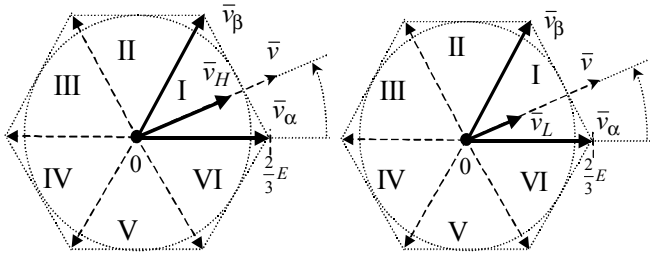



Fig. 6. Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

## IV. Determination of the Operating Limits

The constrains of the duty-cycles expressed by (8) are

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases}, \quad \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases}. \tag{9}$$

These constrains introduce a limit in the range of variation of the power ratio $k$. In particular, the range of variation of $k$ can be evaluated as a function of the desired output vector $\bar{v}$. Introducing in (9) the expressions (8) of duty cycles, and representing $\bar{v}_H$ and $\bar{v}_L$ in terms of $k$ by (5), leads to

$$\begin{cases} \dfrac{k\bar{v}\cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\dfrac{k\bar{v}\cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \dfrac{k\bar{v}\cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1 \end{cases}, \begin{cases} \dfrac{(1\text{-}k)\bar{v}\cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ -\dfrac{(1\text{-}k)\bar{v}\cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \geq 0 \\ \dfrac{(1\text{-}k)\bar{v}\cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \leq 1 \end{cases}. \tag{10}$$

Assuming sinusoidal output voltages $\left(\bar{v} = Ve^{j\vartheta}\right)$, and the modulation index $m$ defined as

$$m = V \Big/ \frac{2}{\sqrt{3}} E \,,\ 0 \leq m \leq 1 \,,$$

with reference to sector I ( $0 \leq \vartheta \leq \pi/3$ ), the solution of (10) is given by

$$\begin{cases} k \leq \dfrac{1}{2m} \dfrac{1}{\cos(\pi/6 - \vartheta)} \\ k \geq 1 - \dfrac{1}{2m} \dfrac{1}{\cos(\pi/6 - \vartheta)} \end{cases}, \tag{11a}$$

introducing the following parameter

$$a = \frac{1 - m\cos(\pi/6 - \vartheta)}{2m\cos(\pi/6 - \vartheta)}$$

in (11a) yields

$$\frac{1}{2} - a \leq k \leq \frac{1}{2} + a \,. \tag{11b}$$

Similar considerations can be made for sectors II ÷ VI. Eq. 11a gives the possible values of $k$ as a function of the modulation index $m$ and the output voltage phase angle $\vartheta$. It can be noted that for any modulation index, the most stringent condition for $k$ is given in the middle of the sector, i.e. for $\vartheta = \pi/6$. By applying this constrain, that corresponds to sinusoidal output voltages, the limit of the power ratio $k$ is given from (11a) as a function of the modulation index only. Admissible values of the power ratio k are represented by the dashed area shown in Fig. 7. By analyzing this figure the following considerations can be done.

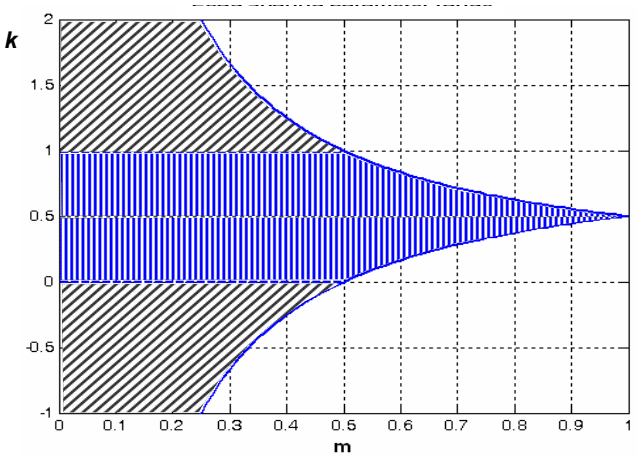



Fig. 7. Limits of the power ratio $k$ vs. the modulation index $m$.

- If the maximum output voltage is required ($m = 1$), there are no means to regulate the power sharing between the dc sources. In this case only the value $k = 0.5$ is admissible and the two sources supply the same voltages, i.e., the same power;
- for $0.5 \leq m \leq 1$ the ratio $k$ is limited as a function of $m$;
- for $m < 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if $k$ is set to 0, all the load power is supplied by inverter $L$, whereas if $k$ is set to 1 all the load power is supplied by inverter $H$. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only;
- for $m < 0.5$ the power ratio $k$ could be greater than unity or lower than zero. It means that an amount of power could be transferred from one dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase opposition, as shown by (5). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources.

## V. Determination of the Switching Sequence

Once the limits for $k$ has been defined, and the required inverter voltages $\bar{v}_H$ and $\bar{v}_L$ have been determined, the duty-cycles $\mu_H, \lambda_H, \gamma_H$ and $\mu_L, \lambda_L, \gamma_L$ can be calculated by (8) and (9). For achieving a correct multilevel operation, the three

TABLE I: SWITCHING SEQUENCE CORRESPONDING TO THREE-STEPS OPERATION FOR EACH INVERTER

| | region ① | | | | | region ② | | | | | | region ③ | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| output vectors | $\bar{v}_A$ | $\bar{v}_B$ | 0 | $\bar{v}_A$ | $\bar{v}_B$ | $\bar{v}_C$ | $\bar{v}_A$ | $\bar{v}_B$ | $\bar{v}_C$ | $\bar{v}_A$ | $\bar{v}_B$ | $\bar{v}_B$ | $\bar{v}_C$ | $\bar{v}_A$ | $\bar{v}_B$ | $\bar{v}_C$ |
| | $\bar{v}_\alpha$ | $\bar{v}_\beta$ | 0 | $\bar{v}_\alpha$ | $\bar{v}_\beta$ | $\bar{v}_\alpha$ | $\bar{v}_\alpha+\bar{v}_\beta$ | $\bar{v}_\beta$ | $\bar{v}_\alpha$ | $\bar{v}_\alpha+\bar{v}_\beta$ | $\bar{v}_\beta$ | $\bar{v}_\alpha+\bar{v}_\beta$ | $\bar{v}_\alpha$ | $2\bar{v}_\alpha$ | $\bar{v}_\alpha+\bar{v}_\beta$ | $\bar{v}_\alpha$ |
| $\bar{v}_H$ | 0 | | | $\bar{v}_\alpha$ | $\bar{v}_\beta$ | $\bar{v}_\alpha$ | | | 0 | $\bar{v}_\beta$ | | $\bar{v}_\alpha$ | | | $\bar{v}_\beta$ | 0 |
| $H$ duty cycles | $\gamma_H$ | | | $\mu_H$ | $\lambda_H$ | $\mu_H$ | | | $\gamma_H$ | $\lambda_H$ | | $\mu_H$ | | | $\lambda_H$ | $\gamma_H$ |
| $\bar{v}_L$ | $\bar{v}_\alpha$ | $\bar{v}_\beta$ | 0 | | | 0 | $\bar{v}_\beta$ | | $\bar{v}_\alpha$ | | 0 | $\bar{v}_\beta$ | 0 | $\bar{v}_\alpha$ | | |
| $L$ duty cycles | $\mu_L$ | $\lambda_L$ | $\gamma_L$ | | | $\leftarrow\gamma_L$ | $\lambda_L$ | | $\mu_L$ | | $\gamma_L\rightarrow$ | $\lambda_L$ | $\gamma_L$ | $\mu_L$ | | |
| sub-int. | $\mu$" | $\lambda$" | $\gamma$ | $\mu$' | $\lambda$' | $\gamma$' | $\mu$' | $\lambda$" | $\gamma$" | $\mu$" | $\lambda$' | $\lambda$' | $\gamma$' | $\mu$ | $\lambda$" | $\gamma$" |

output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, adjacent to the desired output voltage vector $\bar{v}$, must be generated by properly combining active vectors ($\bar{v}_\alpha, \bar{v}_\beta$) and null vector of the two inverters. For regions ①, ②, and ③ shown in Fig. 5, three different vector compositions are defined, according to the following equations

Region ① Region ② Region ③

$$\begin{cases} \bar{v}_A = \bar{v}_\alpha + 0 \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = 0 + 0 \end{cases} \quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \tag{12}$$

On the basis of (12), the duty-cycles for the vectors $\bar{v}_\alpha, \bar{v}_\beta$ and 0 of inverters $H$ and $L$, can be related to the duty-cycles $\mu, \lambda, \gamma$ of the output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$ calculated in (4).

For a given output vector $\bar{v}$ the two inverters $H$ and $L$ modulate with the same active vectors $\bar{v}_\alpha, \bar{v}_\beta$. It means that, at each interval of the switching period, the desired output vector can be obtained with interchangeable combinations of inverters vectors $\bar{v}_\alpha, \bar{v}_\beta, 0$. With reference to the three regions ①, ②, and ③ shown in Fig. 5, the proposed switching sequence is represented in Tab. I. In this switching sequence for example, when the output vector $\bar{v}_\alpha$ must be applied, the application time of $\bar{v}_\alpha$ can be subdivided in two equal sub-intervals. In the first time interval, inverter $H$ generates $\bar{v}_\alpha$ and inverter $L$ generates 0. In the second time interval, inverter $L$ generates $\bar{v}_\alpha$ and inverter $H$ generates 0. The same procedures can be adopted for generating the output vectors $\bar{v}_\beta$ and $\bar{v}_\alpha + \bar{v}_\beta$.

The duty cycles of the sub-intervals introduced in Tab. I can be determined for the three different regions on the basis of main duty-cycles $\mu, \lambda, \gamma$ and duty-cycles $\mu_H, \lambda_H, \gamma_H$, $\mu_L, \lambda_L, \gamma_L$ of the two inverters, as follows

Region ① Region ② Region ③

$$\begin{cases} \mu' = \mu_H \\ \mu'' = \mu_L \\ \lambda' = \lambda_H \\ \lambda'' = \lambda_L \\ \gamma \text{ is known} \\ - \end{cases} \quad \begin{cases} \mu' + \gamma' = \mu_H \\ \mu'' + \lambda' = \lambda_H \\ \lambda'' + \gamma'' = \gamma_H \\ \mu'' + \gamma'' = \mu_L \\ \mu' + \lambda'' = \lambda_L \\ \lambda' + \gamma' = \gamma_L \end{cases} \quad \begin{cases} \mu \text{ is known} \\ - \\ \lambda' = \lambda_L \\ \lambda'' = \lambda_H \\ \gamma' = \gamma_L \\ \gamma'' = \gamma_H \end{cases} \tag{13}$$

It can be noted that for regions ① and ③ the sub-intervals are five, whereas for region ② the sub-intervals are six and the corresponding duty cycles can be determined by solving a system of six equations. Only five of these equations are linear independent. Then, the equation system (13) for region ② can be solved in parametric form, assuming $\gamma'$ as parameter.

Introducing the condition that all intervals must be not negative, $\mu', \mu'', \lambda', \lambda'', \gamma', \gamma'' \geq 0$, the admissible range of parameter $\gamma'$ is determined. By choosing a value for $\gamma'$ inside this range, the values of the other sub-intervals duty cycles are determined by (14) as

$$\begin{cases} \mu' = \mu_H - \gamma' \\ \mu'' = \lambda_H - \gamma_L + \gamma' \\ \lambda' = \gamma_L - \gamma' \\ \lambda'' = \lambda_L - \mu_H + \gamma' \\ \gamma'' = \mu_L + \gamma_L - \lambda_H - \gamma' \end{cases} . \tag{14}$$

In particular, by selecting a proper value for $\gamma'$, it is always possible to null one of the six sub-intervals duty cycles. In this way the six-step commutation sequence collapses in five steps, as it happens in regions ① and ③.

Once all the sub-intervals are determined, they can be grouped in the switching sequence shown in Table I. In this

way, for each inverter, a traditional three-step commutation within the switching period is obtained, involving active and null vectors $\bar{v}_\alpha, \bar{v}_\beta$, 0.

## VI. Simulation Results

The double inverter configuration has been implemented in the Simulink environment of Matlab by using appropriate S-functions. The simulation results, based on the switching sequence shown in Tab.I are shown in Fig. 8.

Fig. 8(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, $m = 1$ ($v = 2/\sqrt{3}\ E$), and $k = 1/2$. In this case, the two inverters generate the same voltages, i.e., supply the same power. It can be noted that the output phase voltage is distributed on nine levels.

Fig. 8(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, $v = 2/3\ E$ ($m = 1/\sqrt{3}$), and $k = 2/3$. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being $k = 2/3$, the voltage generated by inverter $H$ are double with respect to voltage generated by inverter $L$.

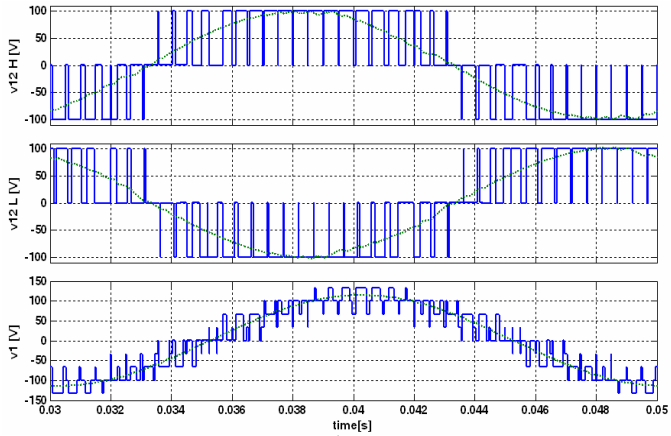
Fig. 8(c) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, $v = 1/\sqrt{3}\ E$ ($m = 1/2$), and $k = 1/3$. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio $k = 1/3$, the voltages and the power generated by inverter $H$ are the half with respect to the ones generated by inverter $L$.

The effectiveness of the multilevel modulation is proved by observing that in all the cases shown in Fig. 8 the output voltage is always distributed in three levels within every switching period, corresponding to the three triangle vertices $A$, $B$, $C$ of the vector diagram shown in Fig. 5(b).

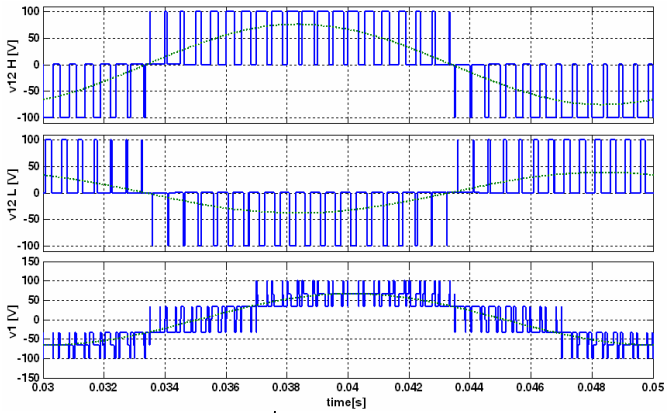
## VII. Experimental Results

The multilevel inverter has been tested by both a reduced scale prototype (Fig. 9) and a full size power converter (Fig. 10), realized in the Labs of the Department of Electrical Engineering in Bologna.

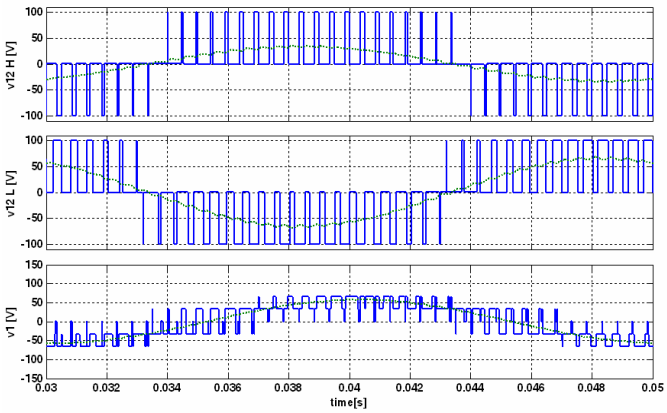
For both converters the control algorithm is based on the switching sequence presented in Table I. The proposed modulation strategy has been implemented on a control board based on TMS320F2812® DSP, operating with a clock frequency of 150 MHz, exploiting both its two independent three-phase PWM generators. In this way, no additional control hardware (e.g., FPGA) is necessary beside the DSP for switch commutation management.




(a) $\boldsymbol{m = 1}$ ($v = 2/\sqrt{3}\ E$), $\boldsymbol{k = 1/2}$ ($1-k = 1/2$)




(b) $\boldsymbol{m = 1/\sqrt{3}}$ ($v = 2/3\ E$), $\boldsymbol{k = 2/3}$ ($1-k = 1/3$)




(c) $\boldsymbol{m = 1/2}$ ($v = 1/\sqrt{3}\ E$), $\boldsymbol{k = 1/3}$ ($1-k = 2/3$)

Fig. 8. Voltage waveforms for different values of $m$ and $k$. From top to bottom: line-to-line voltage generated by inverter $H$; line-to-line voltage generated by inverter $L$; load phase voltage (output).

### *A. Reduced scale converter prototype*

The reduced scale system has been realized by using two modular inverters IR-AMS10UP60B® which assemble both power and driver circuits. These components are rated for a dc bus voltage of 450V and a phase current of 10A RMS (25°C).

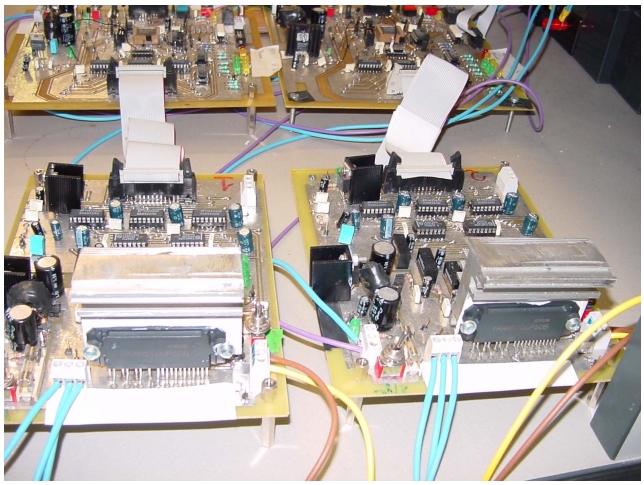


Fig. 9. Picture of the power stage of the reduced scale converter.

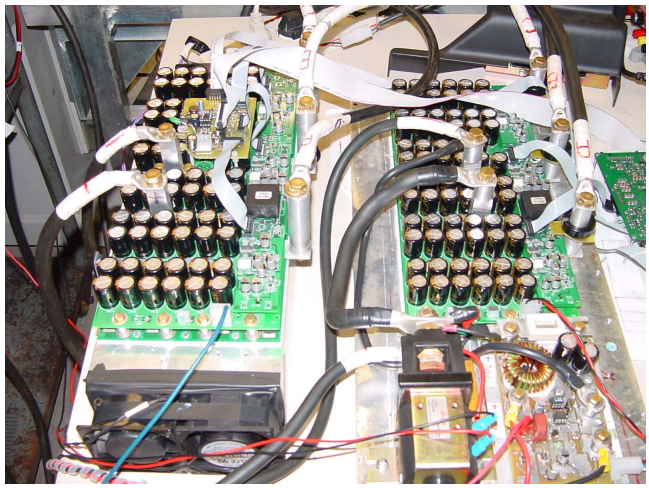


Fig. 10. Picture of the power stage of the full scale converter.

In Fig. 9 is shown a picture of the two power boards. Unfortunately the power and the control grounds are internally connected. Then, to make the required insulation between the two dc sources it has been necessary to introduce photo-couplers.

The experimental results are shown in Figs. 11. Fig. 11(a) shows the square wave operation of the multilevel converter (twelve-step). Fig. 11(b) shows the PWM operations over 9 levels of the load phase voltage, corresponding to the simulation results represented in Fig. 6(a) with a required voltage vector outside the inner hexagon. For both figures, the phase voltage and current are shown in the upper and in the lower trace, respectively.

*B. Full size power converter*

The power stage of the full size multilevel converter is depicted in Fig. 10. The two 'two-level' inverters have the main data reported in Table II.

In order to verify the power balancing capability of the multilevel converter, the averaged line-to-line output voltages with reference to different power ratio $k$ are investigated.
Fig. 12(a) shows the case of the same power delivered by each inverter ($k$ = 1/2), i.e., line-to-line voltages with the same amplitudes and in phase opposition.

Fig. 12(b) shows the case of a power unbalance ($k$ = 3/4), resulting in a corresponding line-to-line voltage unbalance.
The instantaneous output phase voltage is shown in Figs. 13 and 14 with reference to a different modulation index $m$.

Fig. 13 is referred to the case of an output voltage vector rotating on a circle inside the inner hexagon. Note that the output phase voltage is distributed on the lower five levels only, since only the triangles in region ① are involved.

Fig. 14 shows both the voltage (upper trace) and the phase current (lower trace) referred to an output voltage vector rotating on a circle outside the inner hexagon. In this case all the nine voltage levels are involved. The resulting sinusoidal waveform of the phase current proves the effectiveness of the multilevel modulation algorithm.

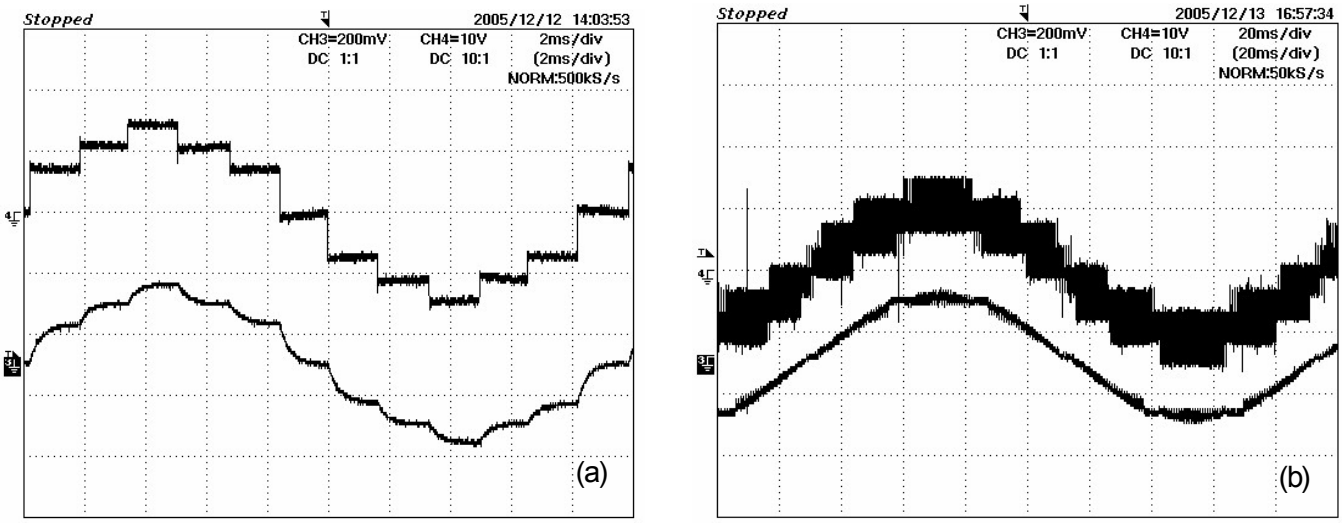



Fig. 11. Reduced scale converter prototype: (a) Square wave operation (twelve-step); (b) PWM operations (over 9 levels).

| Table II. CHARACTERISTICS OF THE POWER INVERTERS | |
|---|---|
| supply system | lead acid battery 80V, 500Ah |
| rated dc voltage | $E = V_{dc} = 80$ V |
| rated output current | $I_{S(RMS)} = 180$ A |
| maximum output current (t = 60", t = 240") | $I_{SM1(RMS)} = 600$ A , $I_{SM2(RMS)} = 450$ A |
| technology | MOSFETs - parallel connected on an Insulated Metal Substrate (IMS) |

## VIII. CONCLUSION

A multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding three-phase open-end winding loads has been considered in this paper. This scheme has the advantages of both avoiding homopolar components and maximizing the output voltage without additional circuitry. The paper has been focused on the development of a modulation strategy able to regulate the power sharing between the dc sources. It has been shown that balanced power sharing between the two inverters is always achievable within the switching cycle with correct multilevel voltage generation. Switching table for each inverter has been proposed and the limits of the power sharing ratio as function of the modulation index have been determined. Simulation results and experimental tests confirm the effectiveness of the proposed switching strategy.

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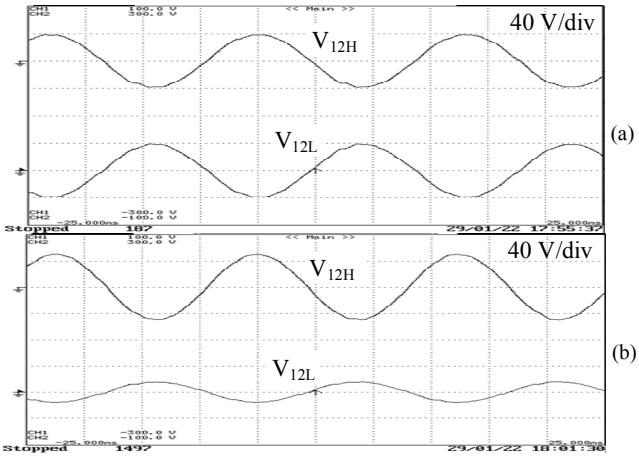


Fig. 12. Averaged line-to-line output voltages
(a) m=1/2, $k$ = 1/2 (balanced); (b) m=1/2, $k$ = 3/4 (unbalanced).


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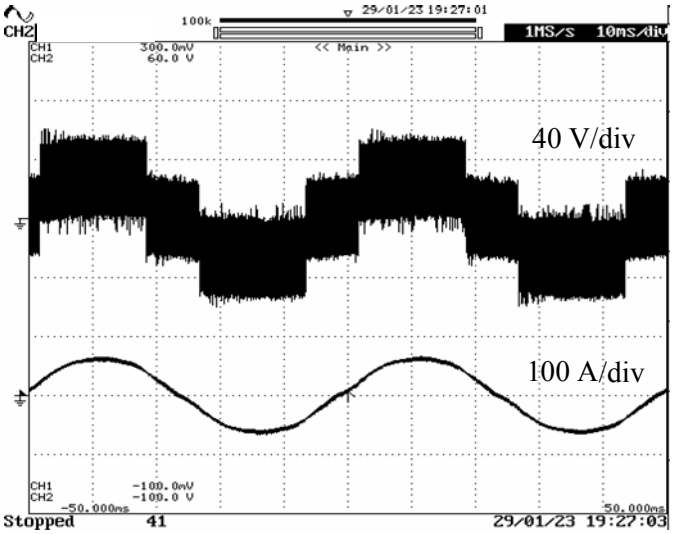


Fig. 13. Output phase voltage (over 5 levels) and current.

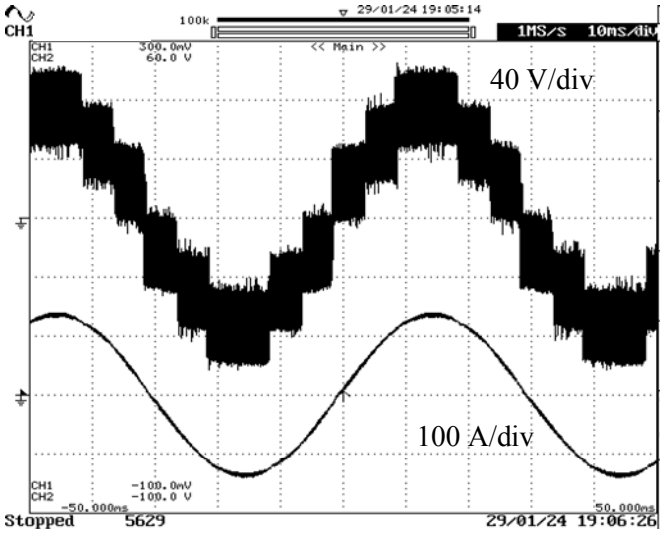


Fig. 14. Output phase voltage (over 9 levels) and current.