A New Multilevel Conversion Structure for Grid-Connected PV Applications

Gabriele Grandi, *Member, IEEE*, Claudio Rossi, *Member, IEEE*, Darko Ostojic, *Member, IEEE*, and Domenico Casadei, *Senior Member, IEEE*

***Abstract*—A novel scheme for three-phase grid-connected photovoltaic (PV) generation systems is presented in this paper. The scheme is based on two insulated strings of PV panels, each one feeding the dc bus of a standard two-level three-phase voltage-source inverter (VSI). The inverters are connected to the grid by a three-phase transformer having open-end windings on the inverter side. The resulting conversion structure performs as a multilevel power active filter (equivalent to a three-level inverter), doubling the power capability of a single VSI with given voltage and current ratings. The multilevel voltage waveforms are generated by an improved space-vector-modulation algorithm, suitable for the implementation in industrial digital signal processors. An original control method has been introduced to regulate the dc-link voltages of each VSI, according to the voltage reference given by a single maximum power point tracking controller. The proposed regulation system has been verified by numerical simulations and experimental tests with reference to different operating conditions.**

***Index Terms*—Multilevel systems, photovoltaic (PV) power systems, power conditioning.**

I. Introduction

BECAUSE of constantly growing energy demand, grid-connected photovoltaic (PV) systems are becoming more and more popular, and many countries have permitted, encouraged, and even funded distributed-power-generation systems. The technology still has shortcomings such as high initial-installation cost and low energy-conversion efficiency thus requiring continuous improvements of both cell and power-converter technologies [1]–[3].

The connection of the PV field to the ac grid is usually made with a voltage-source inverter (VSI), and it may include intermediate dc/dc chopper, transformer, or even both. In many countries, national electric standards require a transformer to achieve galvanic insulation of panels with respect to the grid. The presence of a dc/dc chopper allows the PV panels to operate over a wider voltage range, with a fixed inverter dc voltage and a simplified system design. On the other hand, the dc/dc chopper increases the cost and decreases the conversion efficiency at most operating points. Transformerless and high-frequency-transformer topologies are preferred for avoiding bulky low-frequency (LF) transformer but are usually limited to single-phase connections with powers of up to a few kilowatts.

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The authors are with the Department of Electrical Engineering, University of Bologna, 40136 Bologna, Italy (e-mail: gabriele.grandi@unibo.it; claudio.rossi@unibo.it; darko.ostojic@unibo.it; domenico.casadei@unibo.it).

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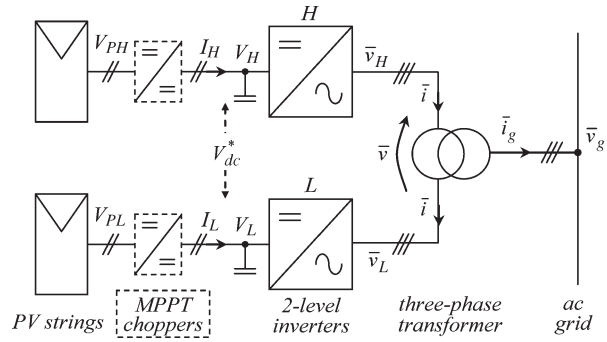


Fig. 1. Proposed dual-inverter configuration for the PV generation system.

Hence, PV-conversion schemes including a line-frequency transformer prevails in higher power three-phase systems, ranging from few tens of kilowatts up to megawatt power ratings.

The novel topology for PV grid-connected systems proposed by the authors in [4] and [5] (Fig. 1) is further developed in this paper, introducing some significant improvements related to the control algorithm. The conversion system utilizes a dual-inverter structure connected to the open-end primary windings of a standard three-phase transformer. The whole PV field is shared into two equal PV strings. Each inverter can be directly supplied by a PV string or through a dc/dc chopper (optional), as shown in Fig. 1. The secondary windings of the transformer can be connected to the grid either with a star or delta configuration. Note that the transformer contributes with its leakage inductance to the ac-link inductance, which is always necessary for coupling a VSI with the grid. Furthermore, the presence of an LF transformer enables voltage adaptation, allowing the direct connection of high-power generation systems to either low- or medium-voltage grids (10 kV or more).

The resulting three-phase converter is able to operate as a multilevel voltage inverter, which is equivalent to a three-level inverter, with reduced harmonic distortion and lower dv/dt in the output voltages. The main advantage of this topology is the simplified hardware structure with respect to the traditional three-level inverters. In fact, two standard six-transistor configurations can be readily utilized, without additional circuitry. Further details are given in the next section.

A novel control scheme including simple proportional–integral (PI) controllers is proposed to achieve the commanded value of dc voltages necessary for maximum power point tracking (MPPT) of PV panels. An improved space-vector (SV) modulation (SVM) strategy has been developed to provide proper multilevel waveform and simple implementation in industrial digital signal processors (DSPs). In this way, additional

logic circuitries [e.g., field-programmable gate array (FPGA)] for generating the firing signals of the power switches can be avoided.

In addition to power generation, the system can operate as an active filter, with additional features such as load balancing, harmonics compensation, and reactive-power injection.

II. Dual-Inverter Topology

Three-level inverters are a good tradeoff solution between performance and cost in multilevel converters for both medium- and high-power applications. The main advantages of three-level inverters over the standard two-level ones are the following: reduced voltage ratings for the switches, lower harmonic distortion (making possible the use of smaller and less-expensive filters), and good dynamic response. In particular, the waveform of the converter output phase voltage has up to nine levels.

Several three-level-inverter topologies have been introduced in the last years, the most important of them being the diode-clamped, the capacitor-clamped, and the cascaded converter [6], [7].

Among these topologies, cascaded converters have received large attention due to the simplicity of the power stage, since they do not require additional components such as diodes and capacitors. The main cascaded multilevel-inverter configurations are cascaded H-bridge, cascaded three-phase, and dual two-level inverters.

1) The well-known cascaded H-bridge configuration is scalable and easy to realize but has the disadvantage of multiple insulated dc sources (three for the three-level version) with oscillating power from each source (each H bridge behaves as single-phase inverter).
2) The cascaded three-phase-inverter configuration [8], [9] reduces the number of dc power supplies and avoids the need of galvanic insulation. It is a scalable structure, but the bottom inverter has not a standard connection layout, and all its switches must be rated with the full dc voltage [8].
3) The dual-inverter configuration [10], [11] consists of the simple connection of two standard two-level inverters to a three-phase open-winding load and performs as a three-level inverter. Although it is not scalable to get more voltage levels, it represents a viable solution to supply transformers and ac motors, particularly when the dc source can be easily split into two insulated parts, as for batteries and PV panels. This is the structure considered in the following.

In the dual-inverter configuration, the presence of two insulated dc sources inherently avoids the circulation of common-mode currents. In the case of a single dc source, common-mode currents can be prevented either by an additional three-phase common-mode reactor or by the application of a proper SVM algorithm. In this last case, common-mode voltages are not generated by the inverter but at the price of lower dc-bus voltage utilization [12].

With reference to the scheme shown in Fig. 1, using SV representation, the output-voltage vector $\overline{v}$ of the multilevel converter is given by the sum of the voltage vectors $\overline{v}_H$ and $\overline{v}_L$ generated by inverter H and L, respectively

$$\overline{v} = \overline{v}_H + \overline{v}_L \tag{1}$$

with

$$\begin{cases} \overline{v}_H = \frac{2}{3} V_H \left(S_{1H} + S_{2H} e^{j\frac{2}{3}\pi} + S_{3H} e^{j\frac{4}{3}\pi} \right) \\ \overline{v}_L = -\frac{2}{3} V_L \left(S_{1L} + S_{2L} e^{j\frac{2}{3}\pi} + S_{3L} e^{j\frac{4}{3}\pi} \right) \end{cases} \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverter legs [13]. The combination of the eight switching configurations for each three-phase inverter yields 64 possible switching states. If the two dc voltages are the same, i.e., $V_H = V_L = V_{\rm dc}$, these switching states correspond to only 19 different output-voltage vectors, including zero vector, as shown in Fig. 2. The redundancy of the switching states represents a degree of freedom which is useful to develop a modulation strategy that is able to regulate the power sharing between the two dc sources within each switching period, as discussed in Section IV.

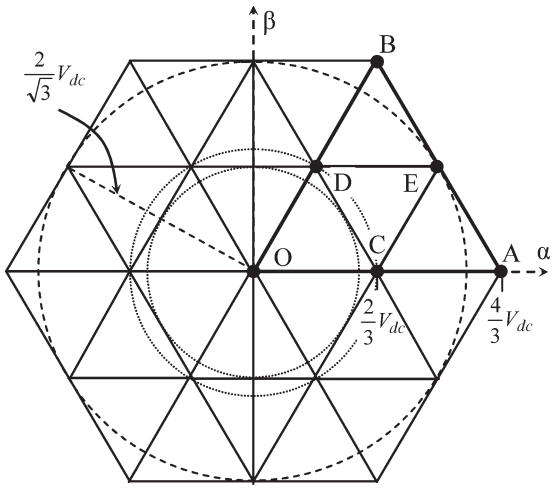


Fig. 2. Dual-inverter voltage-vector plot in the case $V_H = V_L = V_{\rm dc}$.

An alternative solution is to consider different dc voltage levels having a prefixed ratio (e.g., 1 : 2 or 1 : 3), loosing the redundancy of switching states but increasing the number of output-voltage levels [14], [15].

III. Converter Control

The PV conversion system considered in this paper is based on a symmetric structure, having two inverters with the same voltage and current ratings which are supplied by two equal strings of PV panels. It is worth noting that the control algorithm for the proposed dual-inverter is more complex than that for a single inverter. In fact, for single-inverter configuration, the only ac variable being controlled is the output current, whereas in case of a dual inverter, the ac-voltage sharing between two inverters "H" and "L" must be controlled as well. This additional degree of freedom has been addressed in this paper by a simple combination of PI controllers, as shown in Fig. 3. A more complex scheme has been previously adopted by

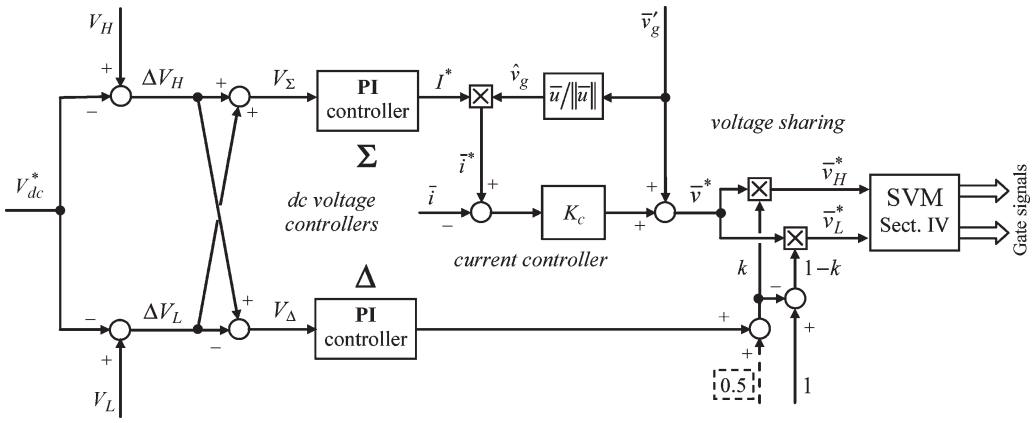


Fig. 3. Block diagram of the whole regulation system.

the authors in [4] and [5], with a solution for the power sharing between two battery banks in electric/hybrid traction systems based on the same dual-inverter configuration [9]. In [16], a multivariable linear quadratic regulator based on state-space models was proposed. It has been applied to the equivalent problem of dc-link neutral-point voltage regulation of a three-level neutral-point-clamped inverter. Another possibility is the independent control of each inverter but at the price of a loss of proper multilevel waveform [17].

A. DC-Voltage Controllers

With reference to the PV generation system shown in Fig. 1, two relevant configurations should be taken into account.

1) If the conversion scheme includes intermediate dc/dc choppers for the MPPT regulation (dashed blocks in Fig. 1), then each of the two PV strings can operate close to its own MPP, and both the dc inverter voltages V_H and V_L can be set to a fixed optimal value $V^*_{\rm dc}$ determined on the basis of both the inverter/transformer design and the ac-grid voltage level.
2) In the case of a direct connection between inverters and PV strings, $V_H = V_{PH}$ and $V_L = V_{PL}$, the MPPT action must be performed by the inverters, and the dc inverter voltages continuously change. Since the PV strings are supposed to be equal, being originated by a single PV field divided into two identical parts, a single MPPT regulation can be considered, as in the case of a single PV field.

For these reasons, the same dc-voltage reference $V^*_{\rm dc}$ for both inverters has been considered in this paper. Despite this assumption, V_H and V_L must be independently controlled to guarantee the system stability for any operating condition. A novel voltage-regulation scheme is here presented, according to the block diagram shown in Fig. 3, whereas the MPPT and other necessary supervisory tasks are not discussed further. In particular, dc voltages V_H and V_L are regulated by two PI controllers, hereafter called "sigma" (Σ) and "delta" (Δ). The voltage controller Σ acts in order to set the average value of the dc-bus voltages (i.e., their sum) to $V^*_{\rm dc}$, whereas the voltage controller Δ acts in order to equalize the dc-bus voltages (i.e., to zero their difference). The input signals of both voltage controllers V_Σ and V_Δ can be built by adding and subtracting one from the other the individual dc-voltage errors $\Delta V_H = V_H - V^*_{\rm dc}$ and $\Delta V_L = V_L - V^*_{\rm dc}$, as follows:

$$\begin{cases} V_\Sigma = \Delta V_H + \Delta V_L = (V_H + V_L) - 2V^*_{\rm dc} \\ V_\Delta = \Delta V_H - \Delta V_L = V_H - V_L. \end{cases} \tag{3}$$

B. AC-Current Controller

Since the two inverters "H" and "L" supplies the transformer's winding from both sides (open ends), their output ac current is the same: $\bar{i} = \bar{i}_H = \bar{i}_L$. An estimation of the magnitude of this current I could be based on the power-balance equation written in steady-state conditions, as proposed in [4] and [5]. In fact, if the inverter current injected into the grid is in phase with the grid voltage, the power balance yields

$$V_H I_H + V_L I_L = \frac{3}{2} V'_g I \tag{4}$$

where V'_g is the magnitude of the grid voltage at the inverter side. Note that in (4), the inverter and transformer losses are neglected. Thus, the reference magnitude of the ac current can be obtained from (4) as

$$I^* = \frac{2}{3} \frac{V_H I_H + V_L I_L}{V'_g}. \tag{5}$$

Equation (5) can be seen as a feedforward action able to compensate sudden changes in PV currents (I_H, I_L) [4], [5].

In this paper, a different solution has been proposed, reducing the computational requirements and simplifying the control scheme. In particular, the voltage controller Σ directly generates the current reference for the dual inverter I^* corresponding to the active power injected into the grid, as shown in Fig. 3. If the ac current is in phase with the grid voltage, the resulting current SV reference $\bar{i}^*$ is

$$\bar{i}^* = I^* \hat{v}_g \tag{6}$$

$\hat{v}_g$ being the unity SV of the grid voltage. It can be noted that the reactive and/or harmonic-compensation current references can be added to $\bar{i}^*$ if active power filter operation is required.

To solve the known problem of current control in a grid-connected application [18], a simple proportional controller

with feedforward action (grid voltage) has been adopted, due to its simplicity, good dynamic response, and immunity to harmonic disturbance. In particular, the reference voltage $\overline{v}^*$is calculated as

$$\overline{v}^* = K_c(\overline{i}^* - \overline{i}) + \overline{v}'_g \tag{7}$$

$\overline{v}'_g$ being the SV of the grid voltage at the inverter side. Although resonant controllers generally provide better characteristics compared with proportional controllers [19], this advantage becomes less relevant as the switching frequency increases. Furthermore, in the proposed system, a small steady-state current error is not a critical drawback, since the controlled variables are dc voltages [4], [5].

C. Voltage and Power Sharing

The reference output voltage $\overline{v}^*$ calculated by (7) can be synthesized as the sum of the voltages $\overline{v}^*_H$ and $\overline{v}^*_L$ generated by the two inverters, as expressed by (1). In order to equalize the two dc-bus voltages V_H and V_L, controller Δ directly determines how the total power should be shared between the two inverters "H" and "L" to compensate for the voltage unbalance, as shown in Fig. 3. Introducing a voltage ratio k and imposing the inverter-voltage vectors $\overline{v}^*_H$ and $\overline{v}^*_L$ to be in phase with the output voltage vector $\overline{v}^*$ yields

$$\begin{cases} \overline{v}^*_H = k\overline{v}^* \\ \overline{v}^*_L = (1-k)\overline{v}^*. \end{cases} \tag{8}$$

The condition expressed by (8) allows maximum dc-voltage utilization. With the output ac current of the two inverters being the same, the coefficient k also defines the power sharing between the two inverters. In terms of averaged values within the switching period, the output power can be expressed as

$$p = \frac{3}{2}\overline{v}^* \cdot \overline{i} = p_H + p_L \tag{9}$$

where p_H and p_L are the individual powers from the two inverters. Combining (8) with (9) leads to

$$\begin{cases} p_H = \frac{3}{2}\overline{v}^*_H \cdot \overline{i} = kp \\ p_L = \frac{3}{2}\overline{v}^*_L \cdot \overline{i} = (1-k)p. \end{cases} \tag{10}$$

The coefficient k has a limited variation range depending on the value of the reference output voltage $\overline{v}^*$, as already investigated by the authors in [9]. Furthermore, it has to be verified that both references are within the range of the achievable output voltages of each inverter, which depend on their dc voltages. In the case of a single-inverter topology, if the voltage demand exceeds the available dc voltage, the output voltage is simply saturated. With the dual-inverter configuration, total voltage reference must be satisfied; therefore, in case of voltage saturation of one inverter, the second has to provide for the missing part. This problem was addressed in [5].

IV. Multilevel Modulation Strategy

Once the inverter reference voltages $\overline{v}^*_H$ and $\overline{v}^*_L$ are determined by (8), they must be synthesized by the dual two-level inverter and applied to the open-end windings of the transformer.

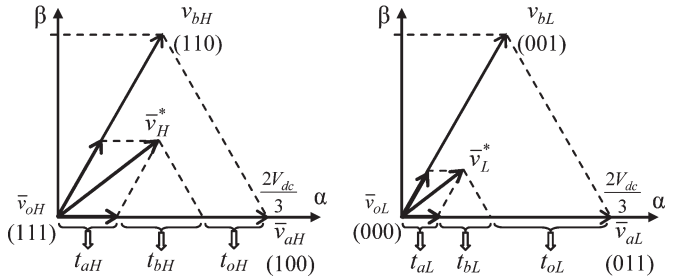


Fig. 4. SV composition of $\overline{v}^*_H$ and $\overline{v}^*_L$ by using the two adjacent active vectors for each inverter.

Generally, all pulsewidth modulators for dual inverter can be divided into two groups.

1) The first group uses two independent modulators for the two single inverters [17], [20]. This approach is characterized by simplicity and large degree of freedom, leading to an independent modulation of $\overline{v}_H$ and $\overline{v}_L$. However, it fails in proper multilevel-waveform generation, and, consequently, the output voltage includes higher harmonic distortion, and the dv/dt is increased.
2) The second group consists of composite modulators, which are able to produce proper multilevel voltage waveforms. As in the case of single inverter, there are carrier-based (CB) and SV pulsewidth modulations (PWMs). The earliest proposed CB modulation for dual three-phase inverters was sine-sawtooth modulation with carriers phase shifted by 180° [11]. Another known CB algorithm is a sine-triangle modulation adopted from the "phase-opposition disposition" approach of traditional three-level inverters [21], which can be easily extended to a dual-inverter configuration. Finally, an SV PWM has been proposed in [22] and [23], where the role of the two inverters is transposed at the end of each switching period in order to obtain a symmetric behavior. All the algorithms of this group can work only with identical reference voltages, i.e., $\overline{v}^*_H = \overline{v}^*_L$, and they cannot provide proper multilevel output voltage in case of different references.

An SVM method developed to overcome these problems has been presented in [13] and [24]. However, this method leads to switching sequences that cannot be implemented in the sole PWM generation unit of an industrial DSP. For this reason, a modified SVM algorithm, more suitable for an easier implementation, is presented in the following.

A. SV Composition

The proposed method is based on the voltage-vector composition shown in Fig. 4, with the assumption of equal dc voltages coming from the two strings of PV panels, $V_H = V_L = V_{\rm dc}$, as a result of the control-system operation. Due to the hexagonal symmetry, the analysis can be restricted to one of the six big sectors (i.e., OAB in Fig. 2), similar to the case of a standard three-phase SVM algorithm. Using SVM principle (Fig. 4), references $\overline{v}^*_H$ and $\overline{v}^*_L$ can be generated by selecting adjacent

vectors $\overline{v}_{aH}$, $\overline{v}_{bH}$, $\overline{v}_{oH}$ and $\overline{v}_{aL}$, $\overline{v}_{bL}$, $\overline{v}_{oL}$,[1] respectively. The application times of the active vectors can be calculated as

$$t_{aH} = \frac{3v_{\alpha H} - \sqrt{3}v_{\beta H}}{2V_{\rm dc}} T_S \qquad t_{aL} = \frac{3v_{\alpha L} - \sqrt{3}v_{\beta L}}{2V_{\rm dc}} T_S \tag{11}$$

$$t_{bH} = \frac{\sqrt{3}v_{\beta H}}{V_{\rm dc}} T_S \qquad t_{bL} = \frac{\sqrt{3}v_{\beta L}}{V_{\rm dc}} T_S \tag{12}$$

with $\overline{v}^*_H = v^*_{\alpha H} + jv^*_{\beta H}$, $\overline{v}^*_L = v^*_{\alpha L} + jv^*_{\beta L}$, and T_S being the switching period. The application times of the null vectors are given by

$$t_{oH} = T_S - t_{aH} - t_{bH} \qquad t_{oL} = T_S - t_{aL} - t_{bL}. \tag{13}$$

The switch configurations corresponding to the selected vectors cannot be applied in an arbitrary sequence if a proper multilevel voltage waveform is desired, i.e., the reference voltage $\overline{v}^*$ should be generated by using the nearest three-vector (NTV) approach [21]. Furthermore, it must be taken into account that the PWM generation unit of industrial DSPs allows up to two commutations within the switching period for each inverter leg.

B. Determination of Switching Sequence

In order to determine the switching sequence, the big triangle OAB is divided into four identical equilateral triangles denoted OCD (inner), CDE (intermediate), ACE and BDE (outers), as shown in Fig. 2. The voltage-reference vector $\overline{v}^*$ lays in one of these triangles, leading to the following four relevant cases.

1) Triangle OCD: For the inner triangle, the NTV are $\overline{v}_O$, $\overline{v}_C$, and $\overline{v}_D$, which can be obtained by the following combinations of voltage vectors selected for the two inverters: $(\overline{v}_{oH}, \overline{v}_{oL})$, $(\overline{v}_{aH}, \overline{v}_{oL})$ and $(\overline{v}_{oH}, \overline{v}_{aL})$, and $(\overline{v}_{bH}, \overline{v}_{oL})$ and $(\overline{v}_{oH}, \overline{v}_{bL})$, respectively. By using these combinations, since $\overline{v}^* = \overline{v}^*_H + \overline{v}^*_L$ is inside the inner triangle, for any value of $\overline{v}^*_H$ and $\overline{v}^*_L$ (Fig. 4), the total application time of the active vectors is

$$t_{aH} + t_{bH} + t_{aL} + t_{bL} \leq T_s. \tag{14}$$

Combining (13) with (14) yields

$$t_{oH} + t_{oL} \geq T_S. \tag{15}$$

Note that (15) provides a criterion for the identification of the inner triangle OCD. The voltage-vector combinations can be arranged within the switching period to obtain a switching sequence suitable for the implementation in PWM generation unit of industrial DSPs, as shown in Fig. 5(a). In the figure is emphasized the overlap between the two null vectors ($\overline{v}_{oH}$ and $\overline{v}_{oL}$), provided by (15), which allows the generation of $\overline{v}^*$ only by vectors $\overline{v}_O$, $\overline{v}_C$, and $\overline{v}_D$.

The proposed switching sequence belongs to symmetrical and discontinuous modulation, minimizing the number of commutations. A continuous modulation can be easily obtained by introducing the null vector $\overline{v}_O$ in the middle and at the ends of the switching period.

2) Triangle ACE: For the first outer triangle, the NTV are $\overline{v}_A$, $\overline{v}_C$, and $\overline{v}_E$, which can be composed by the combination of the following: $(\overline{v}_{aH}, \overline{v}_{aL})$, $(\overline{v}_{aH}, \overline{v}_{oL})$ and $(\overline{v}_{oH}, \overline{v}_{aL})$, and $(\overline{v}_{aH}, \overline{v}_{bL})$ and $(\overline{v}_{bH}, \overline{v}_{aL})$, respectively. Since $\overline{v}^*$ lies inside the triangle ACE, its component along $\overline{v}_{aH}$ is bigger than the amplitude of $\overline{v}_{aH}$ (see Fig. 2). Similar to the previous case, for application times, this consideration leads to

$$t_{aH} + t_{aL} \geq T_S. \tag{16}$$

Equation (16) provides a criterion for the identification of the outer triangle ACE. Moreover, in this case, the voltage-vector combinations can be arranged within the switching period to obtain a switching sequence suitable for the implementation in PWM generation unit of industrial DSPs, as shown in Fig. 5(b). In the figure is emphasized the overlap between the two active vectors ($\overline{v}_{aH}$ and $\overline{v}_{aL}$), provided by (16), which allows the generation of $\overline{v}^*$ only by vectors $\overline{v}_A$, $\overline{v}_C$, and $\overline{v}_E$.

Note that, as in the previous case of the inner triangle, the proposed sequence leads to symmetrical and discontinuous modulation.

3) Triangle BDE: For the second outer triangle, the NTV are $\overline{v}_B$, $\overline{v}_D$, and $\overline{v}_E$. Due to the symmetry of outer triangles ACE and BDE, this case can be treated as the previous one, involving vectors $\overline{v}_{bH}$ and $\overline{v}_{bL}$ instead of $\overline{v}_{aH}$ and $\overline{v}_{aL}$, respectively, leading to

$$t_{bH} + t_{bL} \geq T_S. \tag{17}$$

In addition, in this case, (17) provides a criterion for the identification of the outer triangle BDE. The proposed switching sequence is shown in Fig. 5(c).

4) Triangle CDE: For the intermediate triangle, the NTV are $\overline{v}_C$, $\overline{v}_D$, and $\overline{v}_E$, which can be generated by the combinations of the following: $(\overline{v}_{aH}, \overline{v}_{oL})$ and $(\overline{v}_{oH}, \overline{v}_{aL})$, $(\overline{v}_{bH}, \overline{v}_{oL})$ and $(\overline{v}_{oH}, \overline{v}_{bL})$, and $(\overline{v}_{aH}, \overline{v}_{bL})$ and $(\overline{v}_{bH}, \overline{v}_{aL})$, respectively. The following three conditions define the triangle CDE:

$$t_{oH} + t_{oL} \leq T_S \quad \text{(outside OCD)} \tag{18}$$

$$t_{aH} + t_{aL} \leq T_S \quad \text{(outside ACE)} \tag{19}$$

$$t_{bH} + t_{bL} \leq T_S \quad \text{(outside BDE)}. \tag{20}$$

The presence of (18)–(20) makes the case of the intermediate triangle CDE the most complex among the four considered cases.

The proposed switching sequence is shown in Fig. 5(d). The parameter t_x (denoted with gray) stands for a degree of freedom which determines the relative position of the switching sequence of one inverter with respect to the other (i.e., one of the sequences can be translated by the time interval t_x). A similar degree of freedom also exists in the previous three cases [gray intervals in Fig. 5(a)–(c)]. Since application times are given by (11)–(13), the remaining step is to choose the value for interval t_x, which completely determines the requirements for the DSP implementation. In particular, for the existence of

[1]Due to (2), the switch states for $\overline{v}_{aL}$, $\overline{v}_{bL}$ are opposite to the switch states of $\overline{v}_{aH}$, $\overline{v}_{bH}$, as shown in Fig. 4.

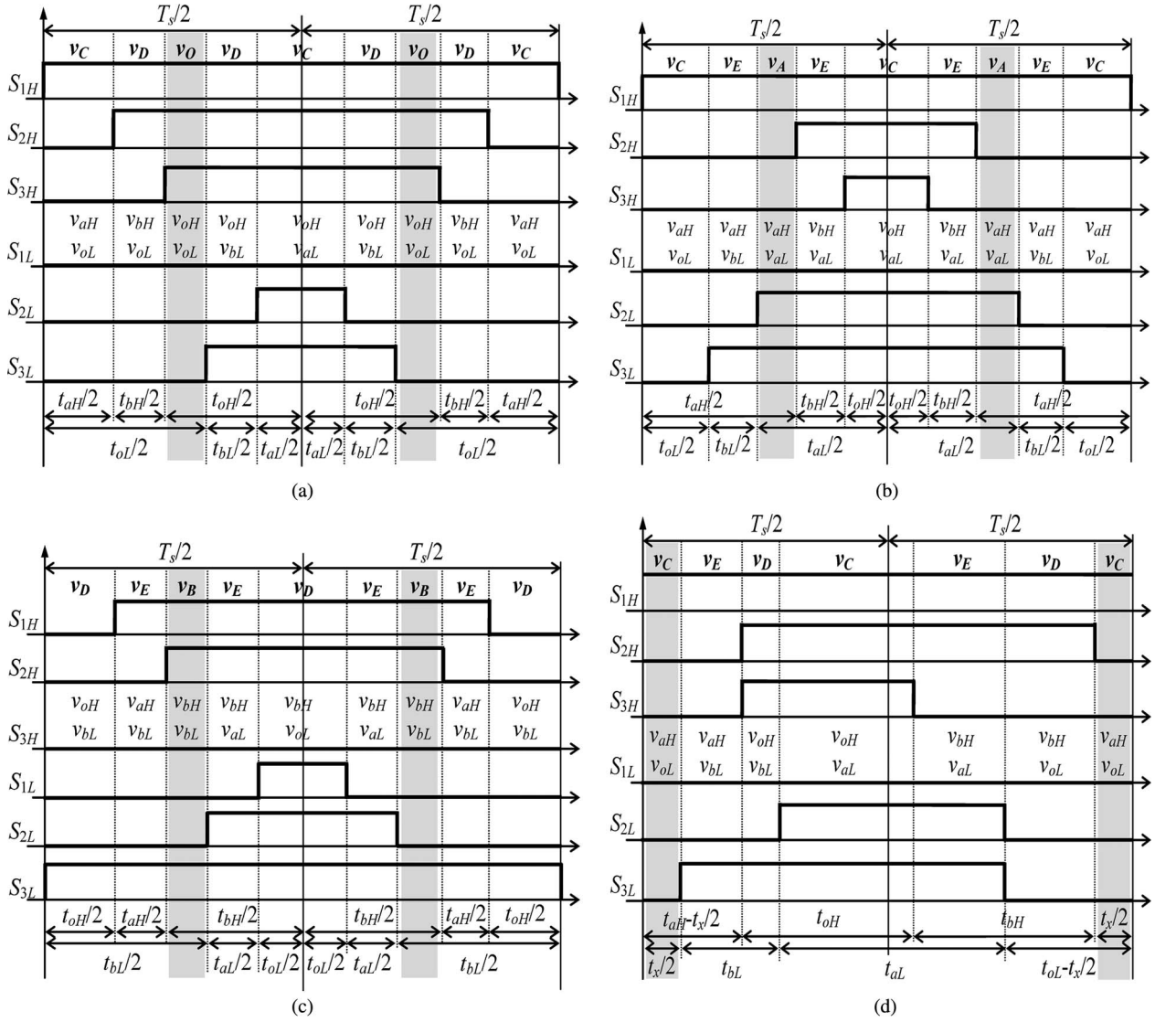


Fig. 5. Proposed switching sequences for the all four possible cases. (a) Switching sequence for the inner triangle OCD. (b) Switching sequence for the outer triangle ACE. (c) Switching sequence for the outer triangle BDE. (d) Switching sequence for the intermediate triangle CDE.

all the vector combinations shown in Fig. 5(d), t_x has to satisfy the following constraints:

$$t_x \geq 0 \tag{21}$$

$$t_x \geq t_{aH} - t_{bL} \tag{22}$$

$$t_x \geq t_{oL} - t_{bH} \tag{23}$$

$$t_x \leq t_{aH} \tag{24}$$

$$t_x \leq T_s - t_{bH} - t_{bL} \tag{25}$$

$$t_x \leq t_{oL}. \tag{26}$$

A detailed derivation of (21)–(26) is presented in the Appendix, together with the proof that a solution always exists.

The proposed switching sequence is discontinuous, as in the previous cases. The difference now is that a simultaneous commutation of two legs for both inverters H and L always occurs. It is possible to overcome this drawback by introducing the additional vectors $\overline{v}_{cH}$, $\overline{v}_{cL}$ and/or $\overline{v}_{dH}$, $\overline{v}_{dL}$ (shown in Fig. 6) in the SV decomposition (Fig. 4), leading to a more complex modulation algorithm which is outside the scope of this paper. A similar problem has been addressed in [24]. Despite the asymmetric distribution of pulses within the switching period, the proposed modulation can be implemented in the PWM generation unit of an industrial DSP, as proved by the experimental tests.

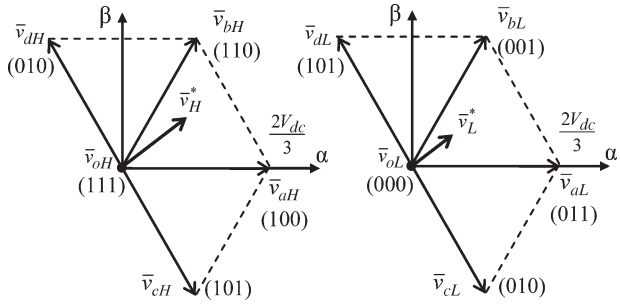


Fig. 6. Additional voltage vectors $\overline{v}_{cH}$, $\overline{v}_{cL}$, $\overline{v}_{dH}$, and $\overline{v}_{dL}$ useful for the vector composition to avoid simultaneous leg commutations (triangle CDE).

TABLE I
SUMMARY OF MAIN PARAMETERS OF PV CONVERSION SYSTEM

PV PANELS	
type	Shell Solar SQ150-C
string arrangement (H and L)	6 panels in parallel
connection cable resistance	43 [mΩ]
test condition: irradiance, cell temperature	900 [W/m^2], 50 [°C]
INVERTERS	
configuration (H and L)	two-level VSI
MOSFETs (6 in parallel per switch)	IRF2807
MOSFETs ratings	V_{DSS}=75[V]; R_{DS}=13[mΩ]
dc-bus capacitance	23 [mF]
switching frequency	20 [kHz]
TRANSFORMER and GRID	
turn ratio	230/24 [V/V]
converter/grid-side winding connection	open ends/star
rated power	1500 [VA]
short circuit voltage	6.9 [%]
ac link inductance (converter side)	0.4 [mH]
grid voltage (line-to-line), frequency	250 [V], 50 [Hz]

V. RESULTS

A complete PV generation system based on the proposed multilevel converter has been implemented in simulation and then realized as prototype. The system layout is based on parallel connection of PV panels. The presence of a grid transformer with the proper turn ratio enables voltage adaptation. The resulting PV string voltage is around 30–40 V, allowing the use of low-voltage high-current MOSFETs. These types of static switches are cheap and have good efficiency, since their ON-state resistance is a strong decreasing function of the blocking voltage rating ($V_{\rm DSS}$). Furthermore, low operating voltages guarantee the electric safety during experiments.

The main characteristics of the whole system are summarized in Table I. Reference is made to the scheme with the two PV strings directly connected to the inverters, without intermediate dc/dc choppers. In this case, the MPPT regulation is achieved by adjusting the dc voltage reference $V^*_{\rm dc}$ for both the two inverters.

Both numerical and experimental tests are referred to the same operating conditions and show the system response to the same step changes in $V^*_{\rm dc}$. The voltage excursion has been chosen to be large enough in order to verify both the dynamic response and the stability of the proposed control system.

A. Simulation Results

The numerical results have been obtained by implementing the whole PV generation system in MATLAB-Simulink environment. The system model parameters are based on the real laboratory prototype used for the experimental tests. The electrical model of each PV string was obtained by fitting the I–V characteristics of a parallel arrangement of six "*Solar Shell*" SP150 modules, including connection cables from the roof to the lab. A picture of the 12 PV panels used for the tests is given in Fig. 7(a). The I–V and P–V characteristics of the PV modules, given in Fig. 7(b), are related to the environmental condition during the experimental test in terms of solar irradiance and temperature of the module.

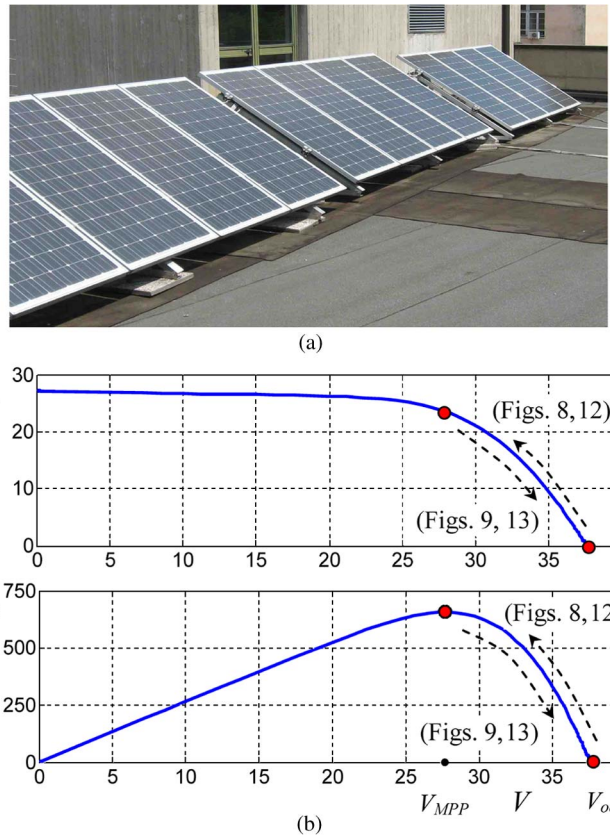


Fig. 7. PV panels utilized for tests. (a) Picture of the arrangement on the roof. (b) I–V and P–V characteristics of the two PV strings.

In the first case, Fig. 8, the voltage reference decreases from 38 to 27.5 V, approximately, corresponding to open−circuit voltage and MPP voltage, respectively [see Fig. 7(b)]. This step leads to a sudden increment of the PV generated power.

In particular, Fig. 8(a) shows the time response of dc voltages (V_H and V_L, blue lines) and dc currents (I_H and I_L, green lines) for the two inverters. It can be seen that the system reaches steady-state condition without overshoot in less than 40 ms, meaning only two periods of grid voltage.

The output of the dual inverter (ac voltage v, and ac current i) is shown in Fig. 8(b). During this transient, there is an increase of the modulation index due to the lowering of the dc voltage. As expected, the instantaneous values of the resulting output voltage v changes its waveform from seven-level (region between the two smaller circles in Fig. 2) to nine-level (region between the two larger circles in Fig. 2). These results confirm the correct operation of the multilevel-modulation technique in these regions. The resulting current ripple practically disappears, as shown in Fig. 8(b).

Fig. 8(c) shows that the grid voltage v_g (line-to-neutral) and grid current i_g are in phase, as expected. With the grid voltage being fixed, the current amplitude increases in response to the sudden change of the PV generated power. It can be noted that, for grid-connected application producing only active power, the MPP corresponds to the operating point with maximum grid-current amplitude.

The second case, Fig. 9, is related to the opposite step of the voltage reference $V^*_{\rm dc}$, from 27.5 to 38 V, yielding to a sudden decrement of PV generated power [see Fig. 7(b)].

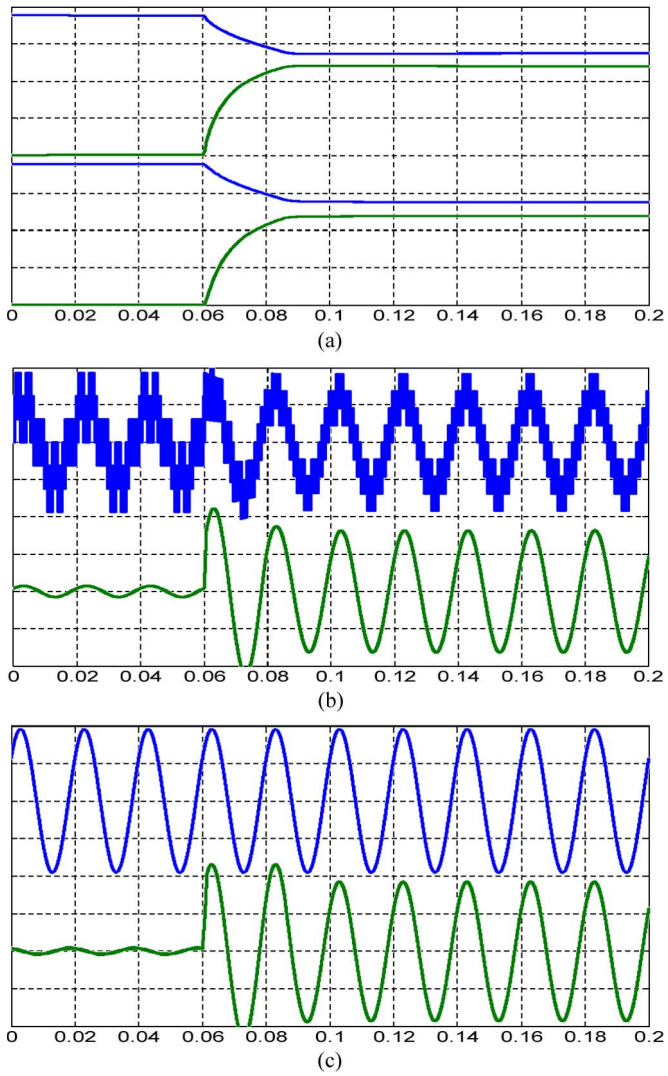


Fig. 8. Simulation: step change (decrease) of the reference dc voltage $V_{\rm dc}^*$ from 38 V to 27.5 V, time scale 20 ms/div (refer to Fig. 7). (a) From top to bottom: dc voltage (10 V/div) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) Top: converter ac voltage v (20 V/div), bottom: ac current i (20 A/div). (c) Top: grid voltage v_g (upper, 100 V/div), bottom: grid current i_g (lower, 2 A/div).

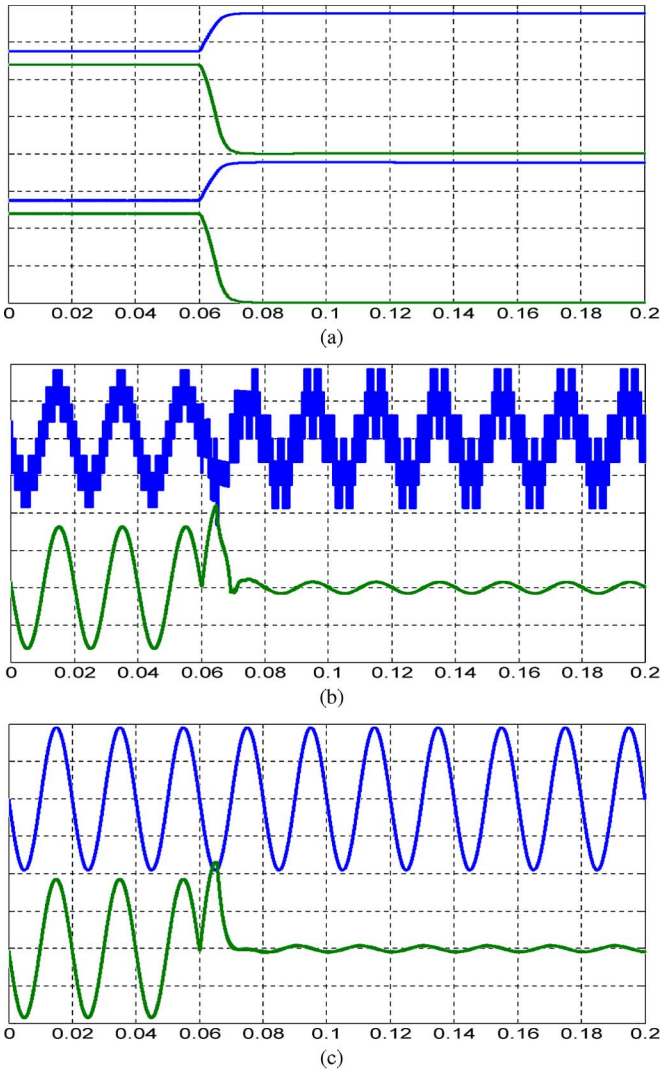


Fig. 9. Simulation: step change (increase) of the reference dc voltage $V_{\rm dc}^*$ from 27.5 V to 38 V, time scale 20 ms/div (refer to Fig. 7). (a) From top to bottom: dc voltage (10 V/div) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) Top: converter ac voltage v (20 V/div), bottom: ac current i (20 A/div). (c) Top: grid voltage v_g (upper, 100 V/div), bottom: grid current i_g (lower, 2 A/div).

Fig. 9(a) shows the time response of dc voltage (V_H and V_L, blue lines) and dc currents (I_H and I_L, green lines) for the two inverters. In addition, in this case, the system response is good, and the steady-state condition is reached in few ac periods, without overshoot.

The output of the dual inverter (ac voltage v and ac current i) during the transient is shown in Fig. 9(b). In this case, a decrease of modulation index due to the higher available dc voltage can be noted.

Fig. 9(c) shows grid voltage v_g and grid current i_g. The transient affects only the grid-current amplitude, as stated in the previous case.

B. Experimental Results

The control algorithm presented in Sections III and IV has been implemented in TMS320F2812 DSP. A picture of the hardware arrangement of the multilevel-converter prototype is shown in Fig. 10.

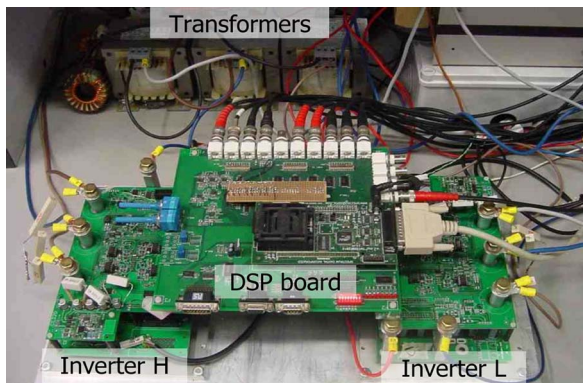


Fig. 10. Experimental setup.

First of all, the voltage waveforms generated by the dual-inverter configuration are shown to prove the effectiveness of the proposed SVM algorithm when implemented on a real DSP board. In particular, in Fig. 11 are depicted the individual

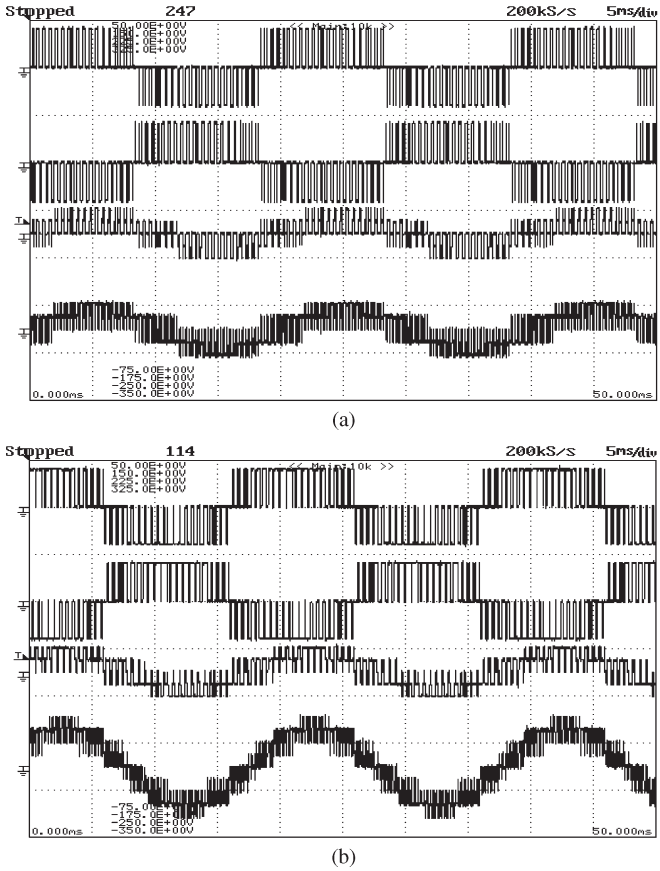


Fig. 11. From top to bottom: line-to-line voltages (v_{H12}, v_{L12}), artificial line-to-neutral voltage (v_{H1}), and converter output voltage (v_1) in two different cases. (a) AC reference voltage $v^* = 20$ V, $f = 50$ Hz (50 V/div). (b) AC reference voltage $v^* = 40$ V, $f = 50$ Hz (50 V/div).

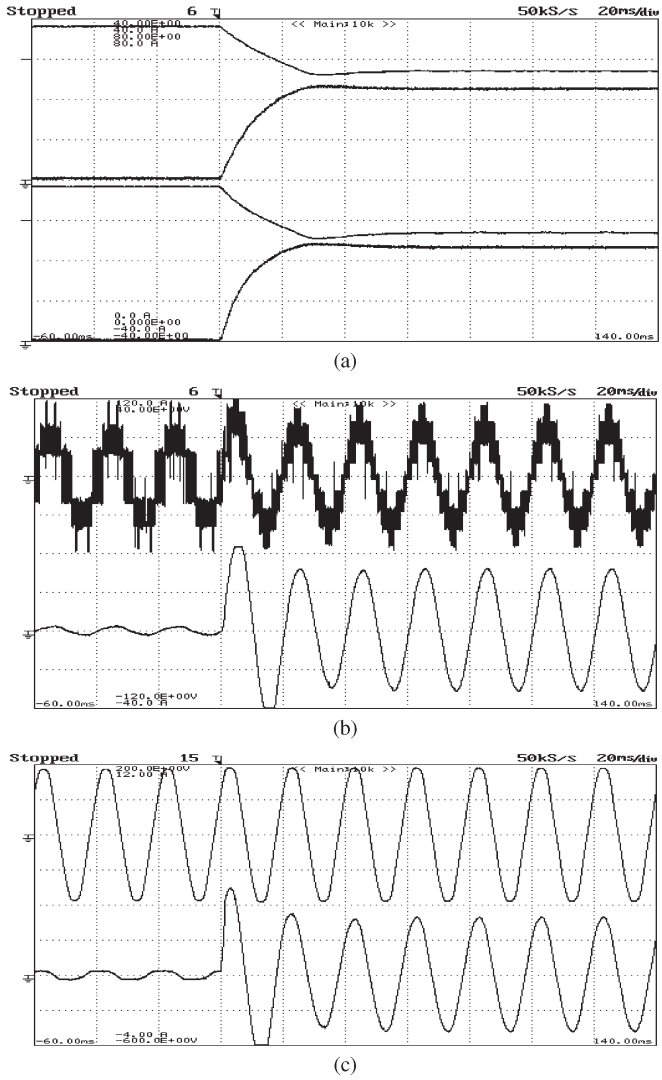


Fig. 12. Experiment: step change (decrease) of the reference dc voltage $V_{\rm dc}^*$ from 38 V to 27.5 V, 20 ms/div (refer to Fig. 7). (a) From top to bottom: dc voltage (10 V/div) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) Top: converter ac voltage v (20 V/div), bottom: ac current i (20 A/div). (c) Top: grid voltage v_g (upper, 100 V/div), bottom: grid current i_g (lower, 2 A/div).

inverter voltages (for both inverters "H" and "L") and the total output voltage of the converter in two different cases: 1) reference output voltage inside the inner hexagon $v^* = 20$ V and 2) reference output voltage between the inner and the outer hexagons, $v^* = 40$ V (reference is made to Fig. 2, $V_{\rm dc} \cong 38$ V). A reduced switching frequency has been chosen for the sake of readability (2 kHz instead of 20 kHz).

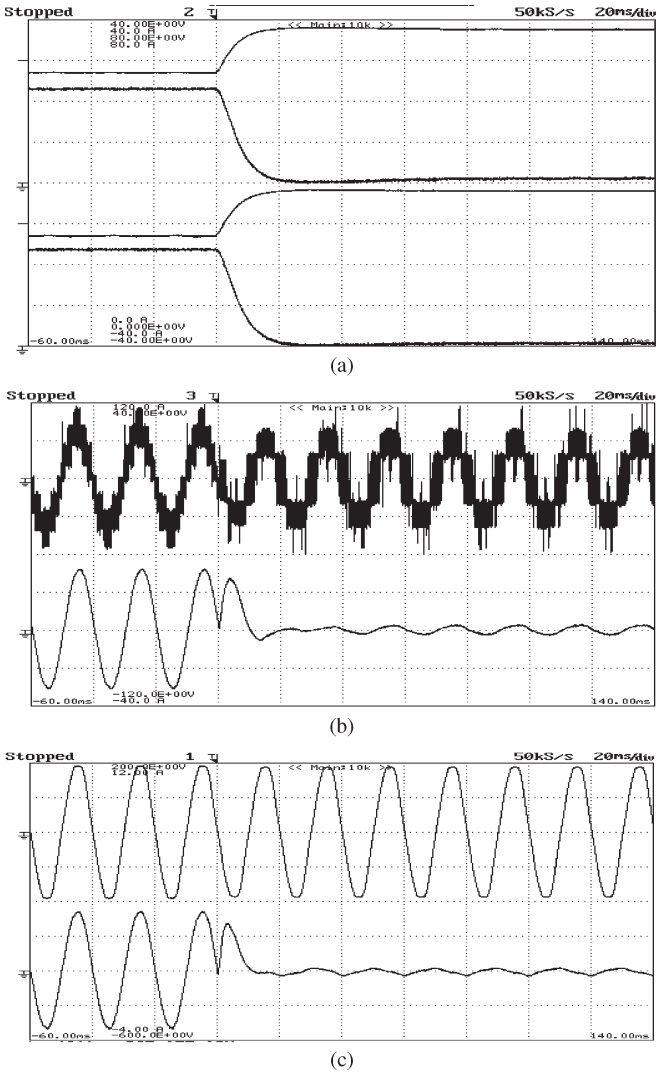
Fig. 11(a) shows that the output-voltage waveform (phase 1, v_1) is over five levels, whereas the line-to-line voltages (v_{H12}, v_{L12}) and the artificial line-to-neutral voltage (v_{H1}) are over three and five levels, respectively.

Fig. 11(b) shows that the output-voltage waveform is over nine levels. Note that both the line-to-line voltages and the artificial line-to-neutral voltage are still over three and five levels, respectively, as in the previous case.

The last experimental tests shown in Figs. 12 and 13 show the dynamic behavior of the system in response to step changes of the dc-voltage reference $V_{\rm dc}^*$ as for the simulation tests shown in Figs. 8 and 9.

In the first case, shown in Fig. 12, the voltage reference decreases with a step change from 38 to 27.5 V, thus, realizing about the same transient analyzed in the simulation of Fig. 8. In addition, in this case, diagrams (a), (b), and (c) are related to the dc side (H and L), ac converter side (v and i), and ac grid side (v_g and i_g) variables, respectively. Results show a good agreement with simulations, just the settling time is slightly higher, due to the neglected parasitic parameters (i.e., connection resistance, voltage drops across the MOSFETs, etc.).

In the second case, shown in Fig. 13, the voltage reference increases with a step from 27.5 to 38 V, introducing a sudden decrement of PV generated power, corresponding to the case analyzed in the simulation shown in Fig. 9. Fig. 13(a) shows the time behavior of dc voltages (V_H, V_L) and dc currents (I_H, I_L) for the two inverters. In addition, in this case, the system response is without overshoot, and the steady-state condition is reached in few ac periods, as in the simulations. The output of the dual inverter (ac voltage v and ac current i) during the transient is shown in Fig. 13(b). In this case, a decrease of modulation index due to the higher available dc voltage can be noted. Fig. 13(c) shows the grid voltage v_g and the grid current i_g. The results show good agreement with the corresponding simulations (Fig. 9).



(a)

(b)

(c)

Fig. 13. Experiment: step change (increase) of the reference dc voltage $V_{\rm dc}^*$, from 27.5 V to 38 V, 20 ms/div (refer to Fig. 7). (a) From top to bottom: dc voltage (10 V/div) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L. (b) Top: converter ac voltage v (20 V/div), bottom: ac current i (20 A/div). (c) Top: grid voltage v_g (upper, 100 V/div), bottom: grid current i_g (lower, 2 A/div).

VI. Conclusion

A novel power conversion scheme for the grid connection of a PV generation system has been analyzed and tested in this paper. The proposed topology includes two insulated PV strings and a three-phase open-end winding transformer. The power electronic converter consists of a dual three-phase inverter, i.e., the combination of two standard two-level VSI. The resulting output ac voltages have a multilevel waveform, equivalent to the one of a three-level inverter, with a reduced ac-current ripple. Furthermore, the energy generation is provided to the grid with a power factor that approaches unity, and additional active-filter tasks could be readily introduced. For the generation of the proper multilevel waveforms, a modified SVM algorithm has been presented, having the merit to be easily implemented in industrial DSP controllers without the need of additional hardware (e.g., FPGA). The regulation of the PV string voltages is directly performed by the inverters by means of an original control scheme.

The whole PV generation system has been implemented and verified by numerical simulations and experimental tests, showing good performance both in steady-state and transient operating conditions. In particular, the settling time in response to PV voltage transient is very small, on the order of tens of milliseconds. In this way, demands of MPPT controller due to solar irradiance and/or temperature changes can be easily satisfied.

Appendix
Inequalities for Intermediate Triangle

The following inequalities need to be satisfied in order to prove the existence of time intervals for all six vector combinations shown in Fig. 6(d). Starting from the left side of switching period the inequalities are the following:

1) $(\overline{v}_{aH}, \overline{v}_{oL}) \longleftrightarrow \overline{v}_C$

$$t_x/2 \geq 0 \tag{A1}$$

leading to (21);

2) $(\overline{v}_{aH}, \overline{v}_{bL}) \longleftrightarrow \overline{v}_E$

$$(t_{aH} - t_x/2) - t_x/2 \geq 0 \tag{A2}$$

leading to (24);

3) $(\overline{v}_{oH}, \overline{v}_{bL}) \longleftrightarrow \overline{v}_D$

$$(t_x/2 + t_{bL}) - (t_{aH} - t_x/2) \geq 0 \tag{A3}$$

leading to (22);

4) $(\overline{v}_{oH}, \overline{v}_{aL}) \longleftrightarrow \overline{v}_C$

$$(t_{aH} - t_x/2 + t_{oH}) - (t_{bL} + t_x/2) \geq 0 \tag{A4}$$

leading to (25) by introducing (13);

5) $(\overline{v}_{bH}, \overline{v}_{aL}) \longleftrightarrow \overline{v}_E$

$$(t_{bH} + t_x/2) - (t_{oL} - t_x/2) \geq 0 \tag{A5}$$

leading to (23);

6) $(\overline{v}_{bH}, \overline{v}_{oL}) \longleftrightarrow \overline{v}_D$

$$(t_{oL} - t_x/2) - t_x/2 \geq 0 \tag{A6}$$

leading to (26).

On the basis of (21)–(26), the solution for t_x exists if the following condition is satisfied:

$$\max\{0, t_{aH} - t_{bL}, t_{oL} - t_{bH}\} \leq \min\{t_{aH}, T_s - t_{bH} - t_{bL}, t_{oL}\}. \tag{A7}$$

Inequality (A7) can be proved by verifying, one by one, the nine possible combinations of (21)–(23) and (24)–(26). For this purpose, (13) and (18)–(20) must be applied. As an example, for pair (23) and (24), i.e.,

$$t_{oL} - t_{bH} \leq t_{aH}. \tag{A8}$$

Introducing (13) in (A8) yields

$$t_{oL} \leq T_s - t_{oH} \tag{A9}$$

which is proved by (18). A similar procedure can be used for the remaining combinations.

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Gabriele Grandi (M'00) received the M.Sc. (*cum laude*) and the Ph.D. degrees in electrical engineering from the Faculty of Engineering, University of Bologna, Bologna, Italy, in 1990 and 1994, respectively.

He has been with the Department of Electrical Engineering, University of Bologna, since he joined as a Research Associate in 1995 and has been an Associate Professor of electric and power electronic circuits since 2005. He has published more than 80 papers on conference proceedings and international journals. His main research interests are focused on power-electronic circuits and power-electronic converters for renewable energy sources.

Claudio Rossi (M'05) was born in Forlì, Italy, in 1971. He received the M.Sc. degree in electrical engineering and the Ph.D. degree from the University of Bologna, Bologna, Italy, in 1997 and 2001, respectively.

Since 2000, he has been with the University of Bologna where he is an Assistant Professor of electrical machines, drives and power electronics. His present research activity is devoted to power electronics and drives for electric vehicles and renewable energy systems.

Dr. Rossi is a Registered Professional Engineer in Italy.

Darko Ostojic (M'09) received the B.Eng. and M.Sc. degrees in electrical engineering from the University of Novi Sad, Novi Sad, Serbia, in 2002 and 2006, respectively. He is currently working toward the Ph.D. degree at the Faculty of Engineering, University of Bologna, Bologna, Italy.

From 2002 to 2006, he was with the Department of Electrical Engineering, University of Novi Sad, as a Research Assistant. His current research interests include control of power converters, photovoltaic generation, and power conditioning.

Domenico Casadei (SM'04) received the Ph.D. degree (with honors) in electrical engineering from the University of Bologna, Bologna, Italy, in 1974.

He has been with the University of Bologna since he joined the Institute of Electrical Engineering in 1975 and was a Research Assistant from 1975 to 1985, has been an Associate Professor since 1985, and is currently a Full Professor of electrical drives and the Head of the Electrical Engineering Department. His scientific work is related to electrical machines and drives and power electronics. He has published extensively in technical journals and conference proceedings. His current research interests include vector control of induction machines, multiphase machines, synchronous machines, electric vehicles, control of power converters, multilevel converters, renewable energy systems, and diagnosis of electrical machines.

Dr. Casadei is a Senior Member of the IEEE Industrial Electronics Society and a member of the Executive Committee of European Power Electronics Society.