Experimental investigation of a three phase multilevel converter based on two standard voltage source inverters with insulated dc supplies

Gabriele Grandi, Claudio Rossi, Alberto Lega, Domenico Casadei
Dept. of Electrical Engineering – University of Bologna
Viale Risorgimento 2, 40136 – Bologna, Italy
http://www.die.unibo.it

Abstract

An experimental investigation of a multilevel converter topology feeding three-phase open-end winding loads is proposed in this paper. The hardware scheme is based on two insulated dc supplies, each one feeding a standard two-level, three-phase inverter. A three-phase, six wires load is connected across the output terminals. A new modulation technique is considered, based on the space vector approach, able to regulate the sharing of the output power between the two dc sources within each switching cycle. The performances of the multilevel converter are discussed on the basis of a complete set of experimental tests.

1. Introduction

Multilevel converters represent a viable solution to overcame the voltage limits of power switching converters. They are able to generate output voltage waveforms consisting in a large number of steps, limiting the stress on the switching devices. In fact, higher voltage levels are synthesized from voltage sources with lower levels, with the additional benefit of a reduced harmonic distortion and dv/dt in the output voltage. These features have made multilevel converter suitable for application in the large and medium induction motor drives.
Several topologies of multilevel converters have been presented for low voltage applications [1]. Among these, the cascaded converter can be conveniently used with a battery supply system, because it is relatively easy to split the supply in several electrically separated sources.
In this paper a complete set of experimental tests on a multilevel converter composed by two standard two-level inverters [2]-[4] are given. This converter is able to supply and drive standard three-phase ac motors, in the open-end winding configuration. The scheme of the multilevel converter is shown in Fig. 1. This scheme is based on the use of insulated supplies, such as two banks of standard lead acid batteries. The three-phase six-wires load is connected across the six output terminals of the inverters. This solution should be preferred to other multilevel configurations because of some advantages: no generation of common mode (zero sequence) currents on the motor winding, best dc bus voltage utilization, use of two standard three-phase, two-level inverters. Furthermore, the dual inverter topology is a high reliability solution. In case of fault in one inverter, its output terminals can be short-circuited, and the drive operates using the other one as a standard three-phase two-level inverter. This possibility allows the operation of the motor at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed).
New switching techniques, based on a proper application of the space vector modulation (SVM), are discussed in the paper. The main feature of these techniques is the capability to regulate the load power sharing between the two dc sources within the switching period [5]. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks.
The capability of the multilevel converter are discussed on the basis of a complete set of experimental tests carried out on both a reduced size and a full power prototype.

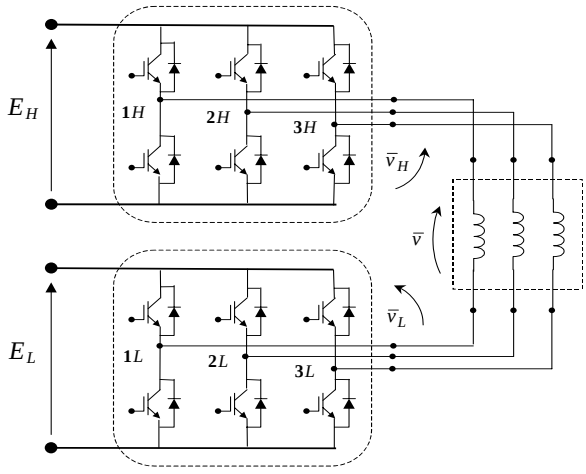


Fig. 1. Electric scheme of the multilevel converter.

2. Multilevel modulation strategy

With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter *H* and inverter *L*, respectively:

$$\bar{v} = \bar{v}_H + \bar{v}_L \ . \qquad (1)$$

The voltages $\bar{v}_H$ and $\bar{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to:

$$\bar{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\, e^{j\frac{2}{3}\pi} + S_{3H}\, e^{j\frac{4}{3}\pi}\right), \text{ and}$$

$$\bar{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\, e^{j\frac{2}{3}\pi} + S_{3L}\, e^{j\frac{4}{3}\pi}\right), \qquad (2)$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs.
The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 2. By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 *E*. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2/\sqrt{3}\ E$ (i.e., the radius of the inscribed circle).
The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 3(a), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted). In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\bar{v}$ is synthesized by using the vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, as represented in Fig. 3 (b) for the three types of triangles.
Considering the standard SVM technique, $\bar{v}$ is obtained on the basis of the duty cycles μ, λ, γ:

$$\bar{v} = \mu\,\bar{v}_A + \lambda\,\bar{v}_B + \gamma\,\bar{v}_C \ . \qquad (3)$$

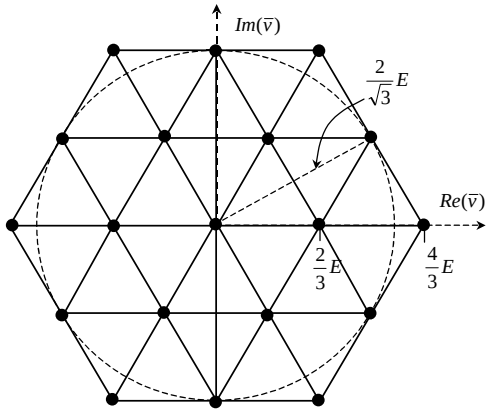


Fig. 2. Output voltage vectors of the multilevel converter.

3. Regulation of the Power Sharing

A novel modulation technique, able to share the output power *p* between the two dc sources, is considered in this section. Introducing the power ratio *k* and assuming the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ in phase with the output voltage vector $\bar{v}$, leads to the following equations (average values over a switching period):

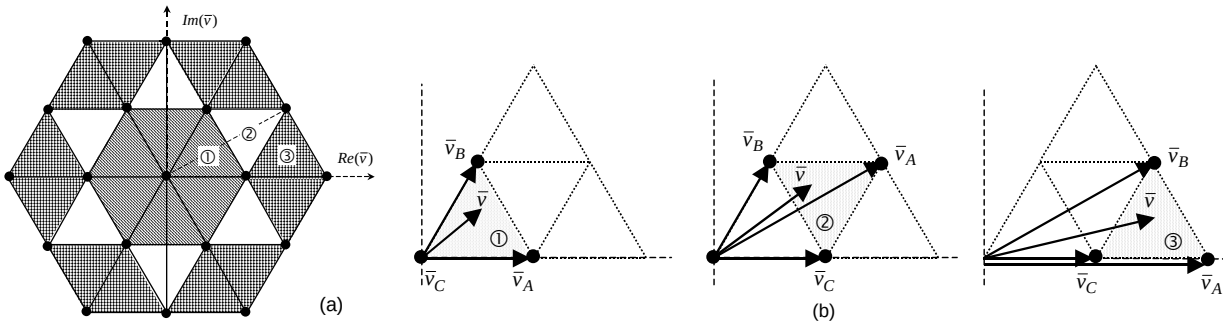


Fig. 3. (a) Highlight of the triangles in the three different regions ①, ②, and ③;
(b) Vector composition to obtain the output voltage in the three different regions.

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \end{cases} \qquad \begin{cases} p_H = \frac{3}{2}\bar{v}_H \cdot \bar{i} = k \cdot p \\ p_L = \frac{3}{2}\bar{v}_L \cdot \bar{i} = (1-k) \cdot p \end{cases} \qquad (4)$$
$$p = \frac{3}{2}\bar{v} \cdot \bar{i} = p_H + p_L$$

In order to synthesize an output vector $\bar{v}$, the two inverters must generate the corresponding fraction of $\bar{v}$ by applying only their active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector. Being $\bar{v}_H$ and $\bar{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$, as shown in Fig. 4.

The duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *H*. The duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *L*. In this way, the voltage generated by the two inverters are:

$$\begin{cases} \bar{v}_H = \mu_H\,\bar{v}_\alpha + \lambda_H\,\bar{v}_\beta \\ \bar{v}_L = \mu_L\,\bar{v}_\alpha + \lambda_L\,\bar{v}_\beta \end{cases} . \qquad (5)$$

By using standard SVM equations, the duty-cycles of inverters *H* and *L* are given by:

$$\begin{cases} \mu_H = \dfrac{\bar{v}_H \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \quad \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \;,\quad \gamma_H = 1-(\mu_H + \lambda_H) \end{cases} , \qquad (6)$$

$$\begin{cases} \mu_L = \dfrac{\bar{v}_L \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_L = -\dfrac{\bar{v}_L \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \;,\quad \gamma_L = 1-(\mu_L + \lambda_L) \end{cases} . \qquad (7)$$

4. Determination of the operating limits

The constrains of the duty-cycles are:

$$\begin{cases} \mu_H \geq 0 \\ \lambda_H \geq 0 \\ \mu_H + \lambda_H \leq 1 \end{cases} \text{ and } \begin{cases} \mu_L \geq 0 \\ \lambda_L \geq 0 \\ \mu_L + \lambda_L \leq 1 \end{cases} . \qquad (8)$$

These constrains introduce a limit in the range of variation of the power ratio *k*. In particular, the range of variation of *k* can be evaluated as a function of the modulation index *m* ($0 \leq m \leq 1$ for sinusoidal output voltages).

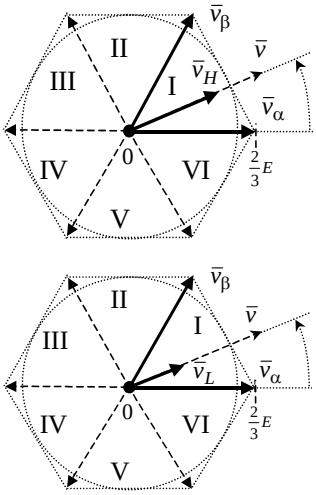


Fig.4. Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

Fig. 5 shows the upper and lower limits of *k* with reference to sinusoidal output voltages as a function of the modulation index *m*. It can be noted that for $m < 0.5$ the power ratio *k* could be greater than unity and lower than zero. It means that an amount of power could be transferred from a dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase oppositions, as shown in (4). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources. In this paper only the range $0 \leq k \leq 1$ is discussed. For $m \leq 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if *k* is set to 0 all the load power is supplied by inverter *L*, whereas if *k* is set to 1 all the load power is supplied by inverter *H*. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only.

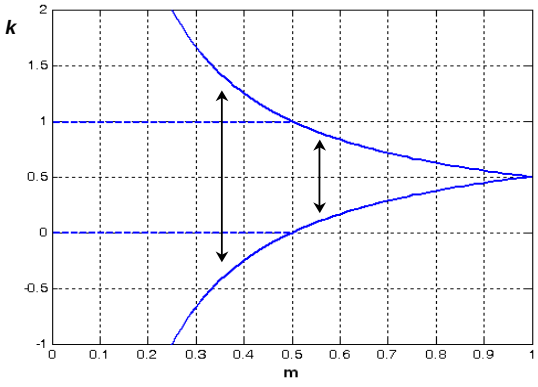


Fig. 5. Limits of the power ratio *k* as function of the modulation index *m*.

6. Numerical simulations

The double inverter configuration has been implemented in the Simulink environment of Matlab by using appropriate S-functions. The simulation results, based on the switching table presented in [5], are shown in Fig. 6.

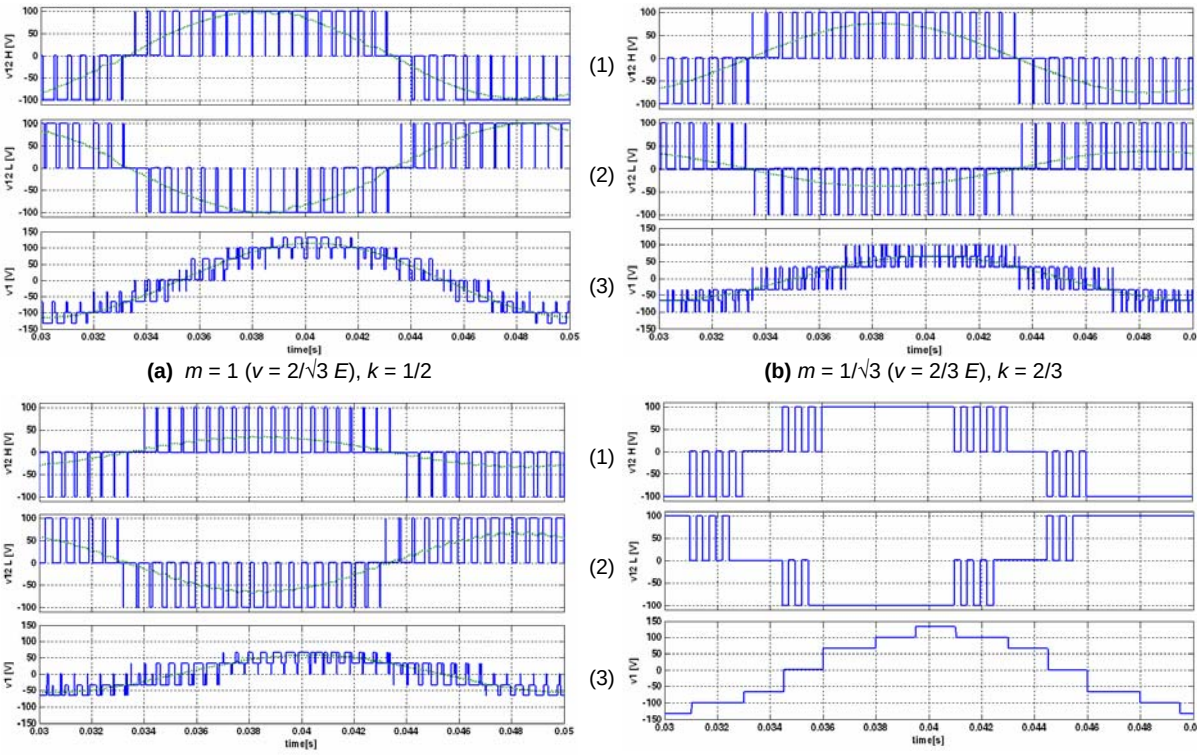
Fig. 6(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, m = 1 (v = 2/√3 E), and k = 1/2. In this case, the two inverters generate the same voltages, i.e., supply the same power. It can be noted that the output phase voltage is distributed on nine levels.

Fig. 6(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, v = 2/3 E (m = 1/√3), and k = 2/3. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being k = 2/3, the voltages and the power generated by inverter H are double with respect to the ones generated by inverter L.

Fig. 6(c) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, v = 1/√3 E (m = 1/2), and k = 1/3. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio k = 1/3, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that the output voltage is always distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 3(b).

Fig. 6(d) shows the waveforms corresponding to the twelve-step behavior of the multilevel converter, with a power ratio k = 1/2. In this case, only the output main vectors $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and $\bar{v}_\alpha + \bar{v}_\beta$ are involved; each vector is applied for a time interval equal to 1/12 of the fundamental period, and the output phase voltage is distributed on seven levels. In particular, the output vector $\bar{v}_\alpha + \bar{v}_\beta$ is obtained by combining $\bar{v}_\alpha, \bar{v}_\beta$ or $\bar{v}_\beta, \bar{v}_\alpha$, whereas the vectors $2\bar{v}_\alpha$ and $2\bar{v}_\beta$ correspond to the applications of $\bar{v}_\alpha$ and $\bar{v}_\beta$ for each inverter, respectively. In this way, the commutations of the inverters allow the power sharing within each switching period, while the output voltage behaves in the twelve-step mode.



(a) m = 1 (v = 2/√3 E), k = 1/2

(b) m = 1/√3 (v = 2/3 E), k = 2/3

(c) m = 1/2 (v = 1/√3 E), k = 1/3

(d) twelve-step, k = 1/2

Fig. 6. Voltage waveforms for different values of m and k: (1) line-to-line voltage generated by inverter H; (2) line-to-line voltage generated by inverter L; (3) load phase voltage (output).

7. Experimental tests

The multilevel inverter has been tested by both a reduced scale prototype and a full size power converter, realized in the Labs of the Dept. of Electrical Engineering in Bologna.
For both converters the control algorithm is based on the switching tables presented in [5]. It has been implemented on a control board based on TMS320F2812® DSP, operating with a clock frequency of 150 MHz, exploiting both its two independent three-phase PWM generators. In this way, no additional control hardware (e.g., FPGA) is necessary beside the DSP for switch commutation management.

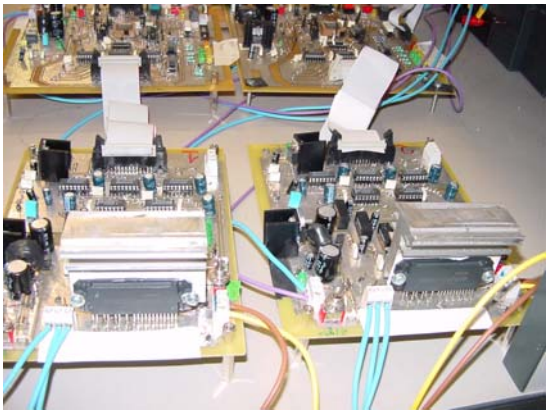


Fig. 7. Picture of the reduced scale converter prototype.

Reduced scale converter prototype

The reduced scale system has been realized by using two modular inverters IR-AMS10UP60B® which assemble both power and driver circuits. These components are rated for a dc bus voltage of 450V and a phase current of 10A RMS (25°C). In Fig. 7 is shown a picture of the two power boards. Unfortunately the power and the control grounds are internally connected. Then, to make the required insulation between the two dc sources it has been necessary to introduce photo-couplers.

The experimental results are shown in Figs. 8.
Fig. 8(a) shows the square wave operation of the multilevel converter (twelve-step), corresponding to the simulation results represented in Fig. 6(d).
Fig. 8(b) shows the PWM operations over 9 levels of the load phase voltage, corresponding to the simulation results represented in Fig. 6(a) with a required voltage vector outside the inner hexagon. For both figures, the phase voltage and current are shown in the upper and in the lower trace, respectively.

Full size power converter

The power stage of the full size multilevel converter is depicted in Fig. 9. The two 'two-level' inverters have the main data reported in Table I.

Table I. CHARACTERISTICS OF THE POWER INVERTERS

supply system	lead acid battery 80V, 500Ah
rated dc voltage	$E = V_{dc} = 80$ V
rated current	$I_{S(RMS)} = 180$ A
maximum current (t = 60", t = 240")	$I_{SM1(RMS)} = 600$ A , $I_{SM2(RMS)} = 450$ A
technology	MOSFETs - parallel connected on an Insulated Metal Substrate (IMS)

In order to verify the power balancing capability of the multilevel converter, the averaged line-to-line output voltages with reference to different power ratio *k* are investigated.
Fig. 10(a) shows the case of the same power delivered by each inverter (*k* = 1/2), i.e., line-to-line voltages with the same amplitudes and in phase opposition.
Fig. 10(b) shows the case of a power unbalance (*k* = 3/4), resulting in a corresponding line-to-line voltage unbalance.

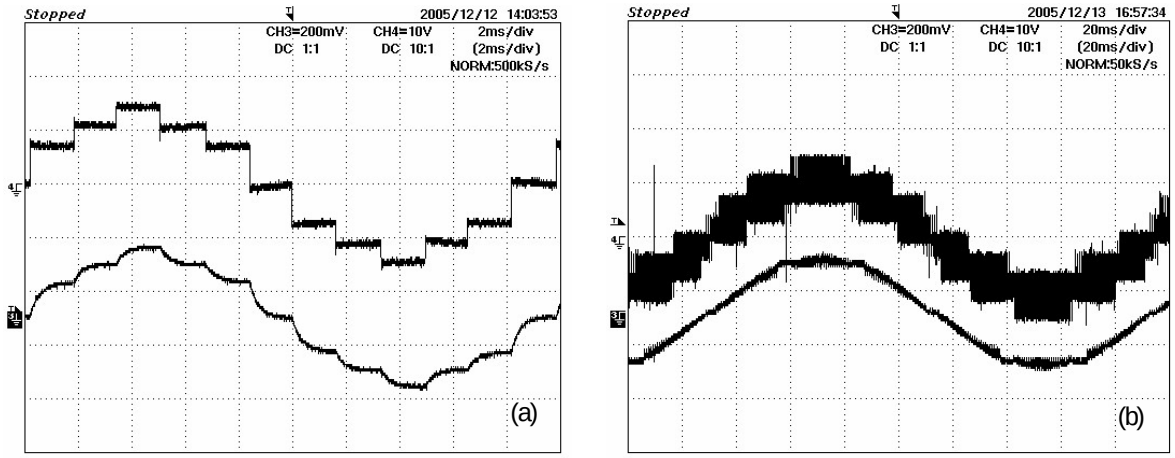


Fig. 8. Reduced scale converter prototype: (a) Square wave operation (twelve-step); (b) PWM operations (over 9 levels).

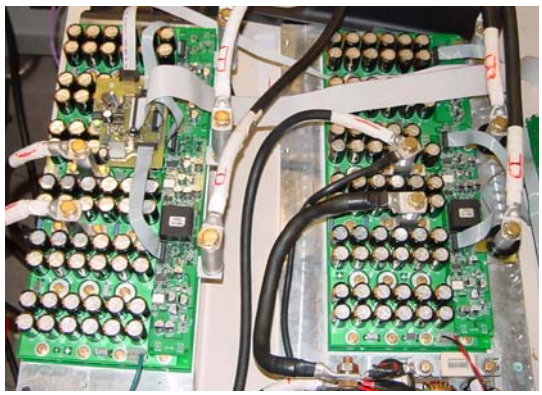


Fig. 9. Picture of the power stage of the full size converter.

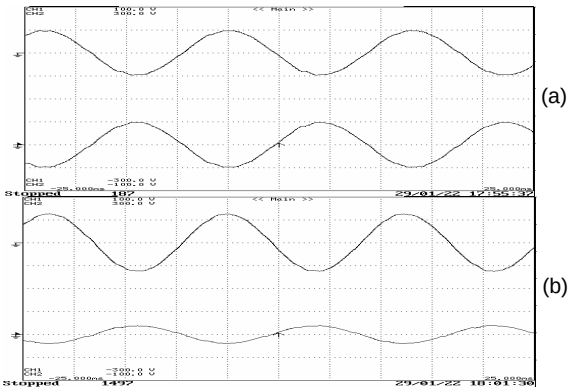


Fig. 10. Averaged line-to-line output voltages:
(a) k = 1/2 (balanced); (b) k = 3/4 (unbalanced).

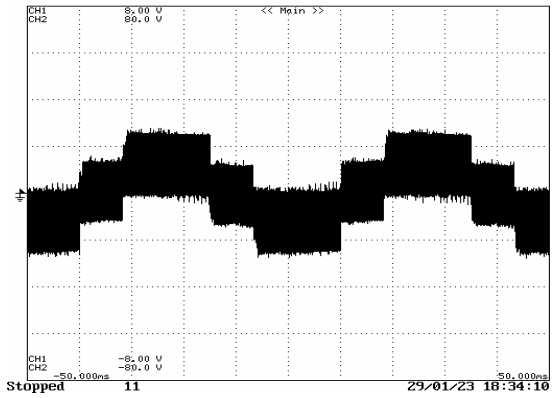


Fig. 11. Output phase voltage (over 5 levels).

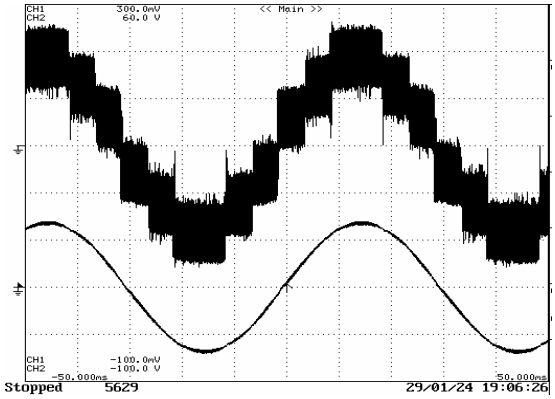


Fig. 12. Output phase voltage (over 9 levels) and current.

The instantaneous output phase voltage is shown in Figs. 11 and 12 with reference to a different modulation index *m*.
Fig. 11 is referred to the case of an output voltage vector rotating on a circle inside the inner hexagon. Note that the output phase voltage is distributed on the lower five levels only, since only the triangles in region ① are involved.
Fig. 12 shows both the voltage (upper trace) and the phase current (lower trace) referred to an output voltage vector rotating on a circle outside the inner hexagon. In this case all the nine voltage levels are involved. The resulting sinusoidal waveform of the phase current proves the effectiveness of the multilevel modulation algorithm.

8. Conclusion

An experimental investigation of a multilevel converter topology consisting of two insulated dc supplies and a dual two-level inverter feeding three-phase six-wires loads has been presented in this paper. The feasibility and effectiveness of both the power and the control schemes have been verified by numerical simulations and a complete set of experimental tests.

In particular, it has been shown that correct multilevel operations with balanced and unbalanced powers between the two inverters are always achievable within a predictable power ratio.

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