Double Inverter as a Multilevel Converter: Circuit Topology, Modulation Strategies and Applications

Gabriele Grandi, *Member*, *IEEE*, Claudio Rossi, Alberto Lega, and Domenico Casadei, *Senior Member*, *IEEE*

***Abstract*— A way to achieve a multilevel converter using two standard three-phase two-level inverters is presented in this paper. In order to obtain the typical multilevel voltage waveforms it is necessary to synchronize the commutations of the two inverters by a proper modulation strategy. Two modulation strategies are presented: the first one allows only generating the characteristic multilevel line-to-line voltages; the second one allows controlling the power flows from the two inverters too. The proposed converter topology can be applied in the automotive and naval fields.**

Index Terms— **Converters, Multilevel systems. Road vehicle propulsion.**

I. Introduction

MULTILEVEL converters have been introduced in high-power applications such as utility and large motor drive systems. The desired output voltage waveform is synthesized from the multiple voltage levels with lower distortion, lower switching frequency, higher efficiency, and lower voltage device ratings. There are three major multilevel topologies: cascaded, diode clamped, and capacitor clamped [1]. Usually, all these topologies require more complex power circuitry and more complex modulation strategies with respect to traditional three-phase inverters.

Multilevel inverters were initially proposed for high voltage applications to lower the voltage rating of the power switches in order to design feasible converters. Nowadays, many multilevel applications can be found in low voltage systems, in the place of standard three-phase inverters, with the aim of reducing waveform distortions and costs. As in example, in battery powered electric vehicles the standard solution for the traction system is given by a two-level inverter feeding a three phase motor. The inverter is supplied by a bank of standard lead acid batteries, often at very low voltage (<100V). With this solution the practical feasibility of a high power ac drive (>20 kW) is limited mainly by the high cost of the semiconductor power switches of the inverter due to the resulting high current rating.

The high cost together with the circuit complexity due to the parallel connection of the power switches can prevent the realization of standard three-phase drives for the traction system of heavy electric vehicles, such as buses, industrial truck, etc…

A viable solution introduced to overcome this problem is given by the use of a six-phase machine supplied by a six-phase inverter [2]-[5]. This solution allows sizing the power switches at half the rated current of an equivalent three-phase scheme, but requires the realization of a six-phase machine.

Another solution for high power electrical drives is the use of a multilevel inverter, which can be realized with semiconductor devices having lower voltage rating. The typical structure of such a system was introduced in [6] and, nowadays, it is widely used to drive three-phase electrical machine with high supply voltages. Several topologies of multilevel converters have been also presented for low voltage applications [7]. Among these, the cascaded converter can be conveniently used with a battery supply system, because it is relatively easy to split the supply in several electrically separated sources.

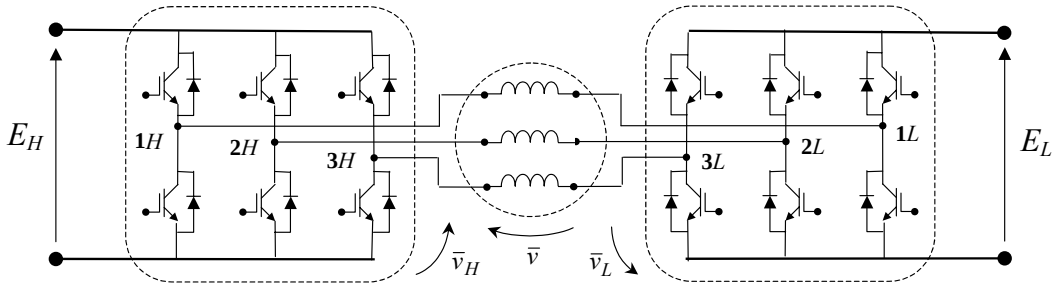


Fig.1: Multilevel converter for six-wire applications composed of two traditional two-level inverters.

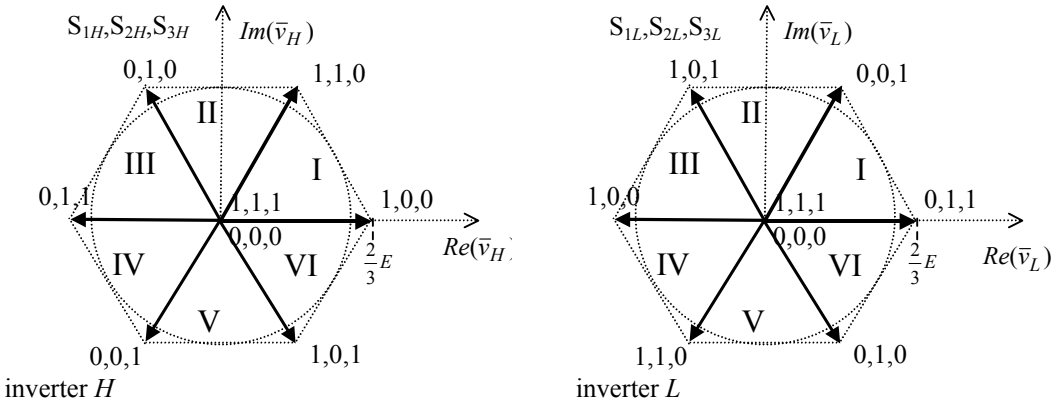


Fig.2: Switch configurations, sectors, and corresponding voltage vectors for inverters *H* and *L*.

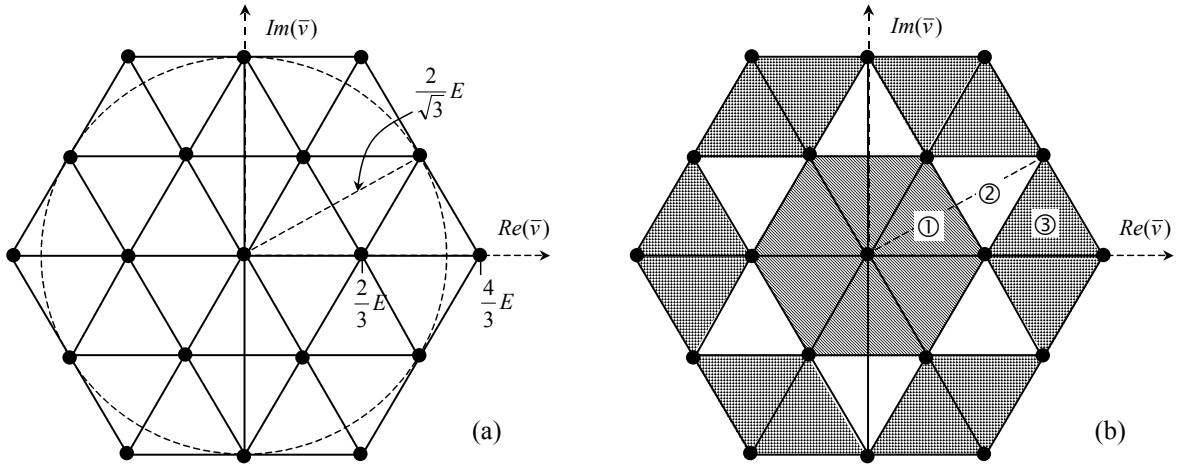


Fig. 3: (a) Output voltage vectors generated by the dual, two-level inverter. (b) Highlight of the triangles in the three different regions ①, ②, and ③.

In this paper a multilevel converter composed of a dual two-level inverter feeding open-end, three-phase ac motor [8]-[10] is considered. The scheme of the multilevel converter is shown in Fig.1. This scheme is based on the use of two insulated supplies, each one feeding a standard, three-phase two-level inverter. A three-phase, six-wires load is connected across the six output terminals of the inverters. The two separate dc sources can be easily obtained on board of an electric vehicle by splitting the batteries in two separate banks.

This solution should be preferred to other multilevel configurations because of some advantages: no generation of common mode (zero sequence) currents on the motor winding, best dc bus voltage utilization, use of two standard three-phase, two-level inverters.

New switching techniques, based on a proper application of the space vector modulation (SVM), are presented in the paper. The main feature of these techniques is the capability to regulate the load power sharing between the two dc sources. This means that it is possible to balance exactly the power flow from the two sources, or to unbalance the power flow in order to restore the same state of charge of two battery banks.

Furthermore, the dual inverter topology is a high reliability solution. In case of fault in one inverter, it must be short-circuited at the output terminals, and the drive can be operated using the other one as a standard three-phase two-level inverter. This possibility allows the operation of the motor at the rated current (that means rated torque) up to the half of the rated voltage (that means half of the rated speed).

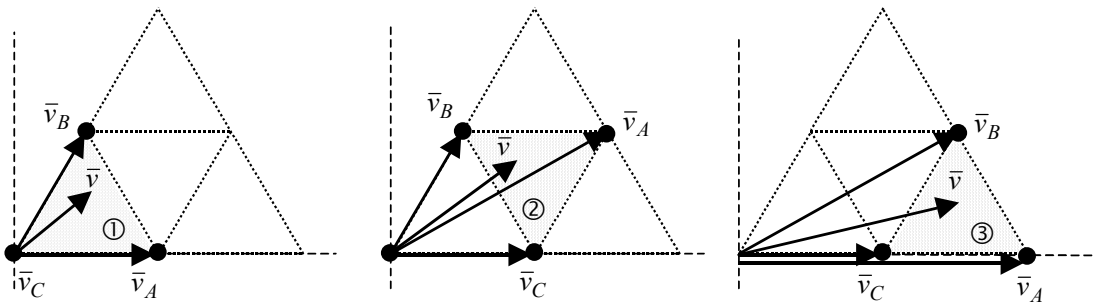


Fig.4: Voltage vectors used for generating the output voltage in the three regions.

II. MULTILEVEL MODULATION STRATEGY

With reference to the scheme of Fig. 1, using space vector representation, the output voltage vector $\bar{v}$ is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter H and inverter L, respectively,

$$\bar{v} = \bar{v}_H + \bar{v}_L \tag{1}$$

The voltages $\bar{v}_H$ and $\bar{v}_L$ can be expressed on the basis of the dc-link voltages and the switch states of the inverter legs. Assuming $E_H = E_L = E$ leads to

$$\bar{v}_H = \frac{2}{3}E\left(S_{1H} + S_{2H}\, e^{j\frac{2}{3}\pi} + S_{3H}\, e^{j\frac{4}{3}\pi}\right)$$
$$\bar{v}_L = -\frac{2}{3}E\left(S_{1L} + S_{2L}\, e^{j\frac{2}{3}\pi} + S_{3L}\, e^{j\frac{4}{3}\pi}\right) \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverters legs. A space vector representation of $\bar{v}_H$ and $\bar{v}_L$ is given in Fig. 2.

The combination of the eight switch configurations for each inverter yields 64 possible switches states for the whole multilevel converter, corresponding to 18 different output voltage vectors and a null vector, as represented in Fig. 3(a). By using the SVM technique, these voltage vectors can be combined to obtain any output voltage vector lying inside the outer hexagon, having a side of 4/3 E. In particular, with reference to sinusoidal steady state, the maximum magnitude of the output voltage vector is $2E/\sqrt{3}$ (i.e., the radius of the inscribed circle).

The outer hexagon is composed by 24 identical triangles. For symmetry reasons, only three different regions can be identified. As shown in Fig. 3(b), there are 6 inner triangles (region ① - dashed), 6 intermediate triangles (region ② - white), and 12 outer triangles (region ③ - dotted).

In a multilevel inverter the output voltage vector is synthesized by modulating three adjacent vectors corresponding to the vertices of the triangle where the output voltage vector lies. It means that, in each region and within each switching period, $\bar{v}$ is synthesized by using the vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, as represented in Fig. 4 for the three types of triangles.

Considering the standard SVM technique, $\bar{v}$ is obtained as

$$\bar{v} = \mu\,\bar{v}_A + \lambda\,\bar{v}_B + \gamma\,\bar{v}_C, \tag{3}$$

where the duty cycle μ, λ, γ can be determined as

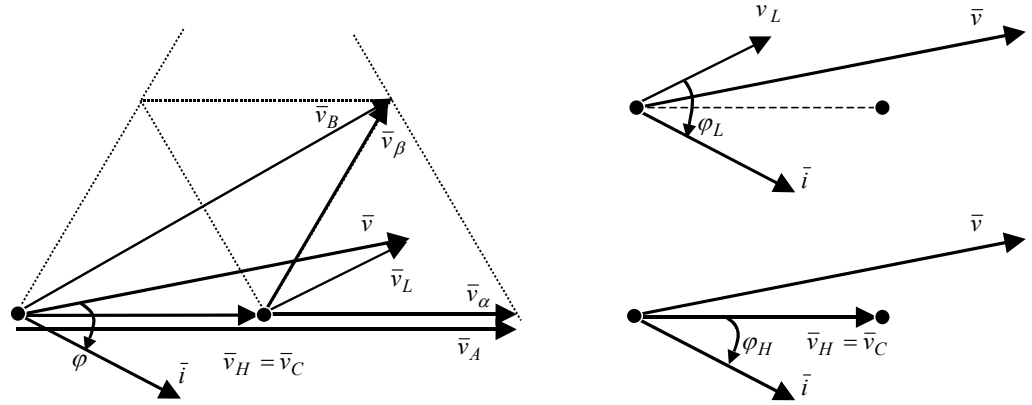


Fig.5: Vector composition of the output voltage combining six-step mode and SVM mode for the two inverters.

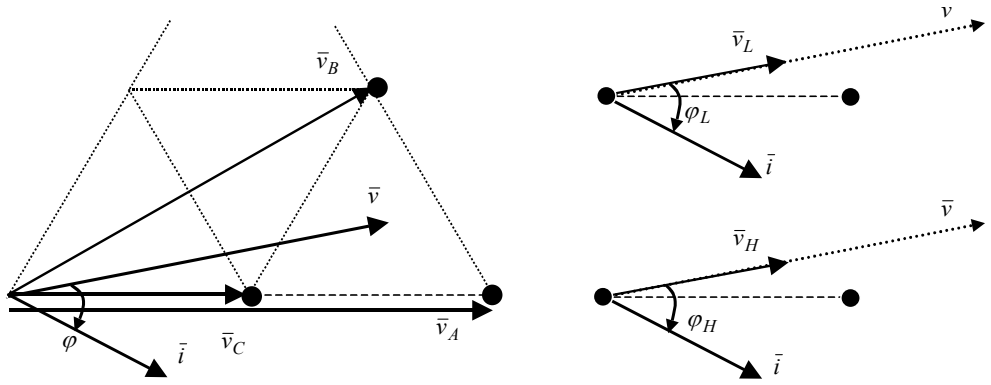


Fig.6: Vector composition of the output voltage with balanced power between the inverters ($k = 0.5$).

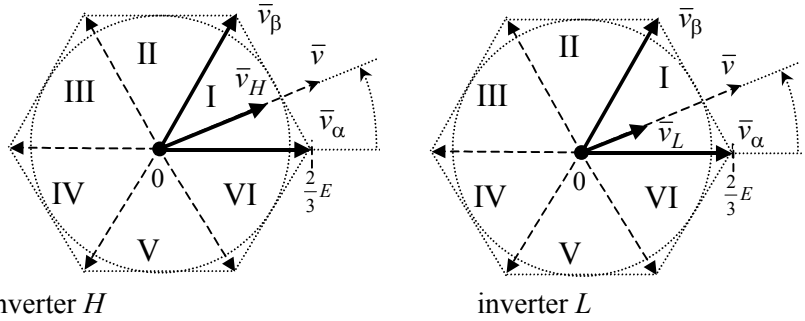


Fig.7: Voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by using the same two adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$.

$$\begin{cases} \mu = \dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \\ \lambda = -\dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_A-\bar{v}_C)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \\ \gamma = 1-(\mu+\lambda) = 1-\dfrac{(\bar{v}-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_A)}{(\bar{v}_A-\bar{v}_C)\cdot j(\bar{v}_B-\bar{v}_C)} \end{cases} . \quad (4)$$

A simple modulation strategy consists of modulating one inverter in the six-step mode, i.e., $\bar{v}_H = \bar{v}_C$, and the other inverter in the SVM mode for generating the residual output voltage $\bar{v}_L = \bar{v} - \bar{v}_C$. As an example, Fig. 5 shows the vector composition considering $\bar{v}$ laying in the outer triangle (region ③).

This simple modulation technique leads to a power unbalance between the two inverters. In fact, the inverter voltages ($\bar{v}_H, \bar{v}_L$) have different magnitude and different phase angle with respect to the output current $\bar{i}$ (the same for both), as shown in Fig. 5.

The problem of balancing the power between the two dc sources could be solved in a simple way, by exchanging the role of the inverter operating in the six-step mode with the one operating in the SVM mode. The commutation can be actuated during a switching period, a triangle change, or a fundamental period. This solution is satisfactory for exactly balancing the powers, but does not allow any different regulation of the power sharing.

III. Regulation of the Power Sharing

A novel modulation technique, able to regulate the power sharing between the two dc sources, is presented in this section. The balanced operation can be considered a particular case.

Introducing the power ratio k, the output power p (average value over a switching period) can be shared between the dc sources (H and L) according to

$$p = \frac{3}{2}\bar{v}\cdot\bar{i} = p_H + p_L$$
$$\Downarrow \quad (5)$$
$$\begin{cases} p_H = \dfrac{3}{2}\bar{v}_H\cdot\bar{i} = k\cdot p \\ p_L = \dfrac{3}{2}\bar{v}_L\cdot\bar{i} = (1-k)\cdot p \end{cases}$$

Assuming the inverter voltage vectors $\bar{v}_H$, $\bar{v}_L$ in phase with the output voltage vector $\bar{v}$, (5) leads to

$$\begin{cases} \bar{v}_H = k\,\bar{v} \\ \bar{v}_L = (1-k)\bar{v} \end{cases} . \quad (6)$$

Fig. 6 shows the particular case with k = 0.5 corresponding

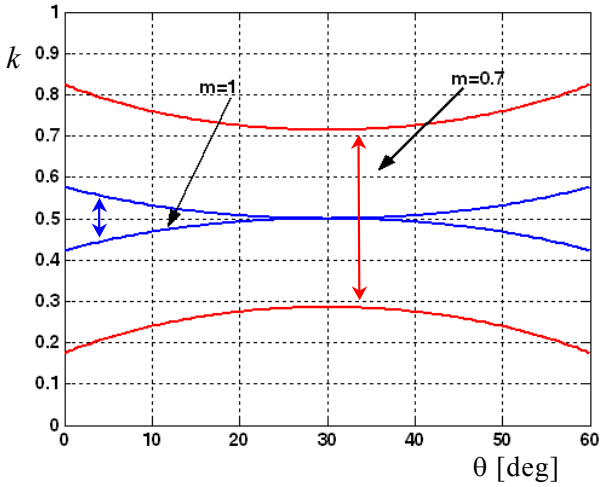


Fig. 8: Possible values of the power ratio k for modulation indexes m = 1 (blu) and m = 0.7 (red).

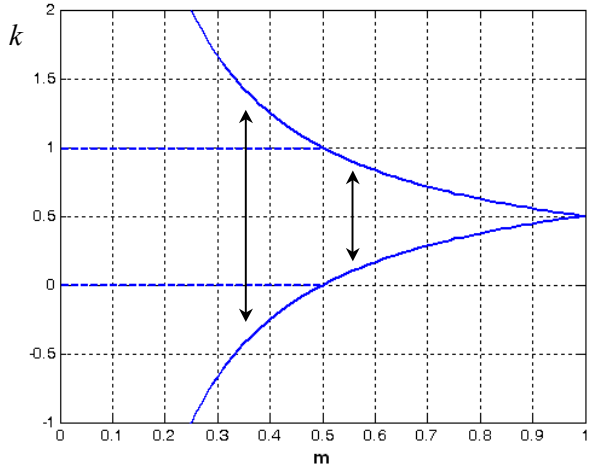


Fig. 9: Limits of the power ratio k as function of the modulation index m.

to $\bar{v}_H = \bar{v}_L = 1/2\,\bar{v}$, i.e., balanced power for the dc sources. In order to synthesize an output vector $\bar{v}$, the two inverters must generate the corresponding fraction of $\bar{v}$ by applying only their active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector. Being $\bar{v}_H$ and $\bar{v}_L$ in phase, they lay in the same sector and can be synthesized using the same adjacent active vectors $\bar{v}_\alpha, \bar{v}_\beta$, as shown in Fig. 7.

The duty cycles $\mu_H, \lambda_H, \gamma_H$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *H*. The duty cycles, $\mu_L, \lambda_L, \gamma_L$, represent the application time of active vectors $\bar{v}_\alpha, \bar{v}_\beta$ and null vector, respectively, for inverter *L*. In this way, the voltage generated by the two inverters are

$$\begin{cases} \bar{v}_H = \mu_H\,\bar{v}_\alpha + \lambda_H\,\bar{v}_\beta \\ \bar{v}_L = \mu_L\,\bar{v}_\alpha + \lambda_L\,\bar{v}_\beta \end{cases}. \tag{7}$$

By using standard SVM equations, the duty-cycles of inverters *H* and *L* are given by

$$\begin{cases} \mu_H = \dfrac{\bar{v}_H \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_H = -\dfrac{\bar{v}_H \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \gamma_H = 1-(\mu_H+\lambda_H) = 1-\dfrac{\bar{v}_H \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \end{cases}$$

and

$$\begin{cases} \mu_L = \dfrac{\bar{v}_L \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \lambda_L = -\dfrac{\bar{v}_L \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \\ \gamma_L = 1-(\mu_L+\lambda_L) = 1-\dfrac{\bar{v}_L \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \end{cases}. \tag{8}$$

IV. Determination of the Operating Limits

The constrains of the duty-cycles expressed by (8) are

$$\begin{cases} \mu_H \ge 0 \\ \lambda_H \ge 0 \\ \mu_H + \lambda_H \le 1 \end{cases} \quad \text{and} \quad \begin{cases} \mu_L \ge 0 \\ \lambda_L \ge 0 \\ \mu_L + \lambda_L \le 1 \end{cases}. \tag{9}$$

These constrains introduce a limit in the range of variation of the power ratio *k*. In particular, the range of variation of *k* can be evaluated as a function of the desired output vector $\bar{v}$. Introducing in (9) the expressions (8) of duty cycles, and representing $\bar{v}_H$ and $\bar{v}_L$ in terms of *k* by (6), leads to

$$\begin{cases} \dfrac{k\bar{v} \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \ge 0 \\ -\dfrac{k\bar{v} \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \ge 0 \\ \dfrac{k\bar{v} \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \le 1 \end{cases}$$

and

$$\begin{cases} \dfrac{(1\text{-}k)\bar{v} \cdot j\bar{v}_\beta}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \ge 0 \\ -\dfrac{(1\text{-}k)\bar{v} \cdot j\bar{v}_\alpha}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \ge 0 \\ \dfrac{(1\text{-}k)\bar{v} \cdot j(\bar{v}_\beta - \bar{v}_\alpha)}{\bar{v}_\alpha \cdot j\bar{v}_\beta} \le 1 \end{cases}. \tag{10}$$

The solution of (10) can be found in each one of the six sectors where $\bar{v}_H$ and $\bar{v}_L$ can be located.

If the output voltage vector is written as $\bar{v} = Ve^{j\vartheta}$, the modulation index *m* can be defined as

$$m = \frac{V}{\frac{2}{\sqrt{3}}E},\ 0 \le m \le 1 \text{ for sinusoidal output voltages.} \tag{11}$$

Then, with reference to sector I ($0 \le \vartheta \le \dfrac{\pi}{3}$), the solution of (10) is given by

$$\begin{cases} k \le \dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \\ k \ge 1-\dfrac{1}{2m}\dfrac{1}{cos(\pi/6-\vartheta)} \end{cases}$$

$$\Downarrow \tag{12}$$

$$\frac{1}{2} - a \le k \le \frac{1}{2} + a$$

being $a = \dfrac{1-m\,cos(\pi/6-\vartheta)}{2m\,cos(\pi/6-\vartheta)}$.

Eq. 12 gives the possible values of *k* as a function of the modulation index *m* and the output voltage phase angle ϑ. It can be noted that for any modulation index, the most stringent condition for *k* is given in the middle of the sector, i.e. for $\vartheta = \pi/6$. Fig. 8 represents the boundaries of *k* as a function of the phase angle ϑ for $m = 1$ and $m = 2/3$.

Similar considerations can be made for the other sectors (II ÷ VI).

In most applications is required to share the output power between the dc sources in equal parts. This means that *k* must be fixed to 0.5 during the whole fundamental period, $0 \le \vartheta \le 2\pi$.

If the maximum output voltage is required ($m = 1$), there is no possibility to regulate the power sharing between the dc sources. In this case only the value $k = 0.5$ is admissible, as

Table I: Resulting switching sequence for multilevel operations

	region ①					region ②						region ③				
output vectors	$\bar{v}_A=\bar{v}_\alpha$		$\bar{v}_B=\bar{v}_\beta$		$\bar{v}_C=0$	$\bar{v}_A=\bar{v}_\alpha+\bar{v}_\beta$		$\bar{v}_B=\bar{v}_\beta$		$\bar{v}_C=\bar{v}_\alpha$		$\bar{v}_A=2\bar{v}_\alpha$	$\bar{v}_B=\bar{v}_\alpha+\bar{v}_\beta$		$\bar{v}_C=0$	
$\bar{v}_H$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0
$\bar{v}_L$	0	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	0	$\bar{v}_\alpha$
duty cycles	μ’	μ”	λ’	λ”	γ	μ’	μ”	λ’	λ”	γ’	γ”	μ	λ’	λ”	γ’	γ”

Table II: Switching sequence corresponding to three-steps operation for each inverter

	region ①					region ②						region ③				
H duty cycles	γ_H			μ_H	λ_H	μ_H		γ_H		λ_H		μ_H			λ_H	γ_H
$\bar{v}_H$	0			$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$		0		$\bar{v}_\beta$		$\bar{v}_\alpha$			$\bar{v}_\beta$	0
output vectors	$\bar{v}_\alpha$	$\bar{v}_\beta$	0	$\bar{v}_\alpha$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\beta$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$	$2\bar{v}_\alpha$	$\bar{v}_\alpha+\bar{v}_\beta$	$\bar{v}_\alpha$
$\bar{v}_L$	$\bar{v}_\alpha$	$\bar{v}_\beta$	0			0	$\bar{v}_\beta$		$\bar{v}_\alpha$		0	$\bar{v}_\beta$	0	$\bar{v}_\alpha$		
L duty cycles	μ_L	λ_L	γ_L			←γ_L	λ_L		μ_L		γ_L→	λ_L	γ_L	μ_L		
sub-int.	μ”	λ”	γ	μ’	λ’	γ’	μ’	λ”	γ”	μ”	λ’	λ’	γ’	μ	λ”	γ”

shown in Fig. 8.

For values of the modulation index lower than 1, the parameter k can be changed, under the limits imposed by (12). Fig. 9 shows the upper and lower limits of k with reference to sinusoidal output voltages as a function of the modulation index m. It can be noted that for $m < 0.5$ the power ratio k can be greater than unity and lower than zero. It means that an amount of power can be transferred from a dc source to the other, and the inverter voltages $\bar{v}_H$ and $\bar{v}_L$ become in phase oppositions, as shown by (5) and (6). This feature could be interesting when using rechargeable supplies, e.g. batteries, because it represents the possibility to transfer energy between the two sources. In this paper only the range $0 \le k \le 1$ is discussed.

For $m \le 0.5$ the output voltage vector lies within the circle of radius $E/\sqrt{3}$. In this case, the output power can be supplied by the two inverters with any ratio. In particular, if k is set to 0 all the load power is supplied by inverter L, whereas if k is set to 1 all the load power is supplied by inverter H. This is a very important feature of this converter in case of fault, because it represents the possibility to supply the load by using one inverter only.

V. Determination of the Switching Sequence

Once the limits for k has been defined, and the required inverter voltages $\bar{v}_H$ and $\bar{v}_L$ have been determined, the duty-cycles $\mu_H, \lambda_H, \gamma_H$ and $\mu_L, \lambda_L, \gamma_L$ can be calculated by (8). As stated above, for achieving a correct multilevel operation, the three vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$, adjacent to the desired output voltage vector $\bar{v}$, must be generated by properly combining active vectors ($\bar{v}_\alpha, \bar{v}_\beta$) and null vector of the two inverters. For regions ①, ②, and ③ shown in Figs. 3 and 4, three different vector compositions are defined, according to the following equations

$$\underline{\text{Region ①}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + 0 \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = 0 + 0 \end{cases} \quad \text{(a)} \qquad \underline{\text{Region ②}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_B = \bar{v}_\beta + 0 \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \quad \text{(b)} \qquad \underline{\text{Region ③}}\quad \begin{cases} \bar{v}_A = \bar{v}_\alpha + \bar{v}_\alpha \\ \bar{v}_B = \bar{v}_\alpha + \bar{v}_\beta \\ \bar{v}_C = \bar{v}_\alpha + 0 \end{cases} \quad \text{(c)} \tag{13}$$

On the basis of (13), the duty-cycles for the vectors $\bar{v}_\alpha, \bar{v}_\beta$ and 0 of inverters H and L, can be related to the duty-cycles μ, λ, γ of the output vectors $\bar{v}_A, \bar{v}_B, \bar{v}_C$ calculated in (4). It can be noted that $\bar{v}_\alpha, \bar{v}_\beta$ and 0 are the same vectors for the two inverters. Then, when the output vector $\bar{v}_\alpha$ must be applied, the application time of $\bar{v}_\alpha$ can be subdivided in two sub-intervals. In the first time interval, inverter H generates $\bar{v}_\alpha$ and inverter L generates 0. In the second time interval, inverter L generates $\bar{v}_\alpha$ and inverter H generates 0. The same procedures can be adopted for generating the output vectors $\bar{v}_\beta$ and $\bar{v}_\alpha + \bar{v}_\beta$. For the other possible output vectors, $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and 0, the subdivision is trivial. The resulting switching

sequence inside a switching period is represented in Tab. I with reference to all the three regions ①, ②, and ③.

The sub-intervals introduced in Tab. I can be determined for the three different regions on the basis of main duty-cycles μ,λ,γ and duty-cycles μ_H,λ_H,γ_H, μ_L,λ_L,γ_L of the two inverters, as follows

Region ① Region ② Region ③

$$\begin{cases} \mu' = \mu_H \\ \mu'' = \mu_L \\ \lambda' = \lambda_H \\ \lambda'' = \lambda_L \\ \gamma \ \text{is known} \\ - \end{cases} \quad \begin{cases} \mu'+\gamma' = \mu_H \\ \mu''+\lambda' = \lambda_H \\ \lambda''+\gamma'' = \gamma_H \\ \mu''+\gamma'' = \mu_L \\ \mu'+\lambda'' = \lambda_L \\ \lambda'+\gamma' = \gamma_L \end{cases} \quad \begin{cases} \mu \ \text{is known} \\ - \\ \lambda' = \lambda_L \\ \lambda'' = \lambda_H \\ \gamma' = \gamma_L \\ \gamma'' = \gamma_H \end{cases} \tag{14}$$

(a) (b) (c)

It can be noted that for regions ① and ③ the sub-intervals are five, whereas for region ② the sub-intervals are six and they can be determined by solving a system of six equations. Only five of these equations are linear independent. In fact, the sum of the first three equations in (14b) gives the same result than the sum of the last three equations, as expressed by (8). Then, the equation system (14b) can be solved in parametric form. Assuming γ' as parameter, the sub-intervals result

$$\begin{cases} \mu' = \mu_H - \gamma' \\ \mu'' = \lambda_H - \gamma_L + \gamma' \\ \lambda' = \gamma_L - \gamma' \\ \lambda'' = \lambda_L - \mu_H + \gamma' \\ \gamma'' = \mu_L + \gamma_L - \lambda_H - \gamma' \end{cases} . \tag{15}$$

Introducing the condition that all intervals must be not negative, $\mu',\mu'',\lambda',\lambda'',\gamma',\gamma'' \geq 0$, the admissible range of parameter γ' is determined. By choosing a value for γ' inside this range, the values of the other sub-intervals are determined by (15). In particular, it can be shown that, by selecting a proper value for γ', it is always possible to null one of the six sub-intervals. In this way the six-step commutation sequence collapses in five steps, as it happens in regions ① and ③.

Once all the sub-intervals are determined, they can be grouped in the switching sequence shown in Tab. II. In this way, for each inverter, a traditional three-step commutation within the switching period is obtained, involving active and null vectors $\bar{v}_\alpha, \bar{v}_\beta$, 0.

VI. Implementation of the Switching Sequence and Results

The proposed switching techniques have been numerically implemented in the Simulink environment of Matlab by using appropriate S-functions. In particular, the typical discretizations caused by a realistic digital control system have been taken into account. A simplified ideal model has been considered for power switches, without additional dead times. The tests have been carried out considering the same dc voltage for the dc sources: E = 100 V, and sinusoidal balanced reference output voltages (f = 50 Hz). In order to emphasize the switching actions, a large switching period has been adopted: TS = 500 μs (fS = 2 kHz).

The voltage waveforms generated by the two inverters are shown in Figs. 10 and 11, from top to bottom: (1) line-to-line voltage of inverter H (v_{12H}), (2) line-to-line voltage of inverter L (v_{12L}), and (3) load phase voltage (v1). The solid blue lines represent the instantaneous values, whereas the dotted green lines represent their moving average over a switching period.

It can be noted that the line-to-line voltages are distributed on three levels (0, ±E), as expected for traditional three-phase inverters, whereas the output phase voltage is distributed on nine levels (0, ±1/3E, ±2/3E, ±E, ±4/3E), as expected for a multilevel converter with 6 switches and according to

$$v_1 = \frac{v_{12H} - v_{31H}}{3} - \frac{v_{12L} - v_{31L}}{3} \tag{16}$$

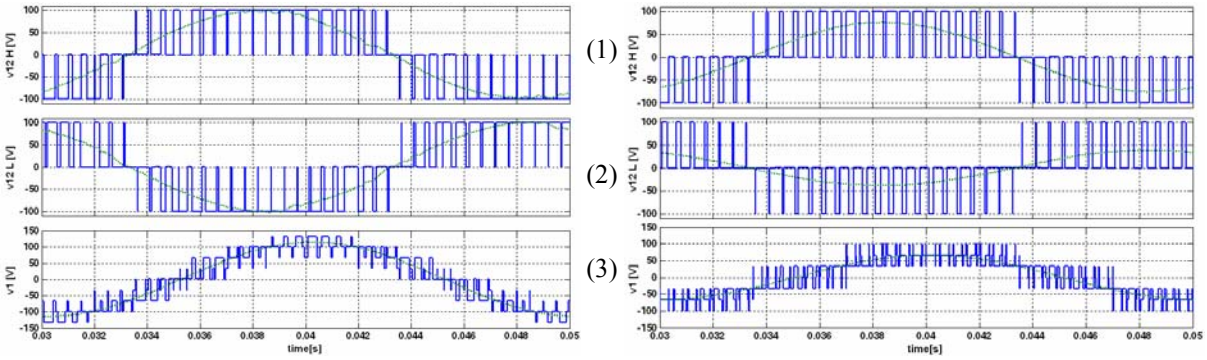
Fig. 10(a) corresponds to the maximum sinusoidal output voltage for the multilevel converter, m = 1 (v = 2/√3 E), and k = 1/2. In this case, the two inverters generate the same voltages and then supply the same power.

Fig. 10(b) shows the waveforms corresponding to a magnitude of the output voltage vector equal to the side of the inner hexagon, v = 2/3 E (m = 1/√3), and k = 2/3. In this case, the outer triangles (region ③) are not involved, and the output voltage is distributed on the lower seven levels only. Being k = 2/3, the voltages and the power generated by inverter H are double with respect to the ones generated by inverter L.

The effectiveness of the multilevel modulation is proved by observing that the output voltage is distributed in three levels within every switching period, corresponding to the three triangle vertices A, B, C of the vector diagram shown in Fig. 4.

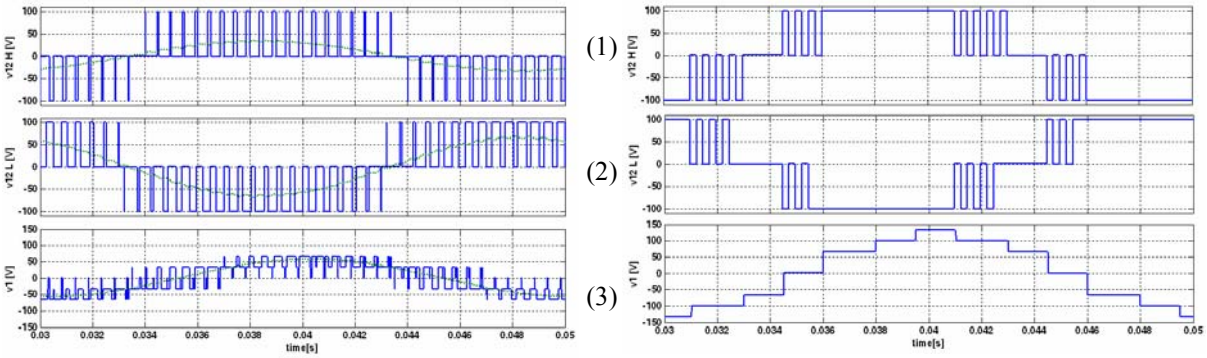
Fig. 11(a) shows the waveforms corresponding to the half of the maximum sinusoidal output voltage, v = 1/√3 E (m = 1/2), and k = 1/3. In this case, the locus of the output voltage vector is the circle inscribed in the inner hexagon. Then, the output voltage is distributed on the lower five levels since only the triangles in region ① are involved. Being the power ratio k = 1/3, the voltages and the power generated by inverter H are the half with respect to the ones generated by inverter L.

Fig. 11(b) shows the waveforms corresponding to the twelve-step behavior of the multilevel converter, with a power ratio k = 1/2. In this case, only the output main vectors $2\bar{v}_\alpha$, $2\bar{v}_\beta$, and $\bar{v}_\alpha + \bar{v}_\beta$ are involved; each vector is applied for a time interval equal to 1/12 of the fundamental period, and the output phase voltage is distributed on seven levels. In particular, the output vector $\bar{v}_\alpha + \bar{v}_\beta$ is obtained by combining $\bar{v}_\alpha, \bar{v}_\beta$ or $\bar{v}_\beta, \bar{v}_\alpha$, whereas the vectors $2\bar{v}_\alpha$ and $2\bar{v}_\beta$ correspond to the applications of $\bar{v}_\alpha$ and $\bar{v}_\beta$ for each inverter, respectively. In this way, the commutations of the inverters allow the power sharing within each switching period, while the output voltage behaves in the twelve-step mode.



(a) $\boldsymbol{m = 1}$ ($v = 2/\sqrt{3}\,E$), $\boldsymbol{k = 1/2}$ ($1–k = 1/2$) (b) $\boldsymbol{m = 1/\sqrt{3}}$ ($v = 2/3\,E$), $\boldsymbol{k = 2/3}$ ($1–k = 1/3$)

Fig. 10: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).



(a) $\boldsymbol{m = 1/2}$ ($v = 1/\sqrt{3}\,E$), $\boldsymbol{k = 1/3}$ ($1–k = 2/3$) (b) **twelve-step**, $\boldsymbol{k = 1/2}$ ($1–k = 1/2$)

Fig. 11: Voltage waveforms for different values of m and k:
1) line-to-line voltage generated by inverter H;
2) line-to-line voltage generated by inverter L;
3) load phase voltage (output).

VII. Applications

Multilevel inverters have many advantages with respect of standard three-phase converters, such as lower output THDs and the capability to handle higher voltages. Nevertheless, multilevel converters require a greater number of semiconductor devices and some constrains in the sources. Diode-clamped and flying-capacitors topologies require a subdivision of the dc bus to create the voltage levels; instead cascaded topologies need insulated sources. In some cases there is a natural agreement between the application and the multilevel converter (i.e. photovoltaic and cascaded converter). In automotive field, the energy source can be either a batteries bank or an endothermic engine or both (in hybrid vehicles). In these cases it is useful to employ the multilevel topology proposed in this paper because the necessary insulated dc sources are easy to obtain. In case of battery bank, it is simple to split it in two parts and using them to feed the two inverters. In this way it, is possible to employ the double inverter system easily and using it as a multilevel converter through one of the modulation described in this paper. Furthermore, an equal discharge of the two battery banks is achieved by a proper control of k index.

Similarly, another application for the proposed system is the propulsion in fishing-boat because these ships have two kind of cruising. When the nets are in the water, it is necessary to have high torque at low speed (higher power condition); when fishers need to move high speed and low torque are required (lower power condition). An endothermic engine with two electrical generators shrunk on can be employed to feed the two inverters. In higher power condition both the two inverters are fed and the converter is controlled by one of the multilevel modulation; in lower power condition only one inverter is fed and the other one has its outputs short-circuited [11].

VIII. Conclusion

The multilevel converter topology presented in this paper is composed by two standard three-level inverters widely commercialized. This means a lower cost than a diode-clamped or flying-capacitor equivalent solution. In case of fault, it is possible to short-circuit the outputs of the broken inverter so to create a star connection in the load and feed it

through the other inverter as a standard three-phase load. Furthermore, it is easiest to substitute the broken parts due to their high availability.

The two modulation strategies presented in the paper let the inverter system properly work: the voltage waveforms are those typical for multilevel inverters, as shown by simulation results. Moreover it is possible to regulate the power supplied from each of the two inverters, making the system suitable for battery applications. Some possible applications in the automotive and naval fields were presented.

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