# Carrier-Based Discontinuous Modulation for Dual Three-Phase Two-Level Inverters

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**Abstract–Dual two-level inverter topology is a simple structure able to produce multilevel output voltage waveforms equivalent to a 3-level inverter. Its modular structure consists of two standard two-level three-phase voltage source inverters (VSI) supplied by two dc supplies. In case of two separate dc supplies an independent modulation of the two inverters can provide arbitrary power sharing between inverters in order to balance their dc voltages. However, proper multilevel voltage waveforms can be obtained only by relatively complex space vector modulation (SVM). This paper proposes two carrier-based modulation techniques for a dual two-level inverter with power sharing capability and proper multilevel voltage waveforms. Their main advantage is a simpler implementation compared to SVM. The proposed algorithms have been verified by numerical tests and preliminary implementation in an industrial DSP.**

## I. INTRODUCTION

Nowadays, multilevel inverters became a standard solution in high-power high-voltage applications due to their advantages over "standard" two-level inverters, such as lower common-mode voltage, lower d$v$/d$t$ (lower leakage currents), lower harmonics in output current and reduced voltage on the power switches. Numerous three-level inverter topologies have been introduced in the last years, the most important of them being the diode clamped, the capacitor clamped, and the cascaded converter [1]. The dual inverter is a type of cascaded converter consisting of two standard two-level three-phase inverters connected to open-winding load, providing output voltages as a difference of corresponding leg potentials having up to nine levels.

The hardware simplification in this configuration is significant compared to its three-level inverter counterparts, due to use of readily available standard two-level inverters [2]. Example in Fig. 1 shows two identical two-level three-phase inverters forming a dual two-level inverter, although in general two inverters do not have to be equal with respect to type (voltage source/current source), number of levels, dc voltage value and voltage/current ratings [3]. The two main advantages of the dual inverter topology over the standard three-phase inverter are: using only half of the switching frequency and half of the dc voltage. On the other side the complexity of pulse-width modulation (PWM) algorithm is higher, due to the additional degree of freedom, as will be shown.

With reference to Fig. 1 it should be noted that it is possible to use only one dc-supply with mandatory elimination of zero-sequence current component either by hardware or software method. The first method requires a three-phase common mode reactor [4], whereas the second one applies particular modulation algorithms [5], [6]. The algorithm proposed in [5] had zero-sequence voltage equal to zero in every instant at the price of maximum output voltage restricted by 15 % and five-level voltage waveform (as a standard two-level inverter). Furthermore, there are simultaneous leg commutations in the switching pattern. More recently, a modulation nullifying the average of the zero-sequence voltage components within the switching period has been proposed [6]. Although the output voltage levels have been increased from five to seven, the other drawback remained. To conclude, the configuration where dc source can be easily split in two insulated parts (as for batteries or photovoltaic arrays) directly eliminates zero-sequence current and will be considered further on in the paper.

The quality of the output voltage is determined by the modulation algorithm and requires minimization of harmonic content, d$v$/d$t$ and number of switching commutations. If a proper multilevel voltage waveform is desired the switching configurations corresponding to the selected vectors cannot be applied in an arbitrary sequence, but generated by using the nearest three vectors approach (NTV) [7]. Furthermore, it must be taken into account that the PWM generation unit of industrial digital signal processors (DSPs) allows up to two commutations within the switching period for each inverter leg. Although converter can be modulated in closed loop mode [4], [8] here the focus will be on open-loop PWM control techniques impressing voltages to the ac side.

As for standard two-level inverters, the two basic modulation strategies for multilevel inverters are carrier-based modulation (CBM) and space vector modulation (SVM). The CBM scheme controls each phase leg separately by comparing phase reference waveforms against a triangular carrier, whereas the SVM schemes directly control the inverter voltages by explicitly selecting the nearest three voltage space vectors. In both cases duty cycles are calculated to achieve the same volt-second aver-

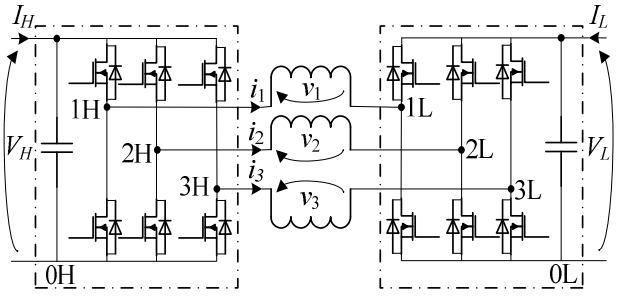


Fig. 1. Dual inverter with two separate dc supplies.

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age as the sampled reference voltage. A comprehensive SVM has been proposed in [2], however due to its complexity a carrier-based approach is proposed in this paper. Different modulation algorithms will be presented, from the simplest to the most effective, providing maximum modulation index and ability to perform multilevel operation and to regulate the load power sharing between the two dc sources. All of them can be implemented in industrial DSPs, avoiding additional logic circuitries such as field programming gate array (FPGA) for generating the firing signals for the power switches.

## II. Dual Inverter Modulation & Power Balancing

Using space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter is given by the sum of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$ generated by inverters *H* and *L*, respectively,

$$\bar{v} = \bar{v}_H + \bar{v}_L \tag{1}$$

as represented by the equivalent circuit of Fig. 2, being

$$\begin{cases} \bar{v}_H = \dfrac{2}{3} V_H \left( S_{1H} + S_{2H}\, e^{j2\pi/3} + S_{3H}\, e^{j4\pi/3} \right) \\ \bar{v}_L = -\dfrac{2}{3} V_L \left( S_{1L} + S_{2L}\, e^{j2\pi/3} + S_{3L}\, e^{j4\pi/3} \right) \end{cases} \tag{2}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverter legs. The combination of the eight switching configuration for each three-phase inverter yields to 64 possible switching states. If the two dc voltages are the same, i.e. $V_H = V_L = V_{dc}$, these switching states correspond to only 19 different output voltage vectors, including zero vector, as represented in Fig. 3. In this case, there are up to nine voltage levels: 0, $\pm 1/3 V_{dc}$, $\pm 2/3 V_{dc}$, $\pm V_{dc}$, $\pm 4/3 V_{dc}$. The redundancy of switching states represents a degree of freedom useful to develop different modulation strategies. An alternative solution is to consider different dc voltage levels having a prefixed ratio (e.g., 1:2 or 1:3), increasing the number of output voltage levels but losing the redundancy of switching states [3], [9]. Equal dc voltages, $V_{dc}$, are considered in this paper.

### A. Modulation

Assuming the nonexistence of the zero-sequence current (2) can be rewritten with reference two different arrangements for dual inverter [10]:

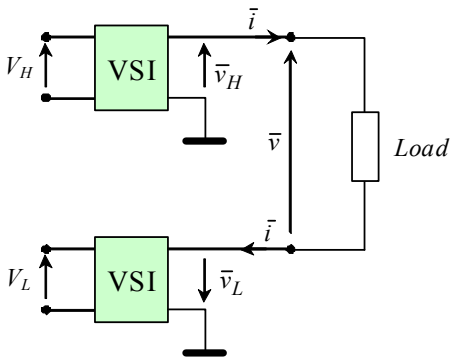


Fig. 3. Space vector equivalent circuit of the dual inverter.

- two separate three-phase inverters

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{1H} \\ v_{2H} \\ v_{3H} \end{bmatrix} - \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{1L} \\ v_{2L} \\ v_{3L} \end{bmatrix} \tag{3}$$

- three separate single-phase inverters

$$\begin{aligned} v_1 &= (2(v_{1H} - v_{1L}) - (v_{2H} - v_{2L}) - (v_{3H} - v_{3L}))/3\,, \\ v_2 &= (-(v_{1H} - v_{1L}) + 2(v_{2H} - v_{2L}) - (v_{3H} - v_{3L}))/3\,, \\ v_3 &= (-(v_{1H} - v_{1L}) - (v_{2H} - v_{2L}) + 2(v_{3H} - v_{3L}))/3\,. \end{aligned} \tag{4}$$

Expressions (3) and (4) are equivalent, only grouped in a different manner to emphasize the modulation approach. The modulations proposed in this paper are based on (3).

Due to the hexagon symmetry, the analysis can be restricted to one of the six big sectors (i.e., OAB in Fig. 3), similarly to the case of standard three-phase SVM algorithm. Using SVM principle (Fig. 4), references $\bar{v}_H^*$ and $\bar{v}_L^*$ can be generated by selecting adjacent vectors $\bar{v}_{aH}^*$, $\bar{v}_{bH}^*$, $\bar{v}_{oH}^*$ and $\bar{v}_{aL}^*$, $\bar{v}_{bL}^*$, $\bar{v}_{oL}^*$, respectively. The application times of active vectors can be calculated as:

$$\begin{cases} t_{aH} = \dfrac{3v_{\alpha H}^* - \sqrt{3} v_{\beta H}^*}{2V_{dc}} T_S\,, \\ t_{aL} = \dfrac{3v_{\alpha L}^* - \sqrt{3} v_{\beta L}^*}{2V_{dc}} T_S \end{cases} \tag{5}$$

$$t_{bH} = \frac{\sqrt{3} v_{\beta H}^*}{V_{dc}} T_S\,, \quad t_{bL} = \frac{\sqrt{3} v_{\beta L}^*}{V_{dc}} T_S \tag{6}$$

being $\bar{v}_H^* = v_{\alpha H}^* + j v_{\beta H}^*$, $\bar{v}_L^* = v_{\alpha L}^* + j v_{\beta L}^*$, and $T_S$ the switching period. The application times of null vectors are given by

$$t_{oH} = T_S - t_{aH} - t_{bH}\,, \quad t_{oL} = T_S - t_{aL} - t_{bL} \tag{7}$$

In order to determine the switching sequence, the big triangle OAB is divided in four identical equilateral triangles denoted OCD (inner), CDE (intermediate), ACE and BDE (outers), as shown in Fig. 3. The voltage reference vector $\bar{v}^*$ lays in one of these triangles, leading to four relevant cases [2]. Furthermore the hexagon is divided in six areas denoted "A" and "B" in Fig. 3. The position of

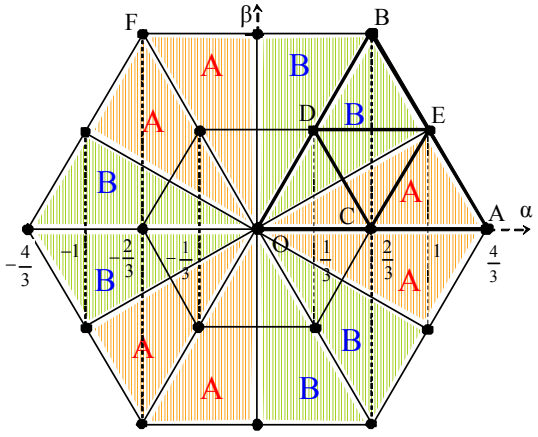


Fig. 2. Dual inverter voltage vector plot (p.u.) in the case $V_H = V_L = V_{dc}$ introducing six main sectors and their subsectors A, B.

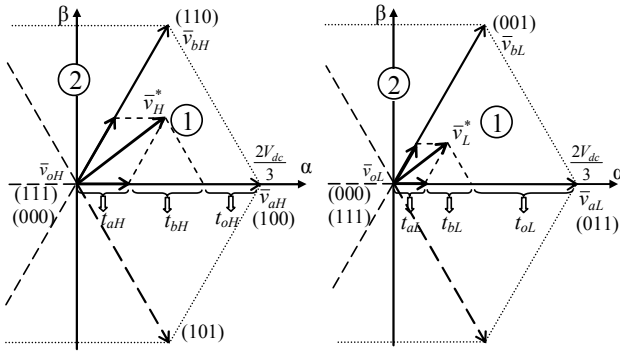


Fig. 4. Space vector composition of $\bar{v}_H^*$ and $\bar{v}_L^*$ by using the two adjacent active vectors for each inverter.

the reference vector inside A-half in the triangle OAB is determined by comparison of corresponding application times of the same inverter, e.g. inverter H:

$$t_a \geq t_b \tag{8}$$

where $t_a = t_{aH} + t_{aL}$, $t_b = t_{bH} + t_{bL}$, are total times of application for vectors "A" and "B". This is identical as for the standard two-level SVM and it rises from the fact that depending whether the sector is even or odd application vectors $\bar{v}_{aH}$ and $\bar{v}_{bH}$ alternatively swap places, and will be used in the following modulation algorithms.

### *B. Power Balancing*

The multilevel inverter structure presents the problem of balancing the power from the two dc voltage supplies [2]. Introducing the voltage ratio $k$ of the dual inverter and imposing the inverter voltage vectors $\bar{v}_H^*$ and $\bar{v}_L^*$ to be in phase with the reference output voltage $\bar{v}^*$, yields

$$\begin{cases} \bar{v}_H^* = k\,\bar{v}^* \\ \bar{v}_L^* = (1-k)\,\bar{v}^* \end{cases}. \tag{9}$$

Being the output ac current of the two inverters the same, the coefficient $k$ also defines the power sharing between the two inverters:

$$\begin{cases} p_H = \dfrac{3}{2}\bar{v}_H \cdot \bar{i} = k\,p \\ p_L = \dfrac{3}{2}\bar{v}_L \cdot \bar{i} = (1-k)\,p \end{cases}. \tag{10}$$

Therefore choice of the two voltage references $\bar{v}_H^*$ and $\bar{v}_L^*$ will determine the power converted by the two inverters. For example [11] proposed that one inverter provides only active power while the reactive power is provided by the other inverter. However in order to maximize output voltage the voltage references $\bar{v}_H^*$ and $\bar{v}_L^*$ need to be collinear as in (9).

During the modulation instantaneous powers differ since the two inverter's discrete vectors are different. However the power balancing can be achieved by taking into account average power over an interval of time. Since voltages are in general different due to the modulation, (10) yields that powers supplied by the inverters will be also different. As averaging interval could be chosen the switching period $T_s$, or larger periods such is the one corresponding to a sextant (60°) [6]. In this paper, the switching period has been chosen as the time interval in which the average inverters powers are shared according to (9) and (10).

## III. Independent Modulation

The application of two equal but independent (separated) modulators to the two single inverters is characterized by simplicity and large degree of freedom. Using (3) output voltage of the dual inverter can be obtained as difference of phase-to-neutral voltages separately produced by two inverters, as illustrated in Fig. 2. The two inverters can be modulated by any known modulation techniques, e.g. popular continuous SVM with centered active vectors and symmetrical placement of zero vectors [7]. However, in general it fails to produce proper multilevel waveform and, consequently, the output voltage includes higher harmonic distortion and increased d$v$/d$t$. The voltage references can be given independently regarding both amplitude (within available dc voltage limits) and phase. This approach has been proposed for automotive applications [11], [12].

### *A. Continuous Modulation*

Applying the most popular method of continuous modulation with symmetrical placement of zero vectors the disadvantage is improper multilevel waveform of output voltage $v_1$ (denoted in Fig. 1). Due to the presence of zero vectors both at the beginning and middle of the sequence two double simultaneous commutations are present, and vector $\bar{v}_O$ is created even for outer triangles, as can be seen in Fig. 5(a). In addition, the big vectors such are $\bar{v}_E$ and $\bar{v}_A$ (or $\bar{v}_B$, depending on A/B-half) are generated when $\bar{v}^*$ is inside the inner triangle OCD. Therefore application of this modulation gives inappropriate multilevel modulation waveforms and, in addition, two double commutations in each switching period. It can be easily seen from Fig. 5(b) that the voltage waveform ($v_1$ in Fig. 1 for the modulation index $m$ = 0.75, $V_{dc}$ = 30 V) shows very large voltage excursion, from 0 to maximum levels (up to $\pm 4/3 V_{dc}$).

### *B. Discontinuous Modulation*

An improvement is application of discontinuous modulation for each inverter since it does not contain both zero vectors within switching period. In particular the proper application of discontinuous 60º modulation with clamp at voltage peaks [7] eliminates completely big vectors for the inner triangle. Modulating signals expressed in relative units are given by:

$$\begin{aligned} (m_H) &= (1, 1 - m\cos(\theta + \pi/6), 1 - m\cos(\theta - \pi/6)), \\ (m_L) &= (0, m\cos(\theta + \pi/6), m\cos(\theta - \pi/6)), \end{aligned} \tag{11}$$

where signals for the L-inverter are obtained from H-inverter by subtraction from the maximum value to produce opposite output voltage. It can be noted that division to sectors A and B (Fig. 3) illustrates the discontinuous modulation (one leg is fixed during each A/B sector). In

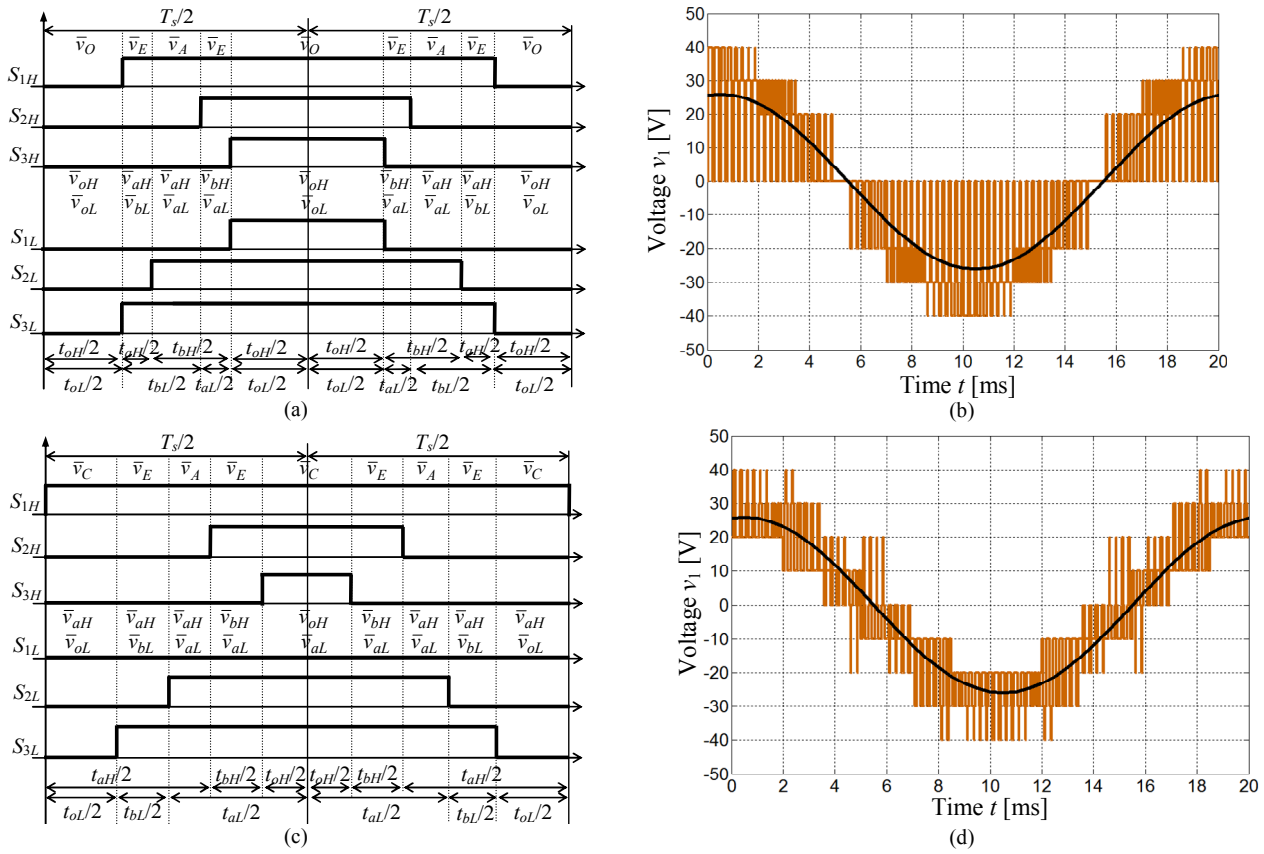


Fig. 5. Switching pattern (triangle ACE) and voltage ($m = 0.75$, $f_s = 2$ kHz) for independent modulation: (a), (b) continuous. (c), (d) discontinuous.

order to balance on- and off-time of the switches division in half-sectors provides possibility to have both always-on and always-off leg in each sector. Each inverter has six switches with two states each gives exact number of twelve different "half-sectors". Example of the switching patterns in A-half is given in Fig. 5(c), where can be seen that the starting vector corresponds to the name of the half-sector. The resulting output voltage is presented in Fig. 5(d). Although the voltage waveform does not show an ideal multilevel shape, a relevant improvement is obtained with respect to the previous method, Fig. 5(b). The problem arises in the intermediate triangles (CDE), as explained in more details in [2].

## IV. Composition of Switching Periods

The complexity of the dual inverter modulation can be considerably simplified considering the space vector hexagon composed of six "basic" hexagons, as shown in Fig. 6. The origins of each of these hexagons (such as AEDORT) are located in the apexes of the inner hexagon CDGJMR. Thus each of these basic hexagons is shifted with respect to the origin O by the vector with amplitude $2/3V_{dc}$. The modulation is simply referred to single inverter case by fixing one inverter vector for whole switching period instead of modulating it [5]-[7]. This principle is used in different manner for asymmetrical dual inverter where the inverter with higher ratings remains in this six-step mode [3]. However for the sake of symmetry here two equal inverters swap roles as analyzed in Section II.*B* after

1) each switching period,
2) one sixth of the output cycle,

since they cannot have instantaneously equal voltages. The modulation with the first approach [5] suffers the problem of simultaneous commutations due to the swap which cannot be avoided. As a solution, in [6] is proposed to use the second approach avoiding so many simultaneous commutations, but asymmetry of powers remains for longer period slowing the fast response. However, a different way to solve this problem is presented here in two steps, based on the combination of two consecutive switching periods and discontinuous modulation.

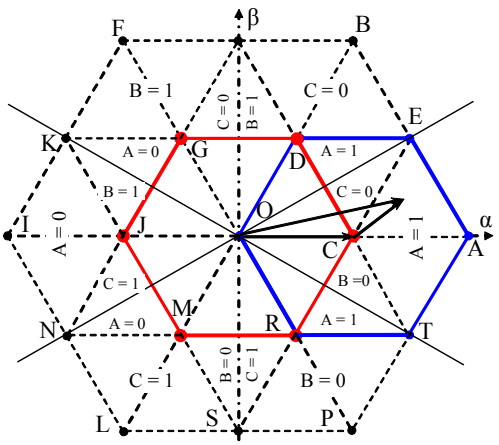


Fig. 6. Composition modulation principle based on six basic hexagons.

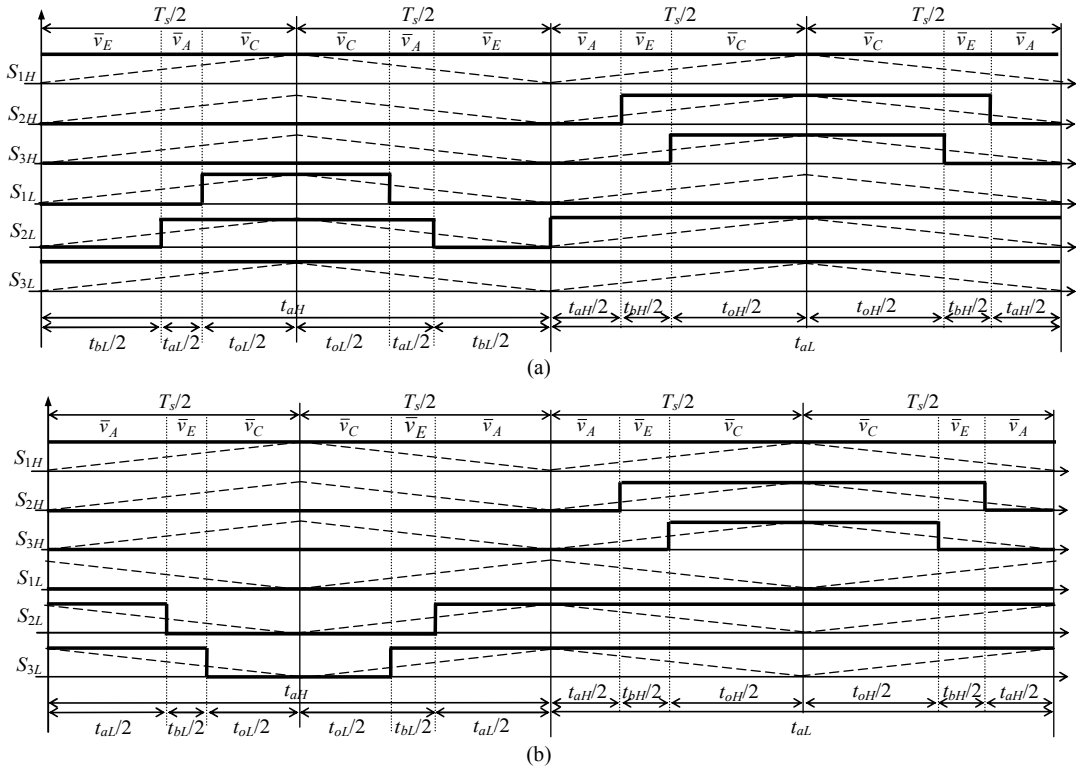


Fig. 9. Decomposition modulation patterns for basic (a) and improved (b) combinations of two switching periods (outer triangle ACE, $m = 0.75$).

### *A. Basic Combination of Two Switching Periods*

Considering big triangle OET with the representative inner, intermediate and outer triangles, as depicted in Fig. 6, the discontinuous modulation will be applied also here. The switching pattern during one switching period for $\bar{v}^*$ inside the inner triangle OCD is the simplest case, having one inverter always fixed to zero vector and therefore without commutations/pulses. For the outer triangle ACE the switching pattern is illustrated in Fig. 9(a). It can be noted that pattern contains two pulses for some legs, and no simultaneous commutations. The most complex case is again the intermediate triangle CDE. Now it is considered divided by OE in two rectangular triangles.

### *B. Improved Combination of Two Switching Periods*

The basic modulation can be improved as shown in Fig. 9(b) providing asymmetrical switching pattern with only one pulse within switching period. The discontinuous modulation [7] is applied with the choice of the non-modulating legs for inverter H shown in Fig. 6, whereas for the inverter L the values are simply inverted. The most complex case of the intermediate triangle CDE, requires introduction of the subsectors A and B (see Fig. 3), with different non-modulating legs to avoid additional commutation within period. In this way the switching frequency is reduced to half with the same multilevel output waveform shown in Fig. 7.

The power sharing can be implemented by realization of two collinear but different vectors inside switching period, as shown in Fig. 8

$$\bar{v}^* = (\bar{v}_1^* + \bar{v}_2^*)/2\,, \tag{12}$$

with the ratio $v_1/v_2$ of their magnitudes determined by (9). However close to the borders of the triangles two references $\bar{v}_1{}^*$ and $\bar{v}_2{}^*$ will produce different voltage levels (e.g. when $\bar{v}_1{}^*$ is in ACE and $\bar{v}_2{}^*$ in CDE).

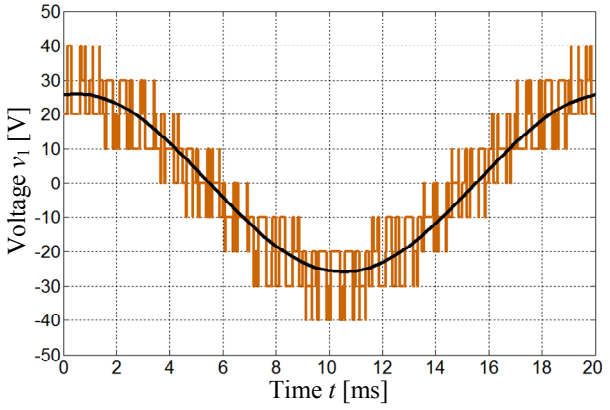


Fig. 7. Output voltage $v_1$ for the decomposition modulation ($m = 0.75$, $V_{dc} = 30$ V, $f_s = 2$ kHz)

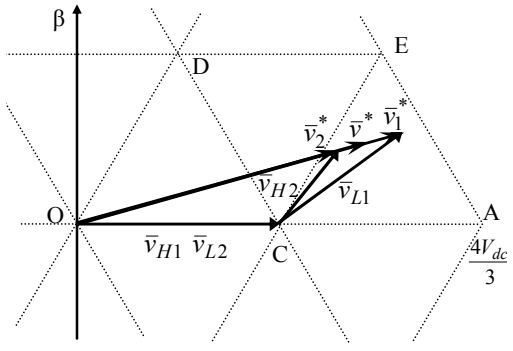


Fig. 8. The power sharing principle for decomposition modulation.

## V. Implementation and Preliminary Results

The dual inverter has been modeled in simulation and then realized as prototype with two separated dc sources used as power supplies, providing the voltage $V_{dc}$ = 30 V. A DSP TMS320F2812 has been used to control all six legs of the dual inverter. Due to high working frequency (150 MHz) it allows the switching frequencies around 20 kHz. Both numerical and experimental tests are referred to the same modulating algorithms. The same numerical results are already given in Fig. 5 and Fig. 7.

Corresponding to the case examined in Section III, Fig. 10 shows experimental voltage waveform for the independent modulation with symmetrical zero vector (a) and discontinuous modulation (b). The upper half of the figure shows a period (20 ms) of the output voltage corresponding to Fig. 5(b) and (d). Additionally, all six PWM signals A0-A5 denote PWM signals for legs H1-H3 and L1-L3, respectively, have been captured using 8-channel digital probe. The zoomed switching period on the lower half shows switching pattern corresponding to Fig. 5(a) and (c) and output voltage within period (position in outer triangle ACE). A reduced switching frequency (5 kHz) has been chosen for better readability.

Experimental implementation of the methods presented in Section IV (composition of switching periods) is still under development, and it will be shown in a next paper.

## VI. Conclusion

Novel modulations for dual two-level inverter have been analyzed and tested in this paper. In particular, proposed techniques are based on the carrier-based approach, which makes them simpler for the implementation. The resulting output ac voltages have a multilevel waveform, equivalent to the one of a 3-level inverter, with a reduced ac current ripple. The carrier-based method has the advantage over SVM algorithm to be easily implemented in industrial DSP controllers without the need of additional hardware (e.g. FPGA). The proposed modulation techniques have been implemented and verified by both numerical simulations and preliminary experimental tests. The obtained results confirm their effectiveness.

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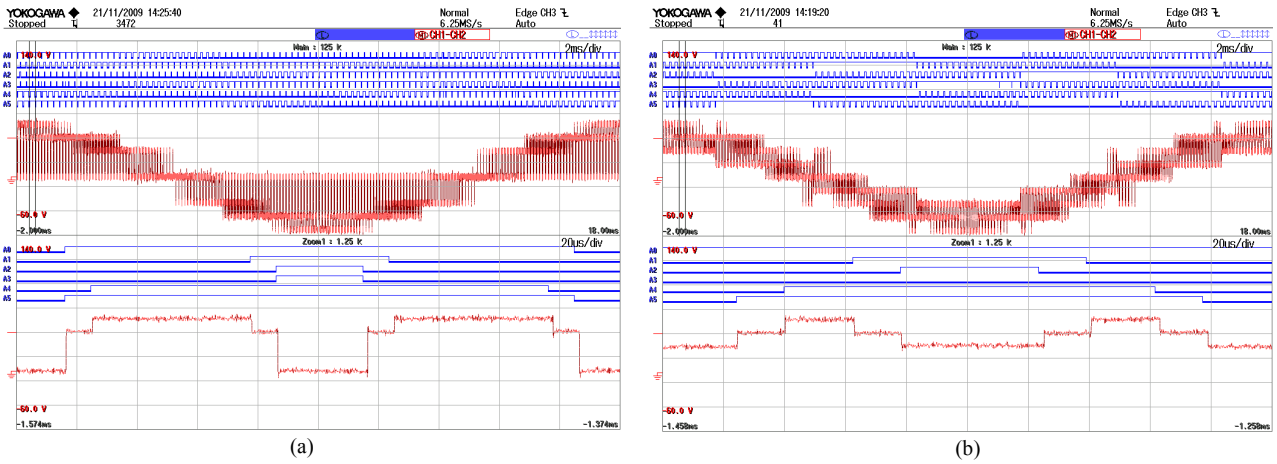


(a) (b)

Fig. 10. Experimental results. PWM pattern and voltage output for the independent modulation ($m$ = 0.75, $f_s$ = 5 kHz) with zoomed detail in the outer triangle ACE: (a) symmetrical zero vectors, (b) discontinuous.